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Design update and characterization of sub-10ps TDC ASIC in 28nm for future 4D trackers.

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High pileup densities imply new challenges. In this context, 4D tracking with a timing resolution of ˜10ps is essential for track reconstruction. For Muon Colliders, precise timing information becomes indispensable to mitigate the Background Integrated Beam (BIB). Therefore, a high-precision Time-To-Digital (TDC) stands as a crucial component in realizing 4D tracking. In 2023, we introduced the design of a 4-channel sub-10ps TDC ASIC fabricated using 28nm CMOS technology. This presentation highlights resolved technical issues since the initial design as well as the characterization setup and test outcomes.

Summary (500 words)

Timing plays a crucial role in addressing the challenges posed by high pileup densities in High Energy Physics (HEP) experiments. It becomes essential for reducing the combinatorial challenge of track reconstruction. Therefore, 4D trackers with ˜10ps timing will be transformative at future collider experiments. They provide completely new handles to detect and trigger on long-lived particles (LLP), expands the reach to search for new phenomena and enables particle-ID capabilities at low transverse momentum. Additionally, the timing information offers a solution to limit the Beam-Induced Background (BIB). In this context, 4D trackers with sub-10ps resolution will be transformative at future collider experiments.

As part of the CERN's EP-R&D-WP5 survey, which promote the selection of 28nm CMOS node as the next step in microelectronics scaling for High Energy Physics (HEP) designs, a 4-channel sub-10ps Time-to-Digital Converter (TDC) ASIC had been designed. It is based on a novel 2D Vernier ring-oscillator structure. The core architecture is composed of a differential voltage-controlled delay cells set at 50ps propagation delay. The ring-oscillator, enabled with a START trigger, coupled with a counter and a series of flip-flops that sample the oscillator's state at a STOP-trigger, is capable of performing time-interval quantization with 50ps time-steps and a range of 1.6ns. The 50ps ring-oscillator is interpolated by a factor of 8 using a second ring-oscillator with delay cells set to 56.25ps propagation delay. The 2D Vernier structure implemented reaches a resolution of 6.25ps, the difference of the propagation delays of cells in the two oscillators. Each channel receives one START and one STOP signal simultaneously sent to both ring-oscillators, performing a 6.25ps and a 50ps measurements of the two time-intervals, for example a time-of-arrival (TOA) and a time-over-threshold (TOT) measurement. The 1.6ns measurement range of the prototype can easily be extended in future iterations by simple addition of a flip-flop to the counter.

Given the 6.5ps resolution of the TDC, optimal jitter performance of the start and stop signal is critical. In 2023, a initial FPGA Mezzanine Card (FMC) was developed to assess the feasibility to meet the ASIC requirements using FPGA delays. After reaching performance limitations, a new hardware, based on external delay lines, dynamically controlled by the FPGA, was designed. In parallel, because of the aggressive pad pitch of the TDC (54um pitch and double row), a new version of the ASIC had been produced.

The final FMC hardware provides interfaces for comprehensive TDC characterization and comparison with simulations. This includes measuring the ring-oscillator frequency response according to the delay's voltage setting, plotting the Time Of Arrival (TOA) based on linear and random settings, characterizing the coarse and fine delay accuracy, etc.

The new ASIC was submitted in late 2023, with characterization expected to start in May 2024. The testing setup had already been produced and shows promising performance. This presentation, divided in three parts

introduces the test system we designed, their limitations and the TDC characterization outcomes.

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