Implementation and performance of ALTIROC3 readout ASIC for the ATLAS HGTD timing detector

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ALTAS HGTD

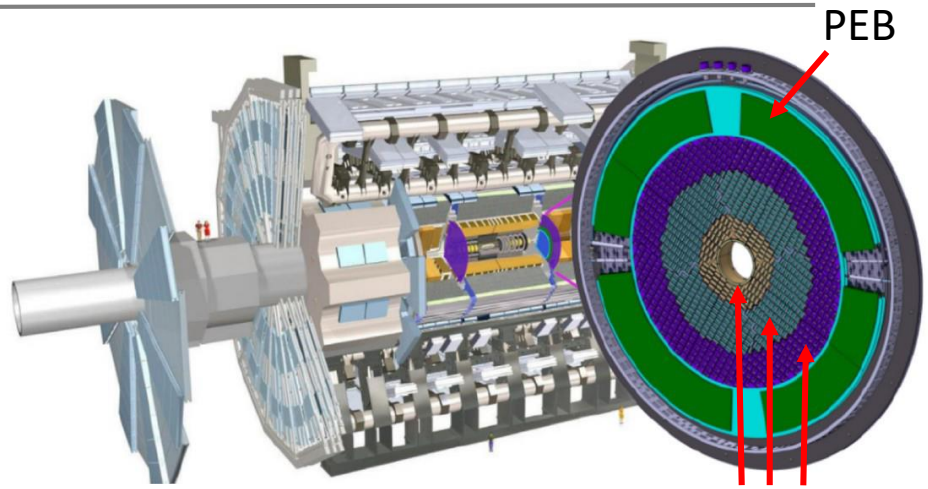
- With the high-luminosity environment of the HL-LHC comes increased pile-up making event discrimination more challenging.

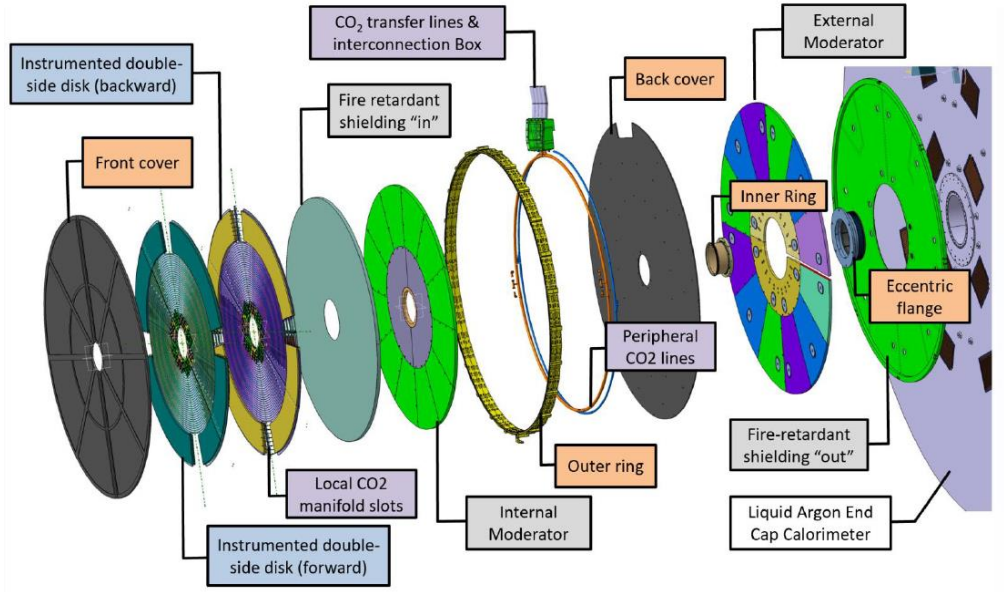
- High-precision timing measurements can be used to improve pile-up rejection when combined with Inner Tracker (ITk) position data.

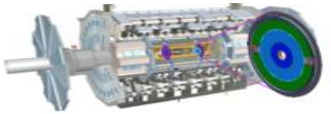
- The High-Granularity Timing Detector for ATLAS aims to provide :
  - Timing information with 30-50 ps per track (35-70 ps per hit) resolution over full lifetime
  - Luminosity information by reading hit counts for each bunch crossing

- Two endcaps located between the barrel and the calorimeters
  - Located at 3.5 m from the interaction point
  - Two double-sided disks per endcap
  - Active radius from 120 mm to 640 mm
  - Each disk is segmented into three rings of modules with different sensor overlaps

    70%, 54%, 20% overlap for inner, middle and outer rings



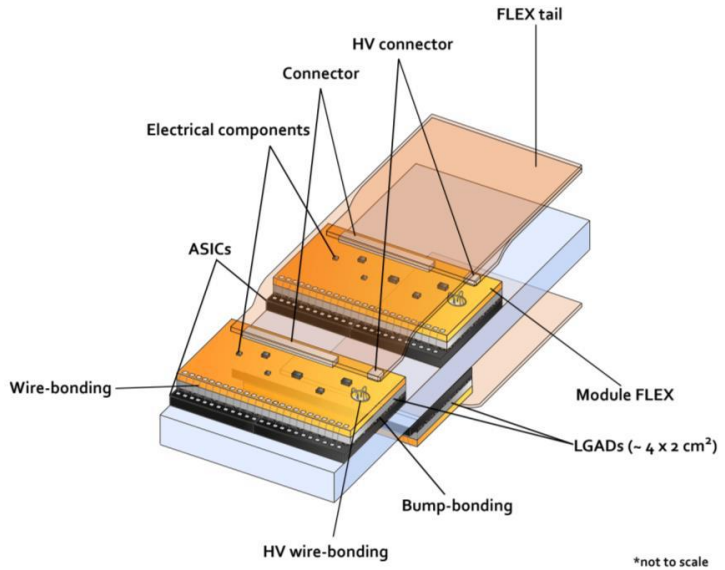


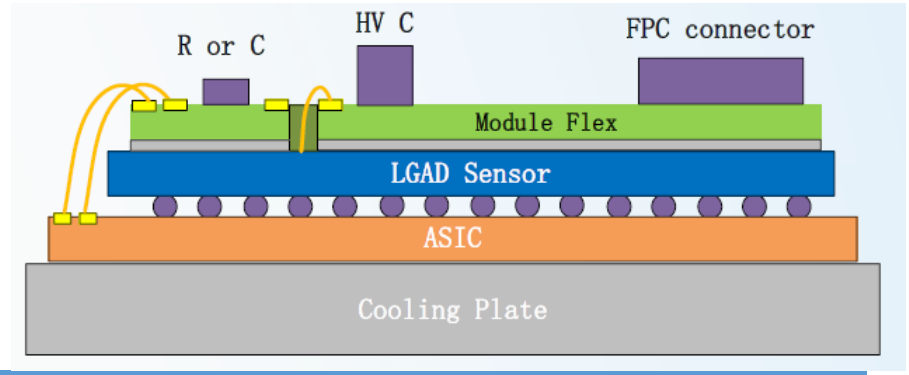


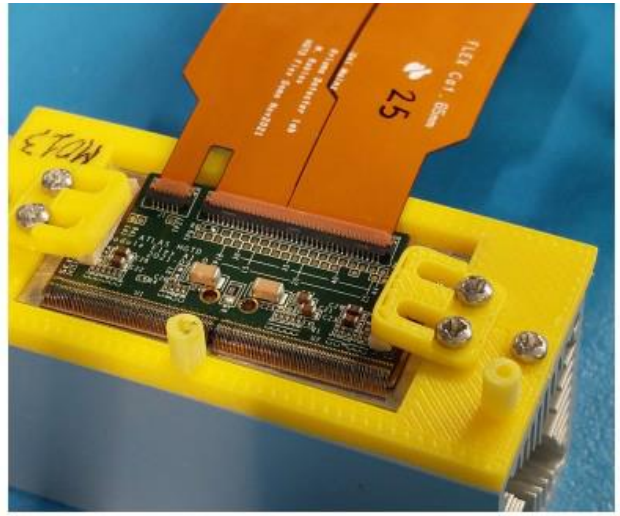
ATLAS HGTD

Modules

- A module is composed of two ALTIROC ASICs bump bonded onto two 15x15 LGAD sensors (hybrids)
- 8032 modules with 3.6 M channels in total
- 2 × 4 cm² modules, 450 pixels per module
- Wire Bonding I/O PADs for all other signals and power supplies
- ASIC in contact with the cooling plate (-30 °C)
- Connection to peripheral electronics with a flex PCB
- ➔ **Power supplies only from one side, voltage drop control is a key issue**







ATLAS HGTD

ALTIROC overview

- **Technology**: 130 nm 1.2 V CMOS TSMC
- **ASIC size**:

  Pixel area: 19.5 x 19. 5 mm²

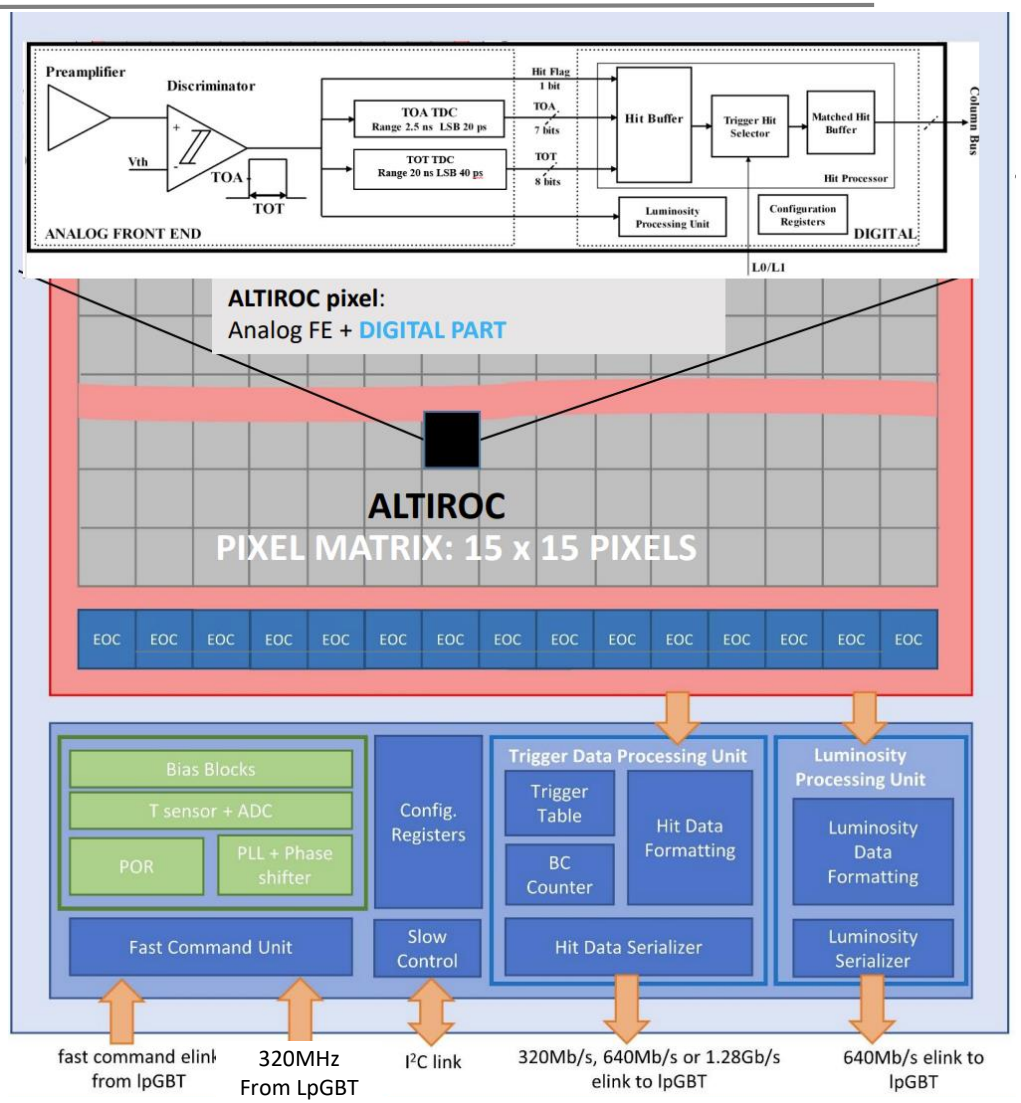
  Total area: 22 x 20 mm²
- **Pixel area**:

  15 x 15 pixel matrix

  Pixel size: 1.3 x 1.3 mm²
- **On-pixel electronics**:

  Analog: preamp + discriminator + **2 TDCs (TOA and TOT)**

  Digital: primary buffer (SRAM) to cope with latencies up to 38 µs, zero suppression, and secondary buffer to keep data after zero suppression
- Periphery composed of slow and fast interfaces, clocks control, bandgap, PLL, phase shifter, bias block…



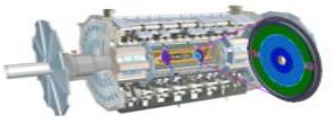
Verification of ALTIROC performances with IRDrop analyses

- ALTIROC is a large chip (>4cm²) and only powered from the bottom

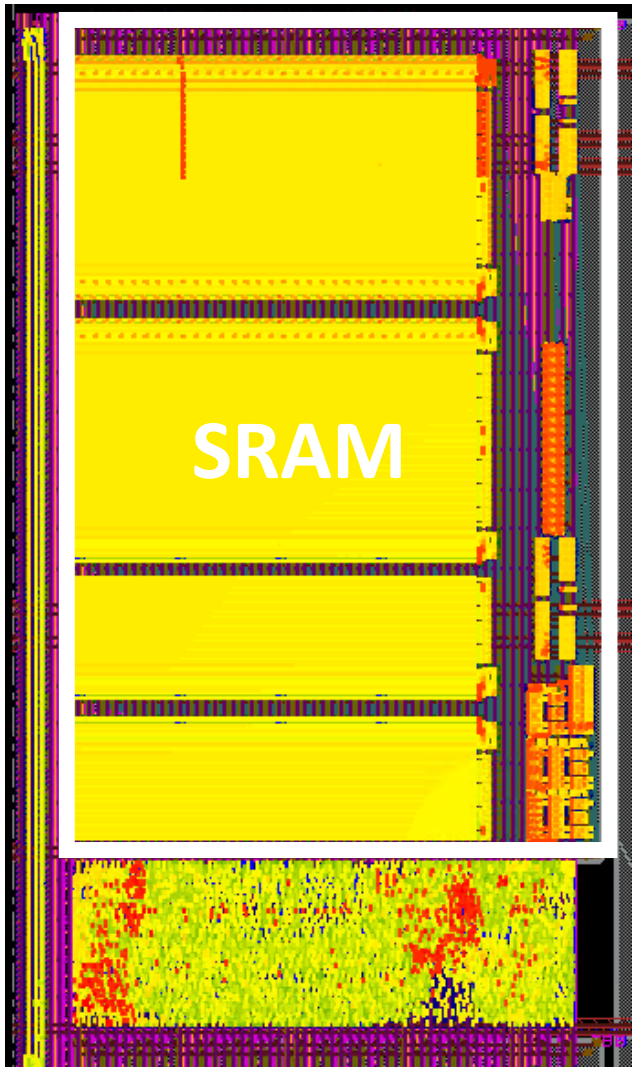
- Voltage drops can be critical in such chips as they can drastically degrade performance of the detector (minimum threshold, timing resolution)

- Main checks to do at chip level :
  - **Limit dynamic digital voltage drop to limit noise that can impact analog front-end**
  - **Limit voltage drops of analog front-end power domains (especially TDCs)**

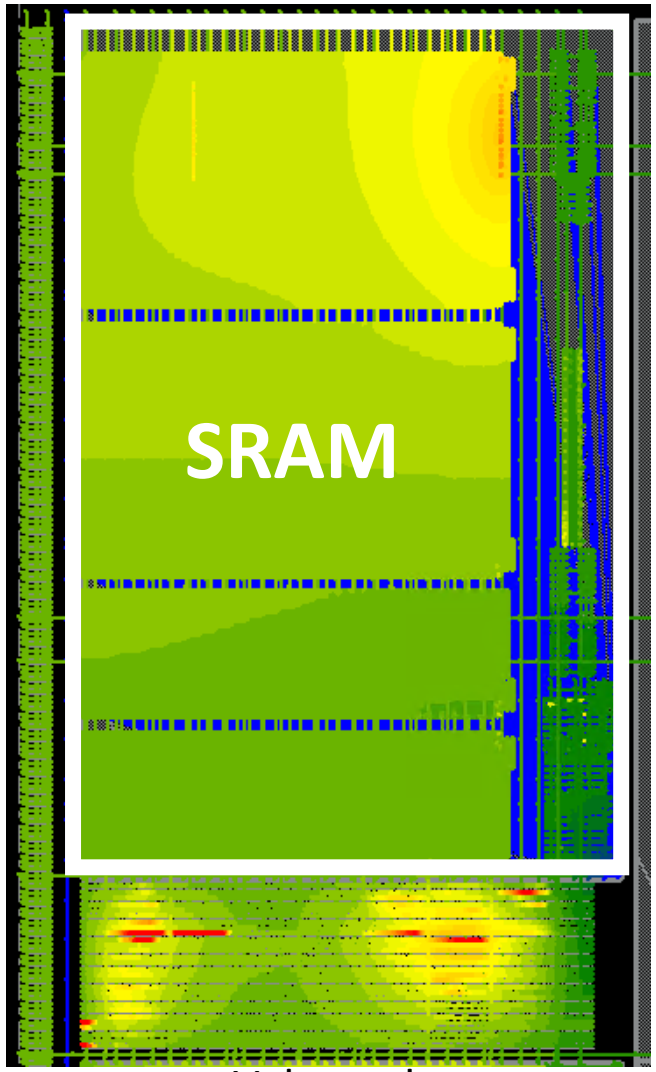
- ALTIROC is designed digital-on-top, which makes full chip verifications a lot easier :
  - Characterization of macros blocks designed with Virtuoso using **Power Grid View (PGV)**
  - Use Voltus for IRDrop analyses



Power Grid View generation for a macro block



Tap Current



Voltage drop

- SRAM (Custom block developed in Virtuoso) :
  - Same power domain as digital part
  - Power must be considered for digital IRDrop analysis

- Power Grid Views are generated to accurately capture the current and capacitance distribution inside a macro block :

➔ **Post layout simulation using spectre** (EMIR flow)

Current profile

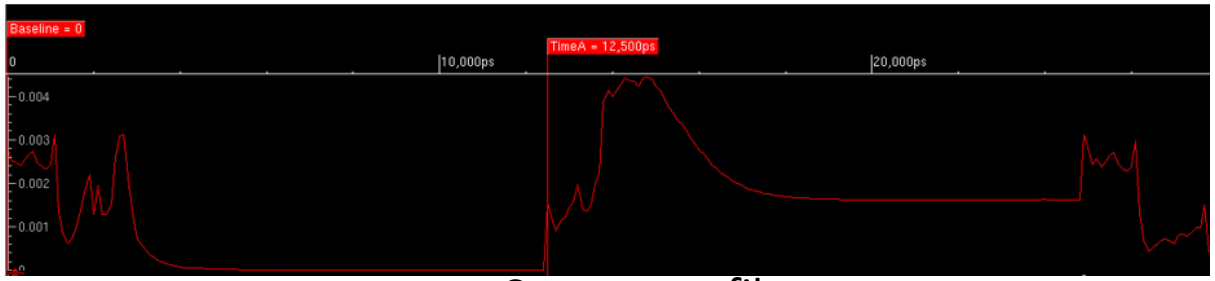
Accurate current distribution inside the block

➔ **Abstract view**

Power Grid information

➔ **Trigger file**

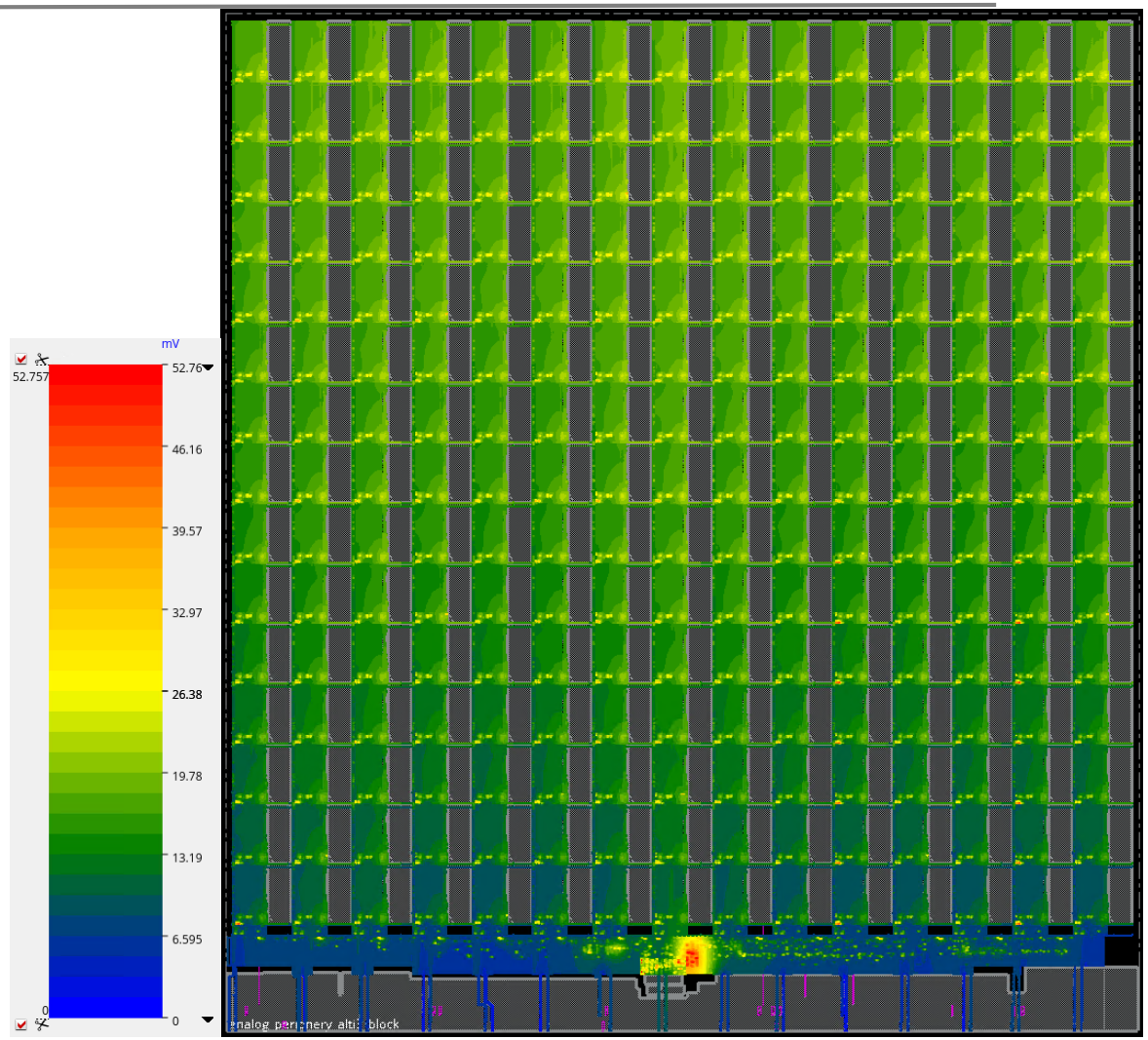
When to start current waveform during IRDrop analysis



Current profile

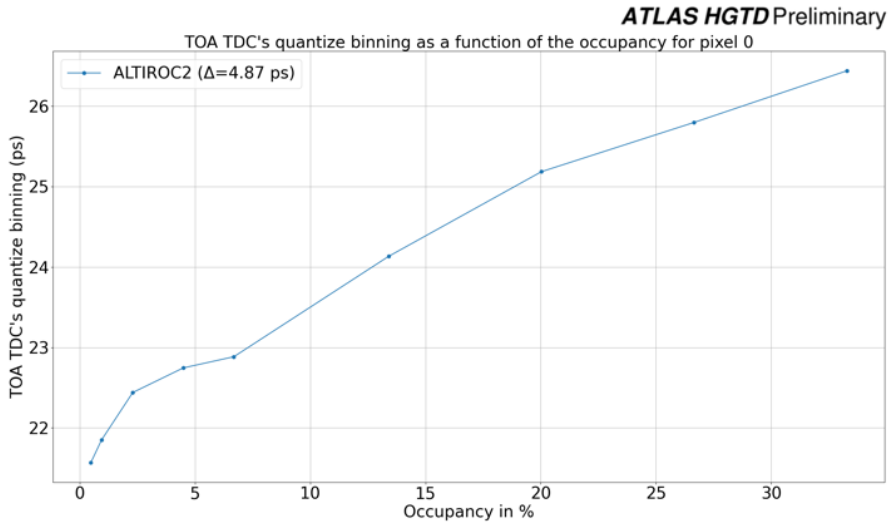
Full chip digital IRDrop analysis

- Integration of SRAM Power Grid View in Voltus flow
- IRDrop analysis uses activity file from digital simulations for its power analysis
  - Accurate activity for all standard cells
  - Trigger the current profile for each SRAM
- Several simulations to test worst possible cases
  - Broadcast I2C
  - Global reset
  - High occupancy + trigger in same bunch crossing
- Corner used is : FF, 1.32 V, -40 °C
- These simulations are really useful to fix local drops, especially in sensitive areas with large buffers
- ~50 mV drop for VDD and GND
  - Specification for this technology is <90 mV for VDD and GND

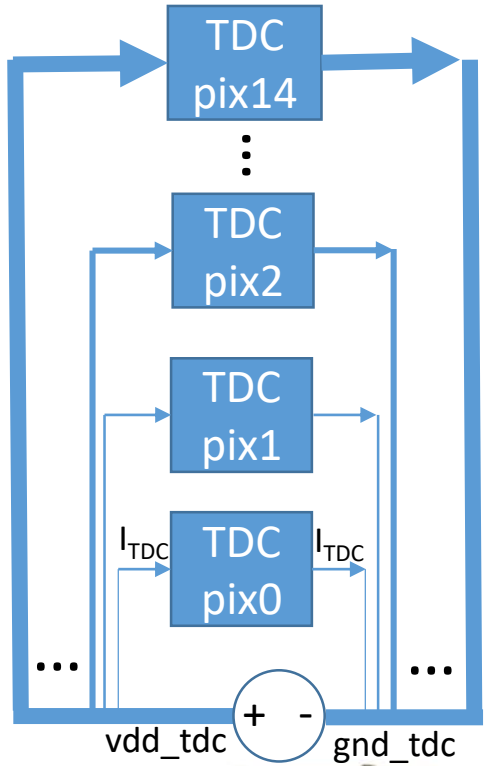


Full Chip digital voltage drop (high occupancy + trigger)

TDC performance issue



- During ALTIROC2 tests, we observed degraded performance of the TDCs inside each pixel when increasing hit occupancy
  - Pixels impact their neighbors when receiving a hit
  - Unstable TDC bin for different hit pattern
  - Identification of voltage drops as main contributor
- For ALTIROC3 the idea of implementing independent power routing for each TDC of each pixel was proposed :
  - Same resistance of power rail for each pixel
  - One PAD per power per column
- This solution uses more space, tradeoff between power domains must be considered

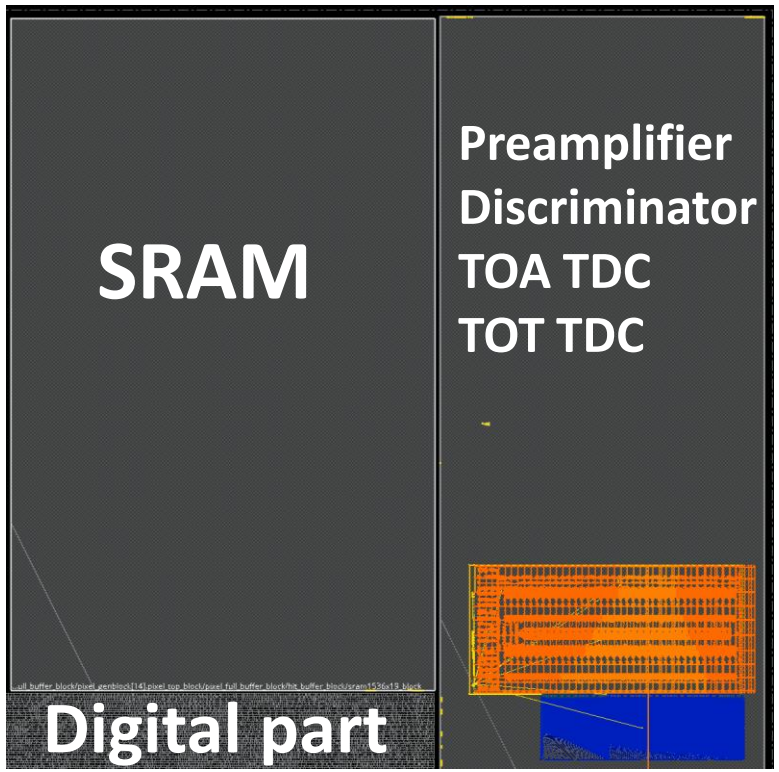


It was mandatory to verify the impact and the effectiveness of this solution with IRDrop analyses

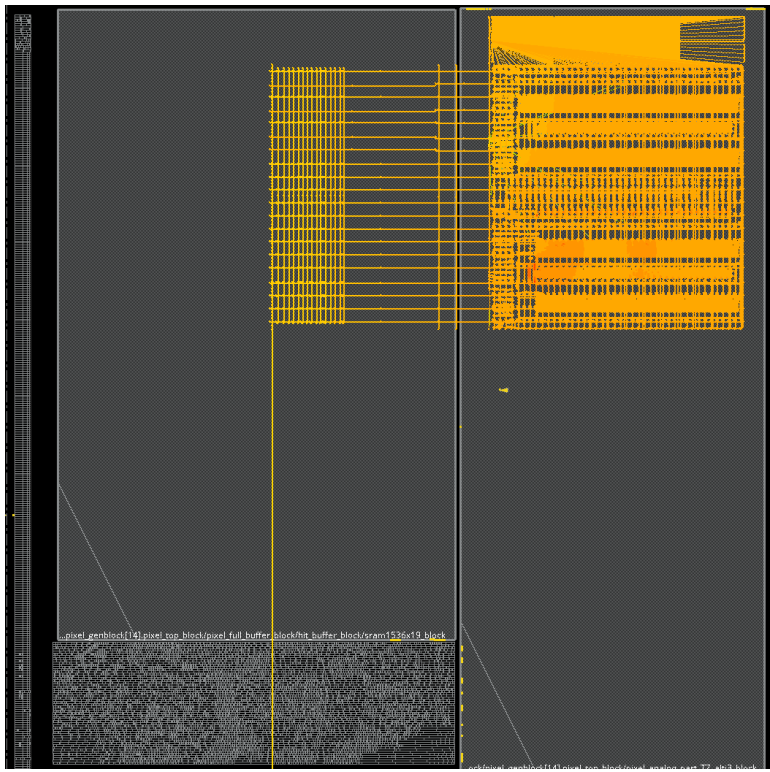
Setting up Power Grid View for the analog IRDrop

- Same flow as presented before to setup analog front-end Power Grid View : **TDC (TOA)**, TDC (TOT), Discri, Preamp
- One PGV for the analog front-end
  - Spectre simulation of the full chain (preamplifier, discriminator, TDCs)
  - Include power routing of all the different power domains
  - Trigger used is the signal starting the charge injection
- Run a digital simulation that sends this signal to all the pixels

  ➔ Generate an activity file
- Both analog PGV and activity files are used to run a full-chip IRDrop analysis



Voltage drop TDC TOA



Voltage drop TDC TOT

Full chip analog IRDrop analysis

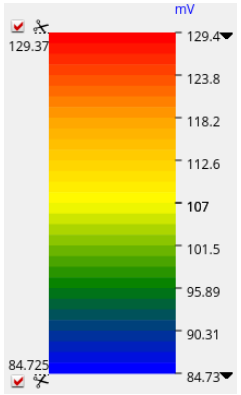
- Aggressive simulation in order to test the worst case (100 % occupancy)
- TDC can cope with reasonnable voltage drops, but the drop must be stable

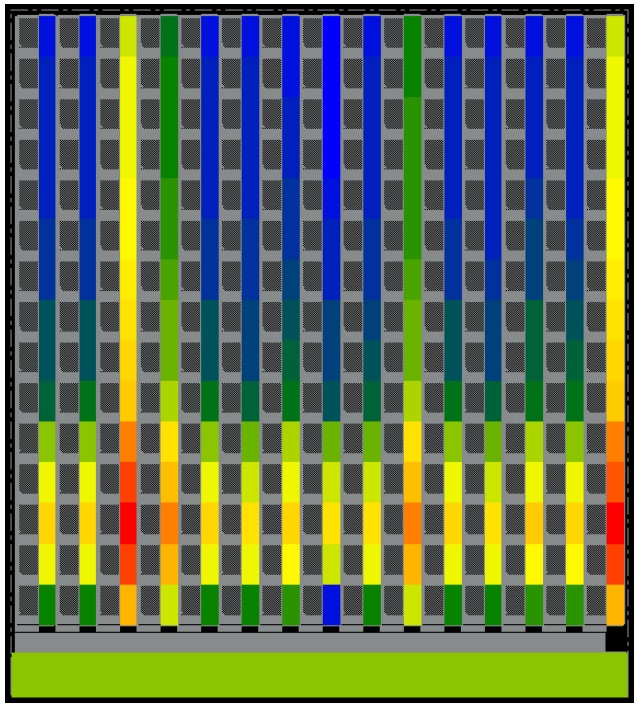
  ➔ The goal is to have the lowest drop possible while having similar drop for each pixel

- Validate that power routing is not missing any connections as it is done manually

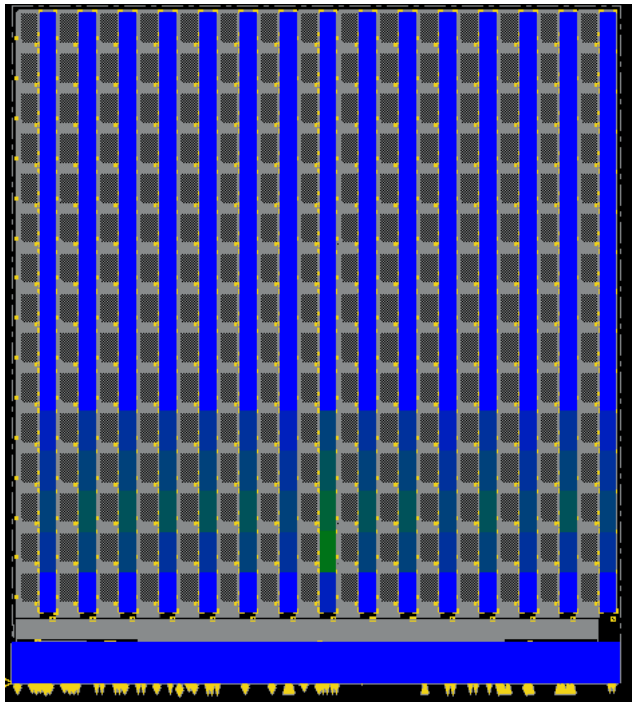
- Keep improving this power routing between ALTIROC3 and pre-production chip ALTIROCA

➔ Balance PADs positions for VDD/GND to remove discrepancies between columns

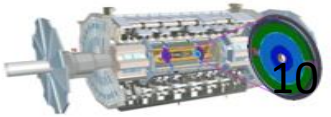




ALTIROC3 TOA domain based
~45mV difference, 129mV worst drop

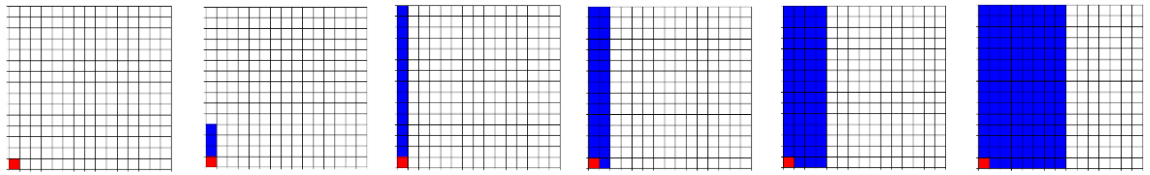


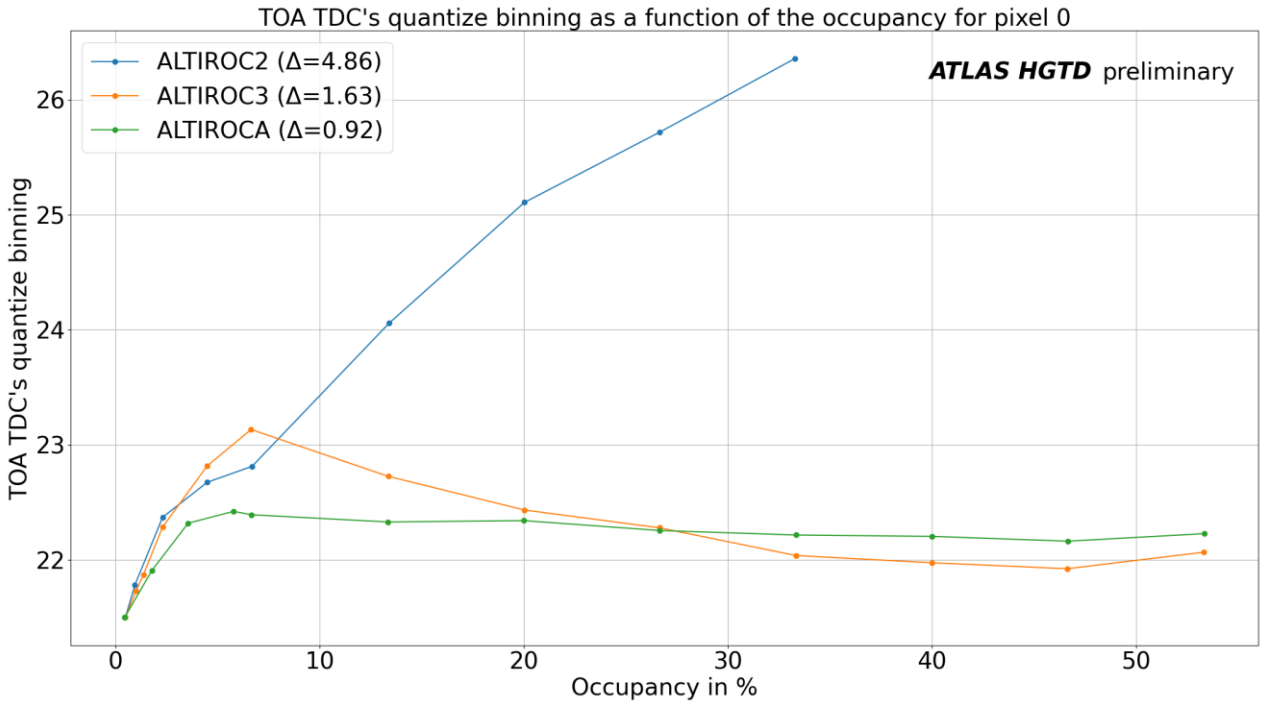
ALTIROCA TOA domain based
~18mV difference, 95mV worst drop



Independent power routing effectiveness

- Independent power routing implemented in ALTIROC3 is very effective but performance could still be improved
- Two other effects were observed :
  - **Voltage drops on wirebonds effect**
    - Need to reduce wirebond resistance
    - Try to reduce length as much as possible
    - Effect is very linear so offline correction should be possible if needed
  - **Noisy signal coupling with one of the bias of the TDC**
    - Shield between the two but large filling above
    - Tested with a Focused Ion Beam to physically cut the line
    - Signal removed in ALTIROCA





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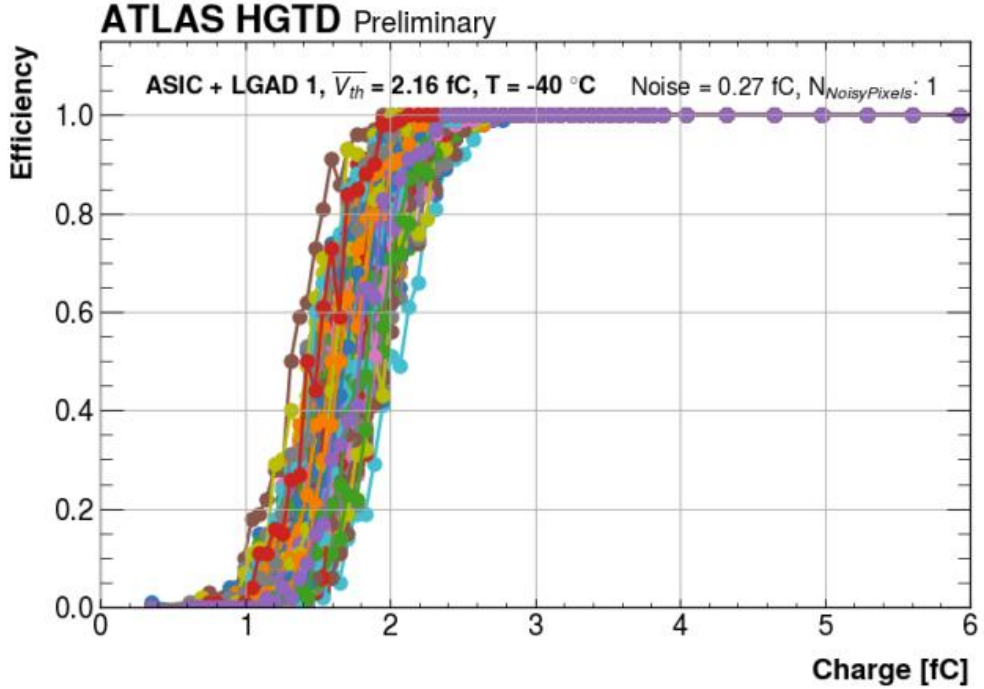
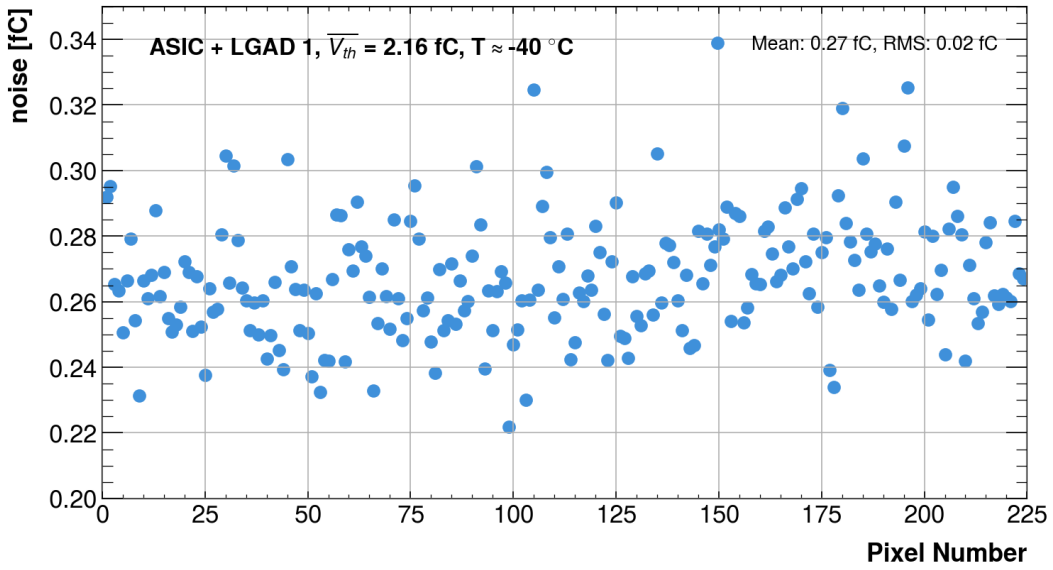
Hybrid Performances – Efficiency

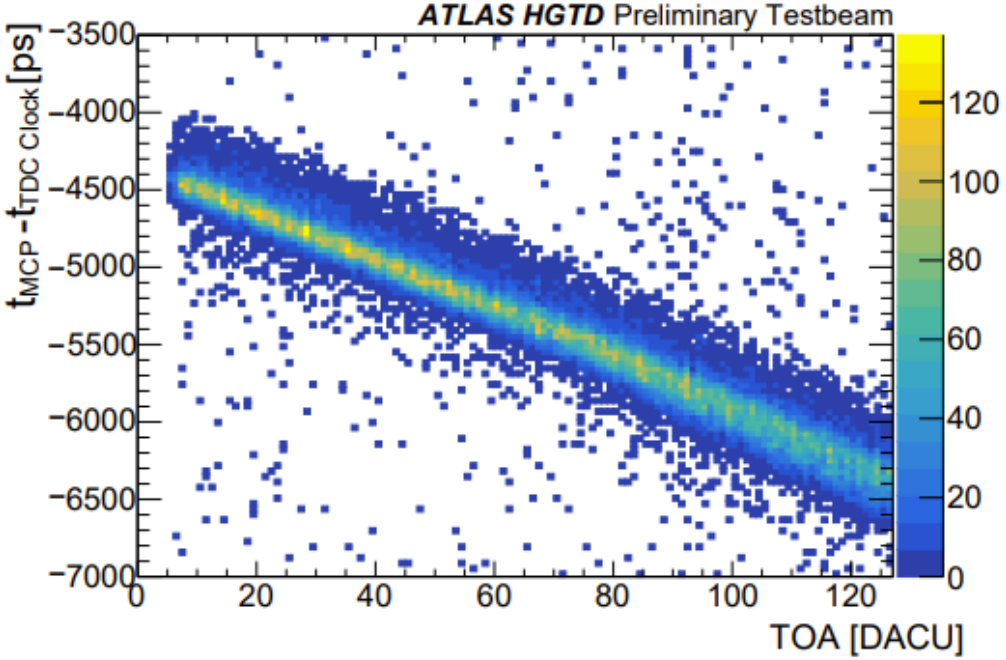
- Hybrid is ASIC + LGAD sensor
- S-curve for the 225 channels are obtained from a charge scan
- The threshold is defined as the charge value at 95 % efficiency
- Minimum detectable charge $Qmin$ is close to 2.5 fC in average

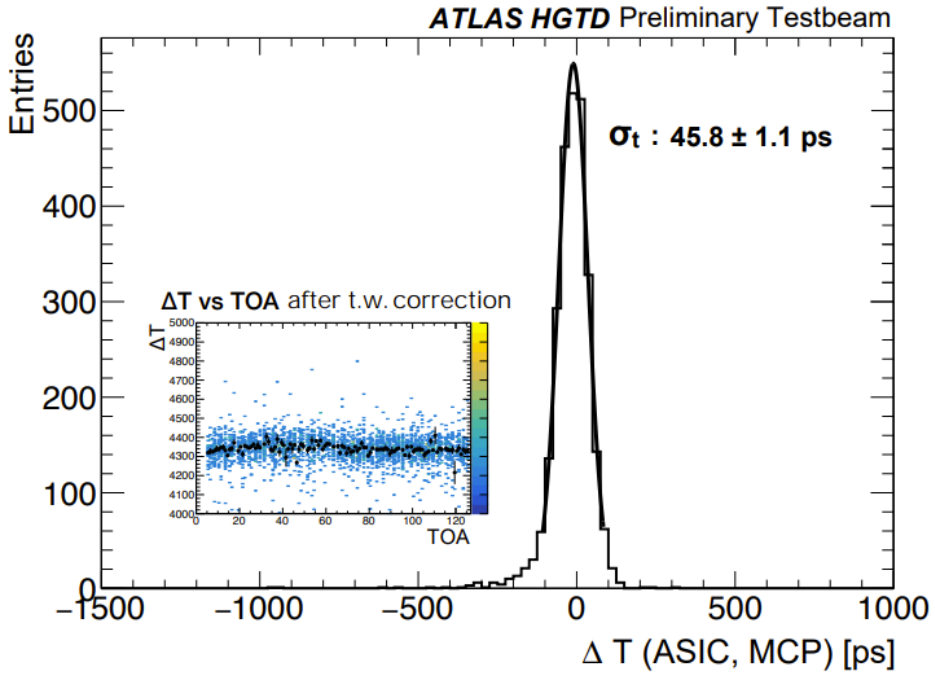




Hybrid Performances in testbeam - Resolution

- Correlation between the TOA measured by ALTIROC3+LGAD (X axis) and TOA measured by a reference Micro-Channel Plate (Y axis)
- The timing resolution of 45.8 ps is obtained with time walk correction (tests are done at room temperature)





ATLAS HGTD

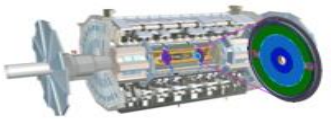
Conclusion

- Power Grid Views and Voltus are very convenient to run full-chip IRDrop analyses on analog blocks designed in Virtuoso

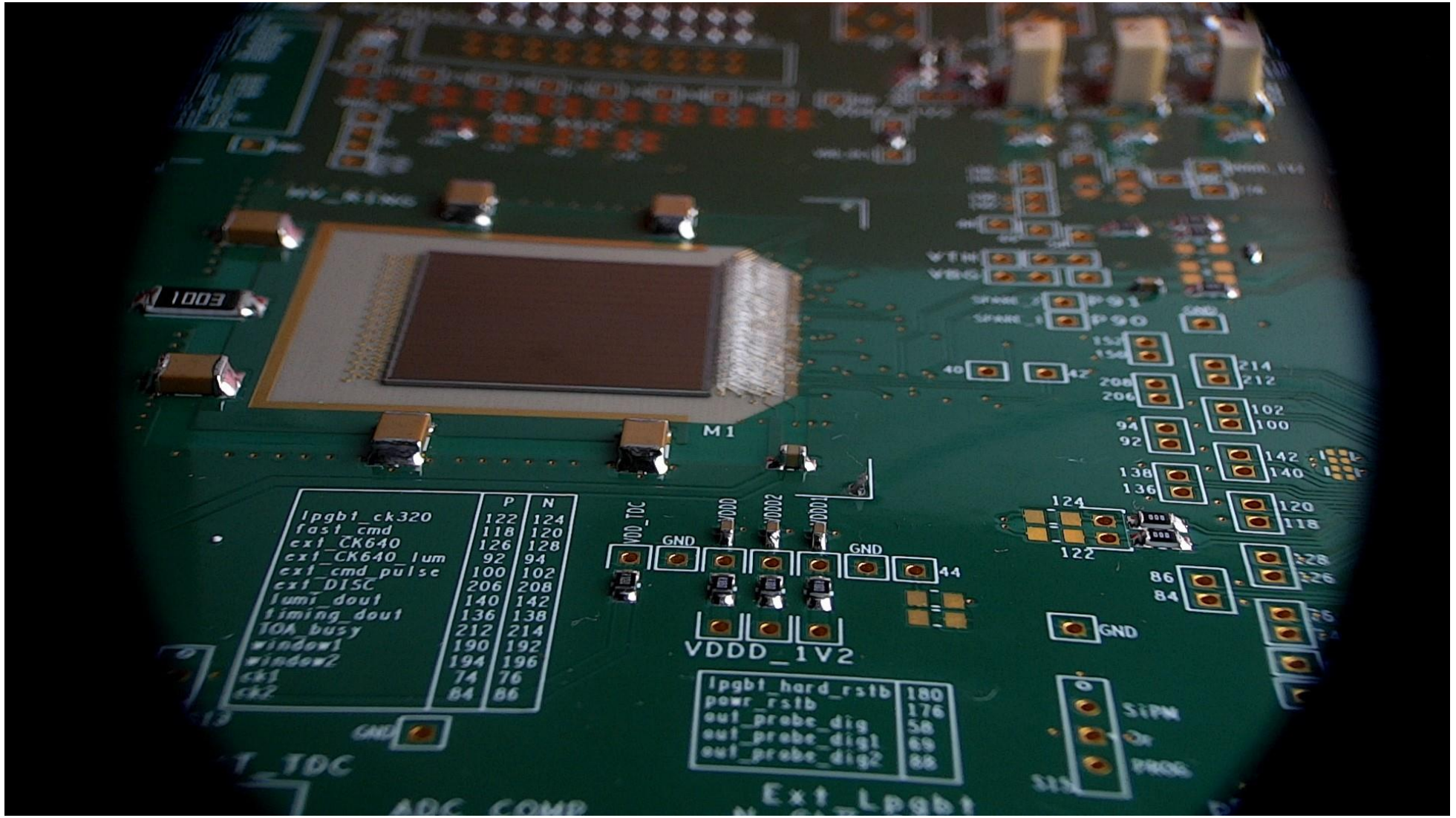
- Power Grid View generation can be difficult to setup the first time
  ➔ Thanks to CHIPS initiative at CERN and microelectronics team for their help and tutorials !
  ➔ I wrote some documentation with tips and solutions to frequent issues for abstract/PGV generation and IRDrop analyses, feel free to contact me if you need them

- ALTIROC3 ASIC is functional and meeting specifications

- Hybrid measurements:
  - Promising results with ALTIROC3 in testbeam
  - First hybrids with ALTIROCA are being characterized at testbeam
  - Full module testing coming soon



Thank you



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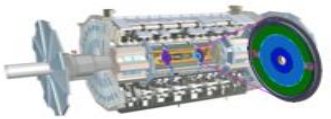
Backup



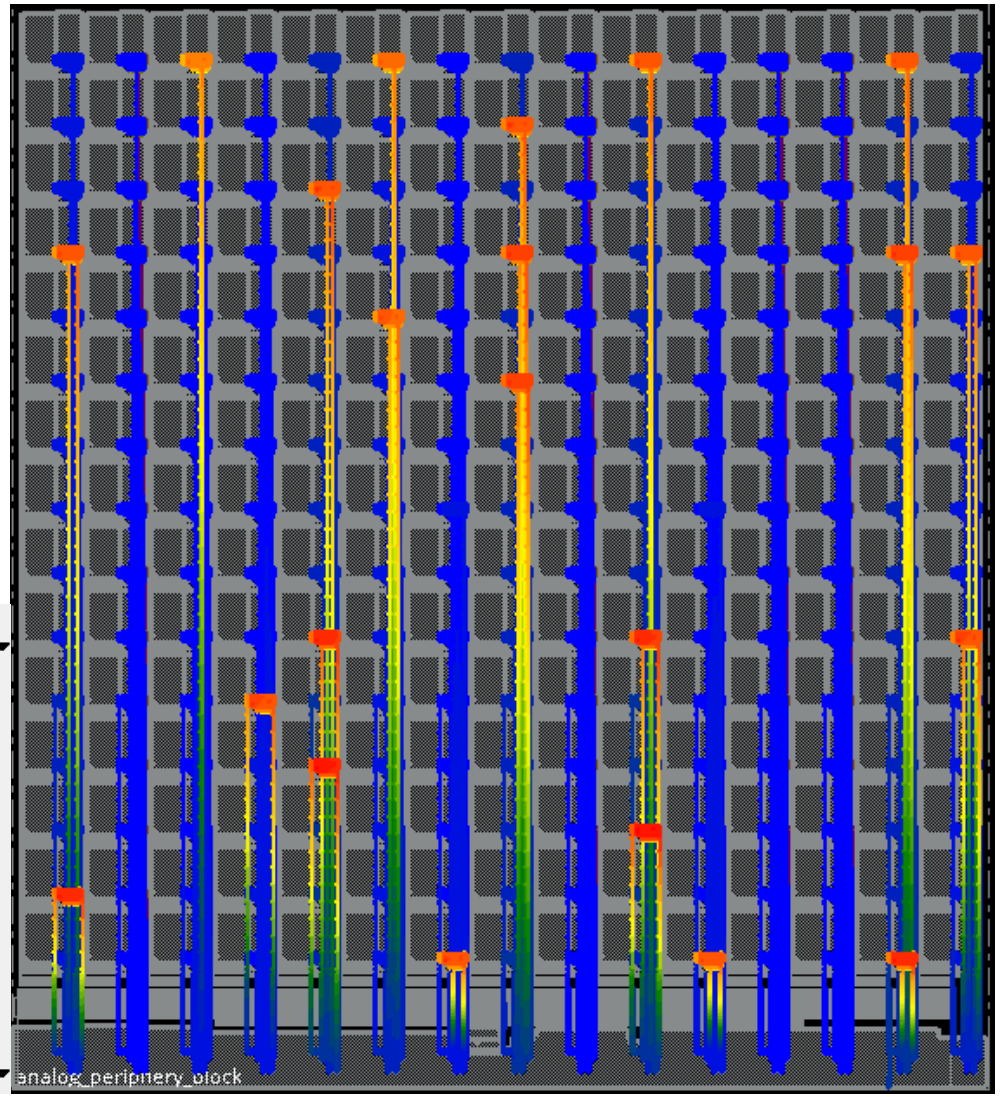
Full chip analog IRDrop analysis – Realistic case

- Can use trigger of the PGV for simulating more realistic cases
- Trigger take into account the enable signal of the TDC
- Simulated with 10% occupancy

- It is also possible to add RLC values to each voltage source for example to take wirebond into account

➔ set_rail_analysis_config

-default_package_resistor
-default_package_capacitor
-default_package_inductor



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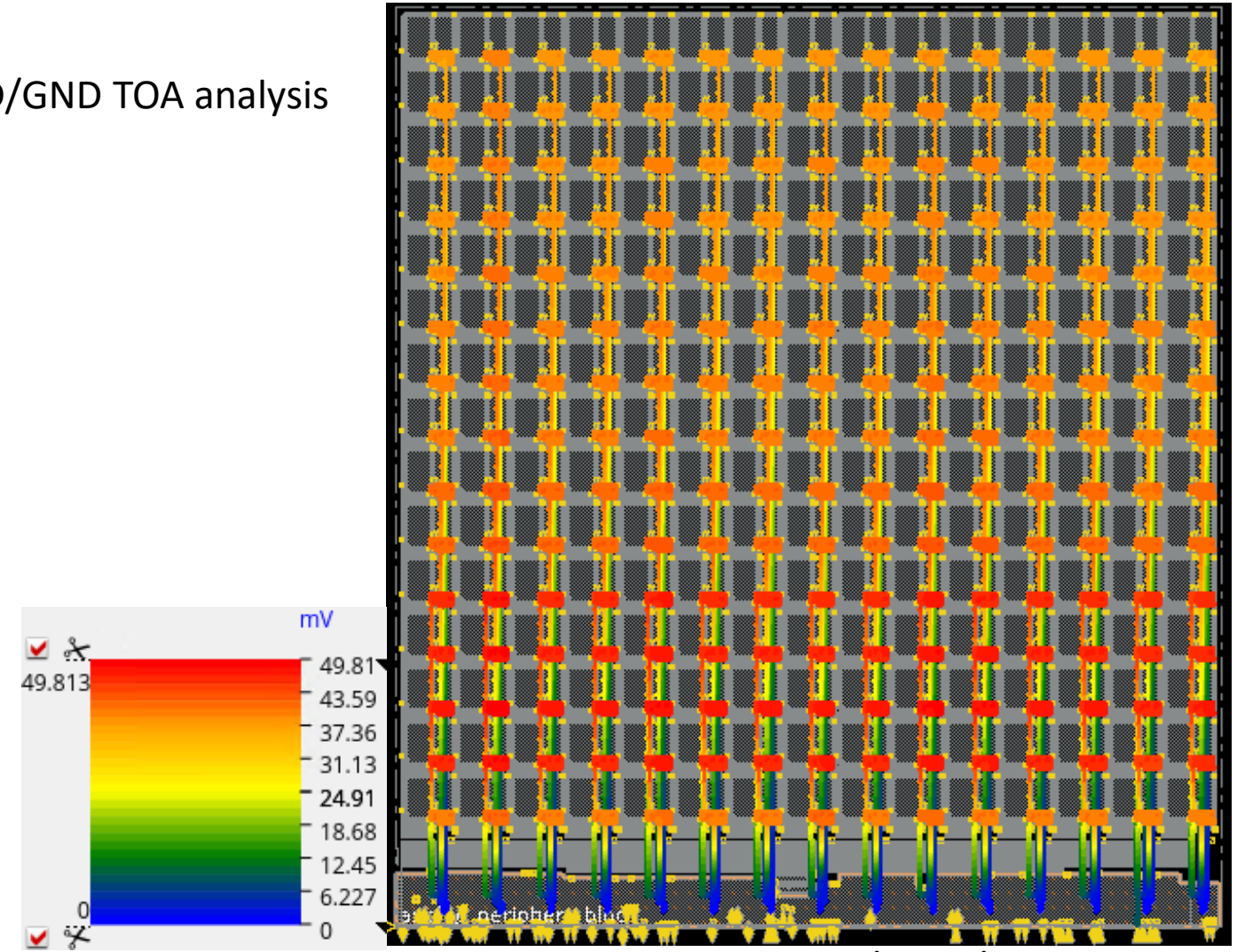
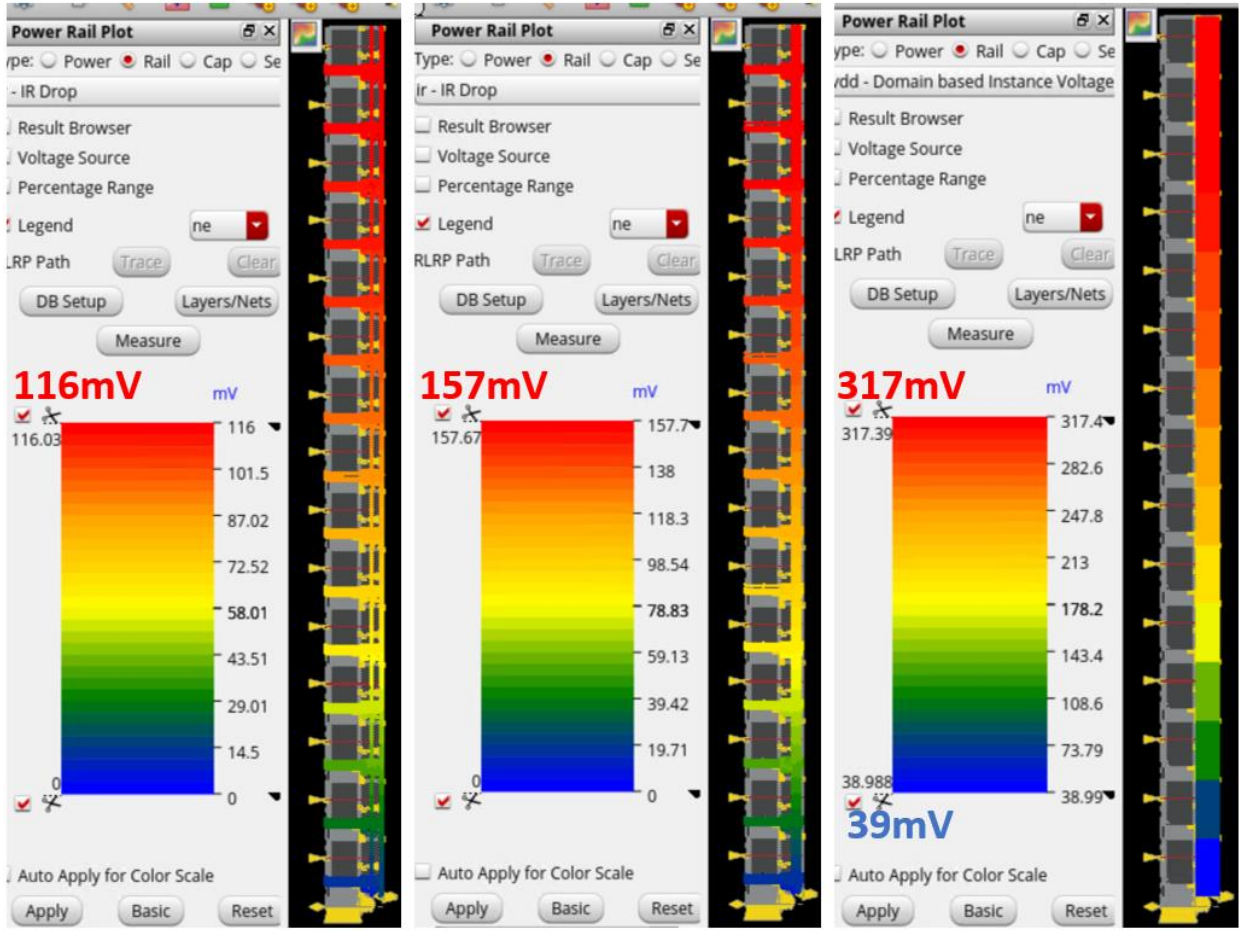
Full chip TOA IRDrop analysis

- Full chip VDD/GND TOA analysis



GND TOA voltage drop

ALTIROC2 TDC voltage drop analysis



Gnd_toa | Vdd_toa | Domain based gnd_toa + Vdd_toa

- Analysis done post foundry
- Agressive simulation/corner showed here, all the pixel's TDCs are triggered
- Issues observed in Altiroc2 :

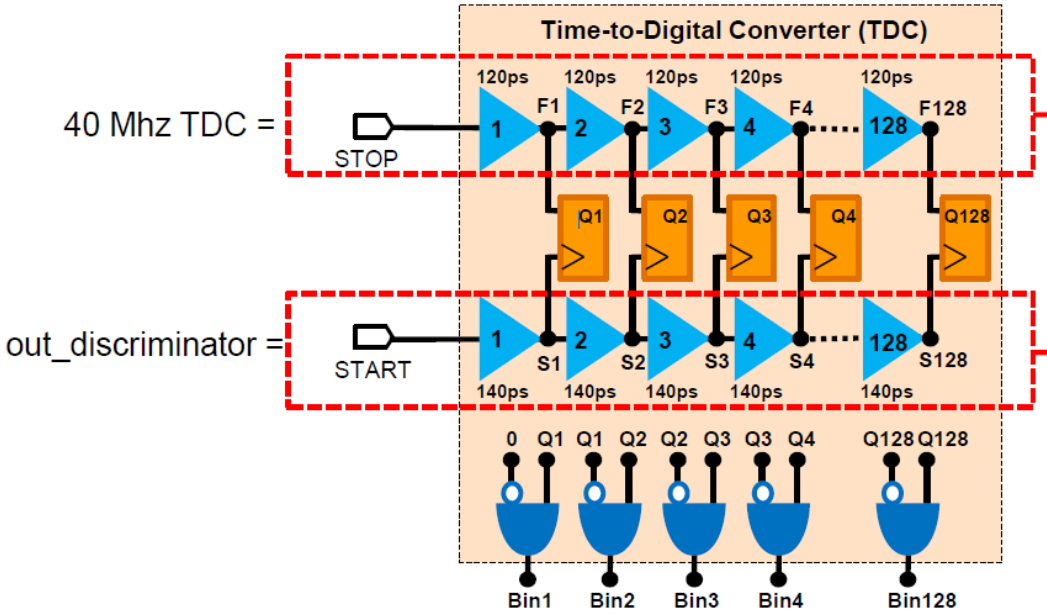
➔ High voltage drops on TDCs

➔ Drops depend on the activity

➔ TDC LSB is different depending on the number of pixel receiving a hit (impossible to tune)

TOA TDC Architecture (simplified): Vernier Delay Line

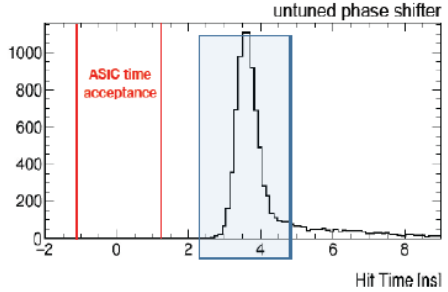
Simplified Block Diagram:



STOP signal propagates in the **Fast Delay Line** (Delay of one cell = **120 ps**)

START signal propagates in the **Slow Delay Line** (Delay of one cell = **140 ps**)

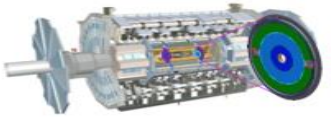
TOA measured in a 2.5 ns window



Bin (LSB) = 20ps = Vctrl_140p – Vctrl_120p

`TOA value= TOA out<6:0>*bin`

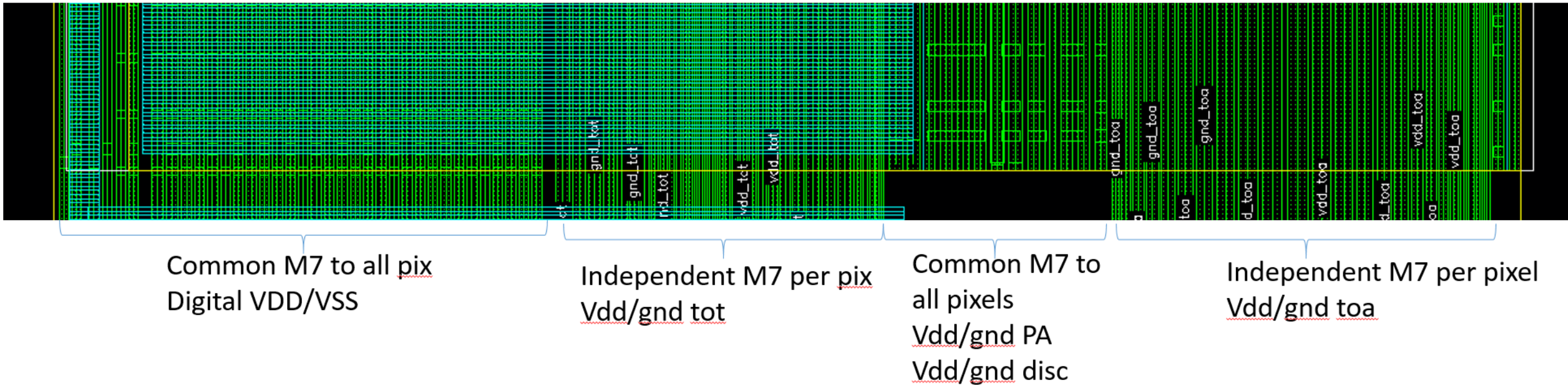
- The **START** pulse comes first and initializes the TDC operation
- The **STOP** pulse follows the **START** with a delay that represents the time interval to be digitalized
- At each tap of the Delay Line the **STOP** signal catches up to the **START** signal by the difference of the propagation delays of cells in Slow and Fast branches of the delay line i.e. **140ps - 120ps = 20 ps** that represents the LSB of time measurement
- The number of cells necessary for **STOP** signal to surpass the **START** signal represents the result of TDC conversion
- TDC range is equal to **128*20ps=2.56 ns**



ALTIROC3 power routing

- Implementation of independent power routing for each TDC of each pixel in Altiroc3
- Adjust width of M7 to control Resistance of each power line
- Independent power routing has been done manually in innovus at column level (now included in scripts)
- This new power routing is wider than before and impact digital power routing

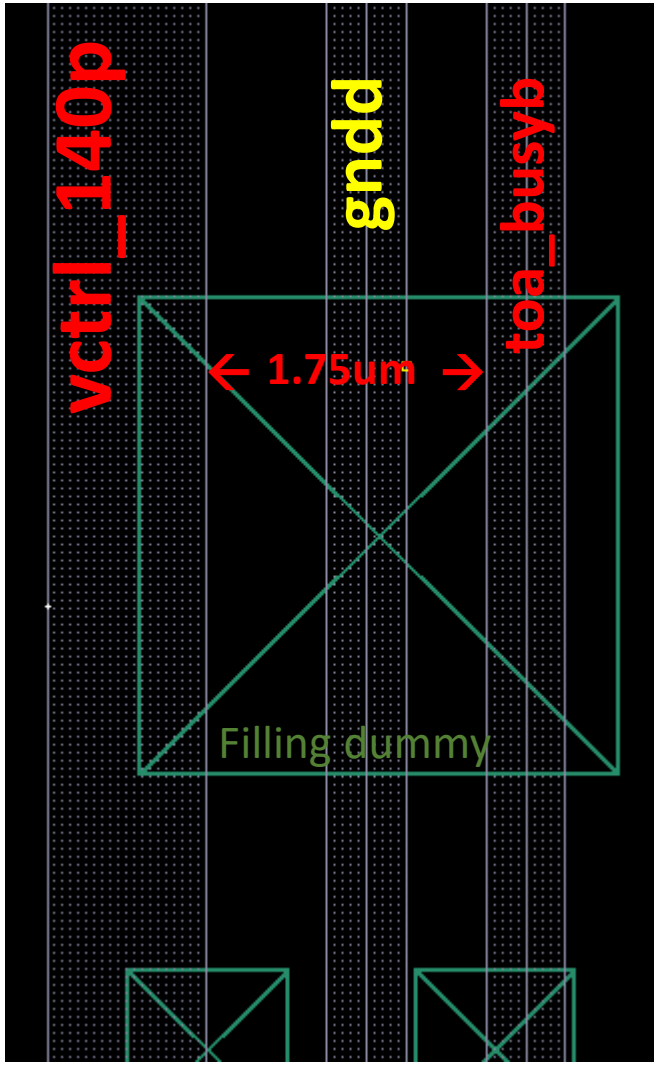
End of Column :



Crosstalk between vctrl and toa_busy

- Noisy signal coupling with one of the bias of the TDC
- Vctrl is one of the bias of TOA TDC
- Toa_busy is a debug signal (not possible to disable)
- Shield done using gndd, width/spacing was quite small
- This bias is a sensitive signal
- These lines are in parallel for 15x2cm
- Filling is done using scripts
  - It is possible to remove filling from some area but we didn't see the issue early enough
- FIB (Focused Ion Beam) was done to cut the toa_busy in several columns (SERMA company)

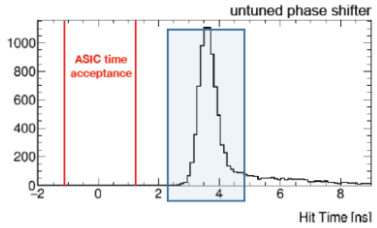
  ➔ Effect completely removed for these columns



ASIC Specification

Charge dynamics : up to 100 fC
Noise : < 0.5 fC
Cross talk : < 2 % to guarantee single hit with 2 fC threshold

TOA :
Measurement window 2.5 ns
Jitter : 25 ps for Q = 10 fC
65 ps for Q = 4 fC
Conversion time < 25 ns (TDC LSB of 20 ps)



TOT :
For 100 fC, TOT < 20 ns

Landau MPV	4 fC	> 10 fC
Time Walk contribution rms (ps)	25	10
TOT resolution for VPA (ps)	120	120
TOT resolution for TZ (ps)	120	70

Conversion time < 25 ns
TDC LSB of 120 ps enough but TZ better use with 40 ps

40 MHz Clock of the TDC :
Jitter < 10 ps
ASIC global clock aligned with better than 100 ps
Clock skew between channels in ASIC : +/- 150 ps

Luminosity
Provide ASIC number of hits per bunch crossing on two time windows
Similar alignment as for the clock but skew relaxed to +/- 200 ps

Read out bandwidth and latency :
Should cope with 1 MHz with 12.8 µs and 0.8 MHz with 35 µs
ASIC bandwidth adjustable by slow control : 0.32, 0.64 or 1.28 Gb/s

Radiation tolerance :

	TID [MGy]		NIEL [n_{eq}/cm^2]		SEE [h/cm^2]	
ASIC Barrel	2.0	(2.25)	2.5×10^{15}	(1.5)	$1. \times 10^{15}$	(1.5)

ASIC power dissipation < 1.2 W

Calibration injection :
Range 0 – 100 fC
Rise time : 0.5-1.5 ns

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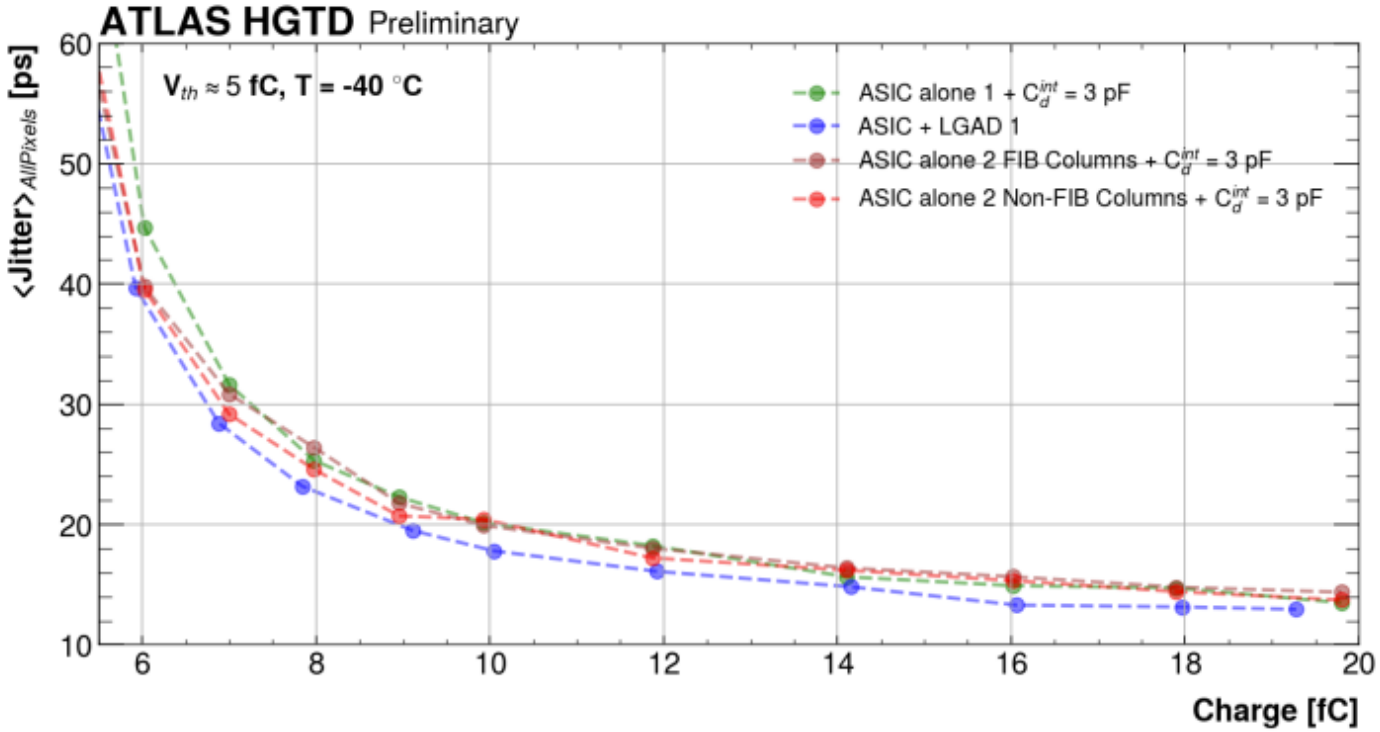
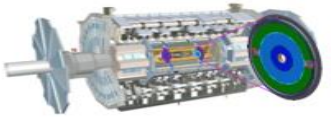
Hybrid Performances – Jitter

- Mean jitter across all channels as function of charge with a threshold of ~5 fC for different boards with ALTIROC3
- The temperature shown in the figure is the temperature inside the climate chamber
  ➔ At −40°C the temperature of the hybrid is around −30°C
- Jitter increase close to the charge used for threshold alignment is caused by the lower pulse slope on top of the pulse

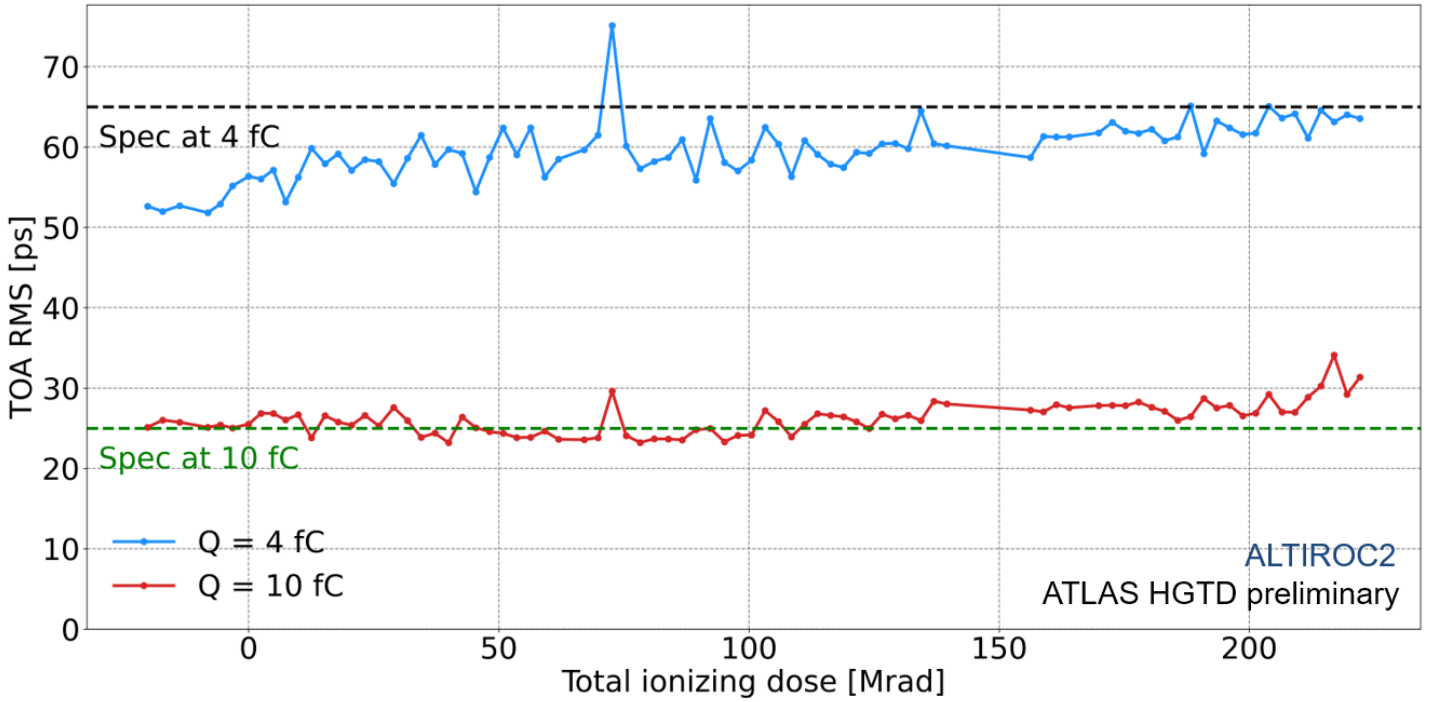




ATLAS HGTD

ASIC Performances – TID

- Mean Time Of Arrival (TOA) jitter for 4 and 10 fC injected charges versus total ionizing dose for **ALTIROC2** ASIC alone showing stability under radiation up to 220 Mrad.
- Dose rate : 3 Mrad/h Temperature : 22°C
- Jitter stays stable with the increasing Total Ionising dose



ATLAS HGTD

ASIC Performances – SEE

- Two main goals :
  - Prove the effectiveness of the triplication
  - Show a limited number of data frames corrupted

- Two campaigns in two different facilities (CAL at Nice and ARRONAX at Nantes)
  - Use of 65 MeV proton beam to realize irradiation test

- Counters implemented inside ASIC to count single errors in triplicated registers

- Expected erroneous registers at HL-LHC : no error expected on the configuration registers

- Erroneous timing at HL-LHC : 5×10^{-9}% of data frames