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Implementation and performance of ALTIROC3 readout ASIC for ATLAS HGTD timing detector

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ALTIROC3 is a 2x2 cm² CMOS 130nm ASIC with 225 channels to read-out the new ATLAS HGTD detector for the High Luminosity-LHC upgrade. It was designed using "Digital-On-Top"flow and triplicated for radiation hardness. Chip level IR-Drop analyses were performed to evaluate accurately the power distribution impact, especially for the Time- to- Digital- Converters implemented in each pixel. These studies that drove implementation choices will be presented as well as the challenging performance obtained at system level with a jitter of 25 ps for input charges of 10 fC and under irradiation (SEE and TID).

Summary (500 words)

The increase in particle flux during the high luminosity phase of the Large Hadron Collider (HL-LHC) and the instantaneous luminosities up to L ⊠ 7.5×1034 cm−2 s-1, will significantly impact the performance of the ATLAS detector. Pile-up mitigation is one of the main challenges as 200 interactions per bunch crossing are expected on average. The new High Granularity Timing Detector (HGTD) located in the forward region with pseudo-rapidity range from 2.4 to about 4.0 will provide high-precision timing information that allows to distinguish between collisions occurring close in space but well-separated in time.

The HGTD incorporates two double-sided layers of Low Gain Avalanche Detectors (LGAD) sensors. These sensors are designed to provide timing information for minimum ionizing particles with a time resolution better than 70 ps per hit (equivalent to 50 ps per track at the end of its operational lifetime), crucial for accurately assigning particles to their respective vertices.

This ASIC is bump-bonded onto a 15 x 15 channel matrix 1.3 mm x 1.3 mm LGAD sensor. Operating in a highly irradiated environment (200 MRad and 2.5 x 1015 neq/cm2 fluence), the chip has been tested thoroughly since May 2023.

Each channel of the ASIC integrates a 1 GHz bandwidth preamplifier, followed by a high-gain leading-edge discriminator and two TDC used for Time-of-Arrival and Time-Over-Threshold measurements, along with a 35 µs depth memory. Zero suppression is implemented at pixel level. The ASIC also provides luminosity measurements. Timing data are output at a rate up to 1.28 Gb/s and luminosity data at 640 Mb/s to the DAQ. The ASIC has been designed full Digital-On-Top and is triplicated to ensure its robustness against SEE.

Testbench measurements demonstrate the ability of the ASIC to detect charges as low as 4 fC with 95 % efficiency. The jitter is smaller than 25 ps (65 ps) for a charge of 10 fC (4 fC respectively). This performance is achieved while keeping a challenging power consumption smaller than 4.5 mW per channel.

This 2x2 cm² chip is powered only on one side, which leads to voltage drops along the column when several hits occur at the same time. The expected occupancy is expected to be up to 10 % per bunch crossing. For the ALTIROC3 design, advanced Power Grid Views were generated for the whole analog front-end, allowing to simulate the IR Drop effects at chip level, in particular for the Time-to-Digital Converters. It was then possible to simulate and validate solutions such as independent power routings to each pixel that prove on testbench to greatly improve the TDC performance of ALTIROC3 for different occupancies.

ALTIROC3 has also demonstrated a very good performance under TID irradiation up to 200 Mrad and under SEU and SET.

This talk will decribe the implementation choices done to reach the challenging requirements as well as the

measurements done under irradiation, at system level and in testbeam conditions.

Author: SOULIER, Alexandre Pierre (Université Clermont Auvergne (FR))

Presenter: SOULIER, Alexandre Pierre (Université Clermont Auvergne (FR))

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