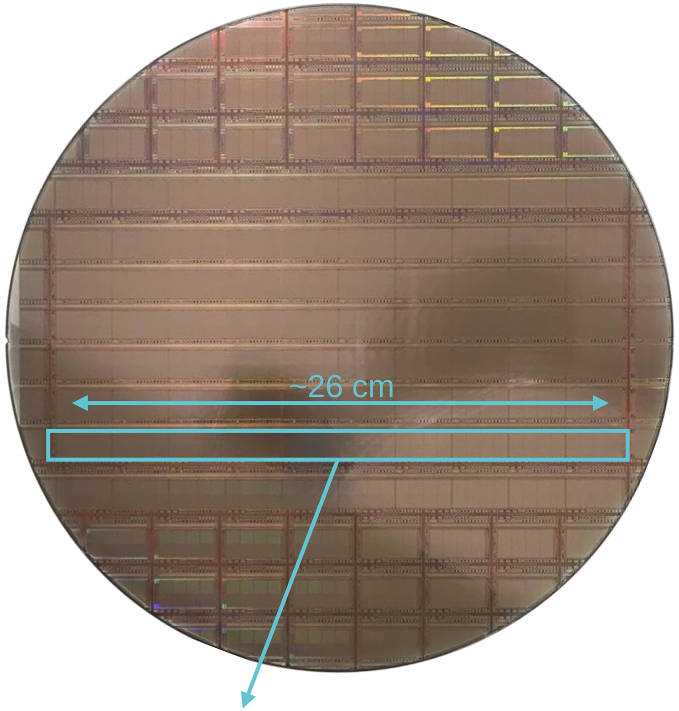
Investigation of non-idealities of pulsing circuitry in the ALICE ITS3 MOSS monolithic sensor

Simone Emiliani, on behalf of EP-R&D Work Package 1.2 and ALICE ITS3 team

02/10/2024

Monolithic Stitched Sensor (MOSS) ASIC

ER1 submission wafer



- **ITS3 → ALICE new inner tracker with wafer-scale bent silicon detector:**
  - Minimized material budget.
  - Reduced radial distance from interactions.
- Small-electrode Monolithic Active Pixel Sensor (MAPS) which features low input capacitance.
- Stitching technique.
- 65nm CMOS imaging technology.

ITS3 - half barrel dummy silicon model

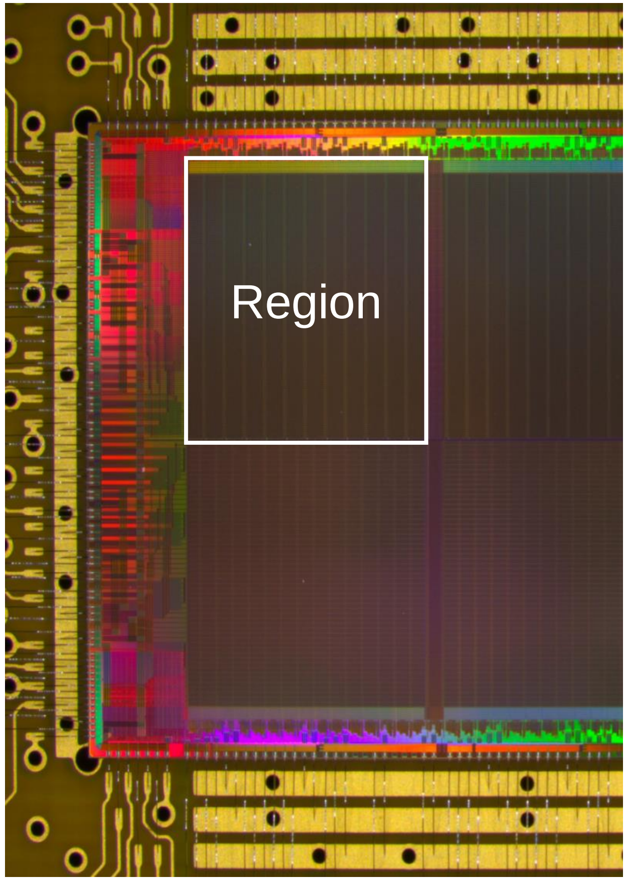
- MOSS chip was the first stitched chip developed by the team.
- 6.72 Mpixels grouped in independent regions (in terms of power, biasing, IOs).
- **The characterization of MOSS is crucial for the development of its successor (MOSAIX), the final prototype for ITS3.**

Development of the MOSAIX chip for the ALICE ITS3 upgr
Pedro Vicente Leitao

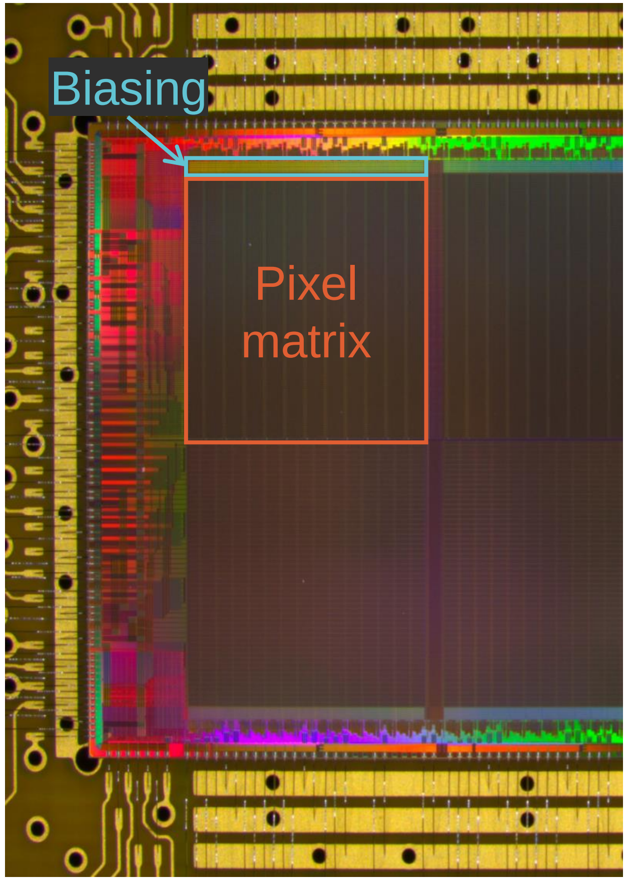
Power distribution over the wafer-scale monolithic pixel d
Szymon Bugiel

Yield Characterisation and Failure Analysis of the Monolit...
Gregor Hieronymus Eberwein

MOSS pixel matrix



MOSS pixel matrix



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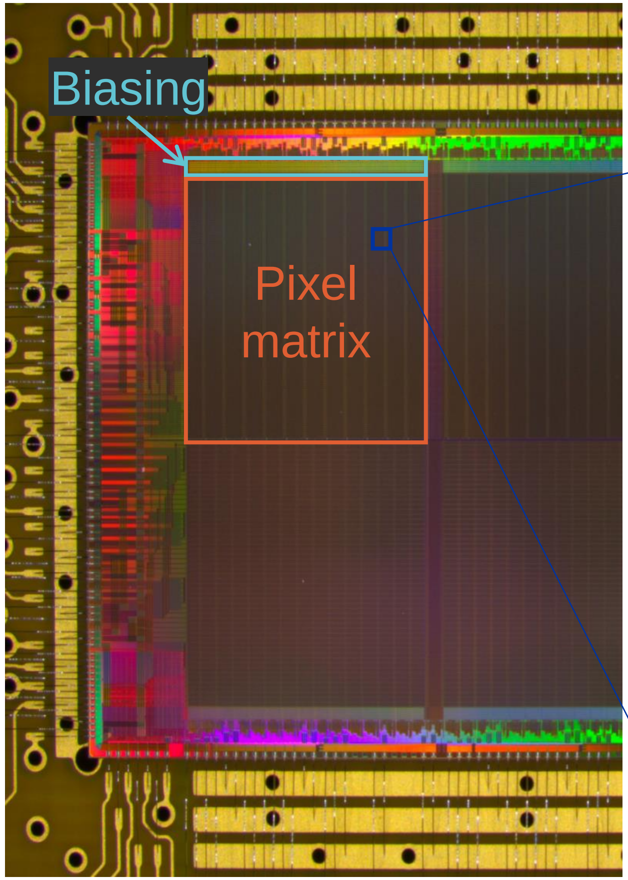
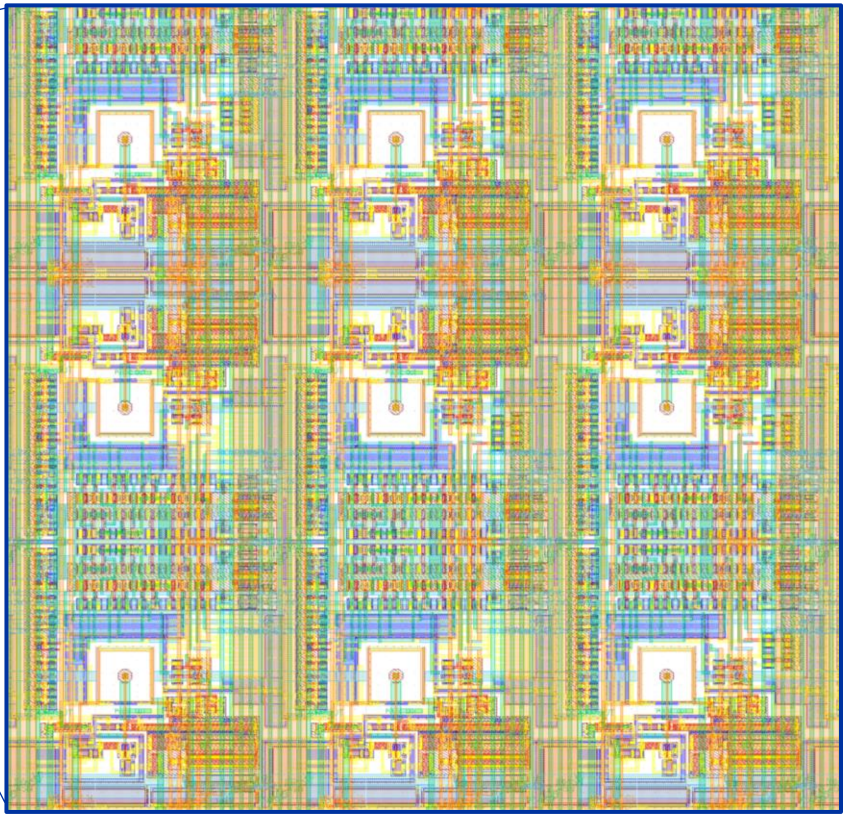


Layout snapshot of a portion of pixel matrix (3x3 pixels)



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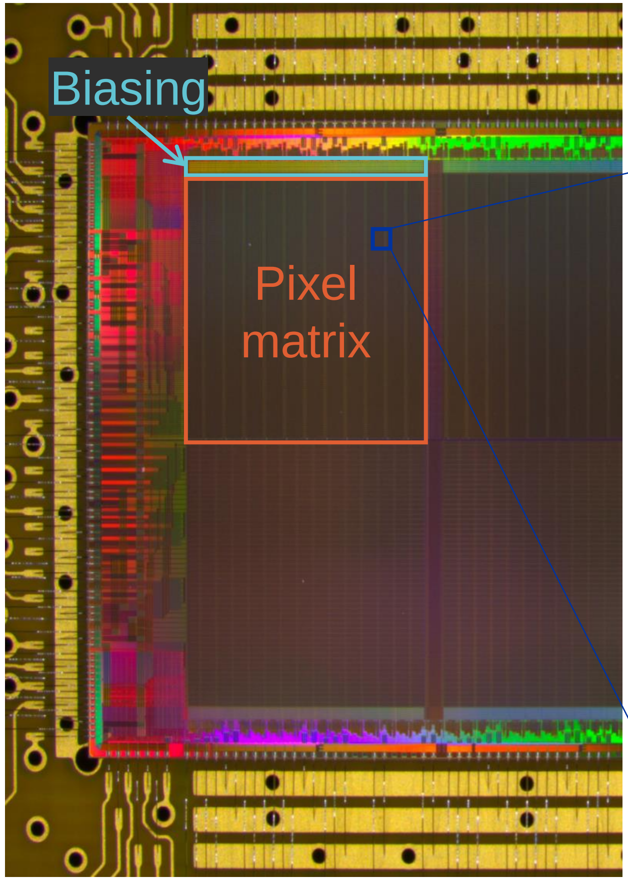

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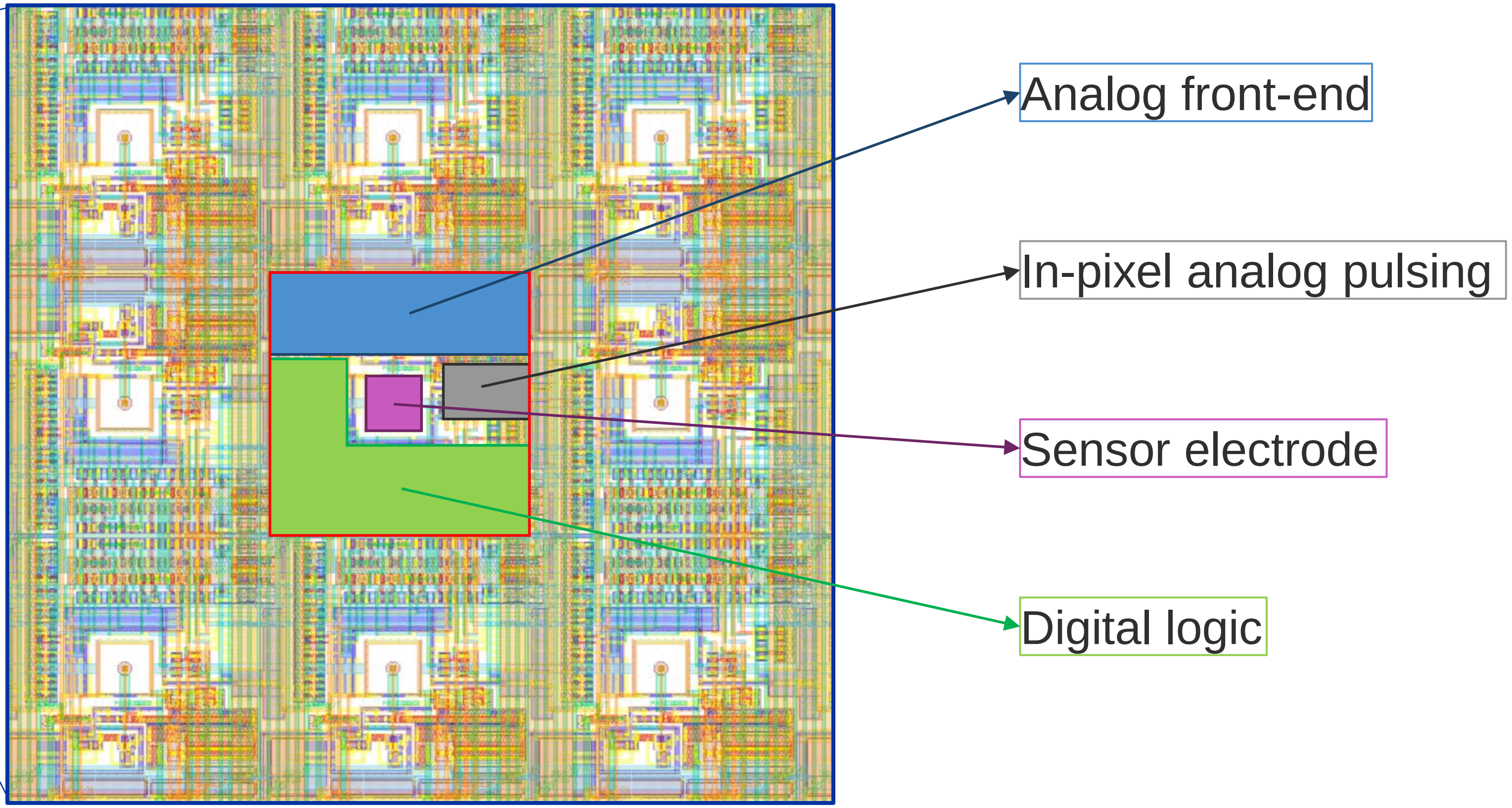

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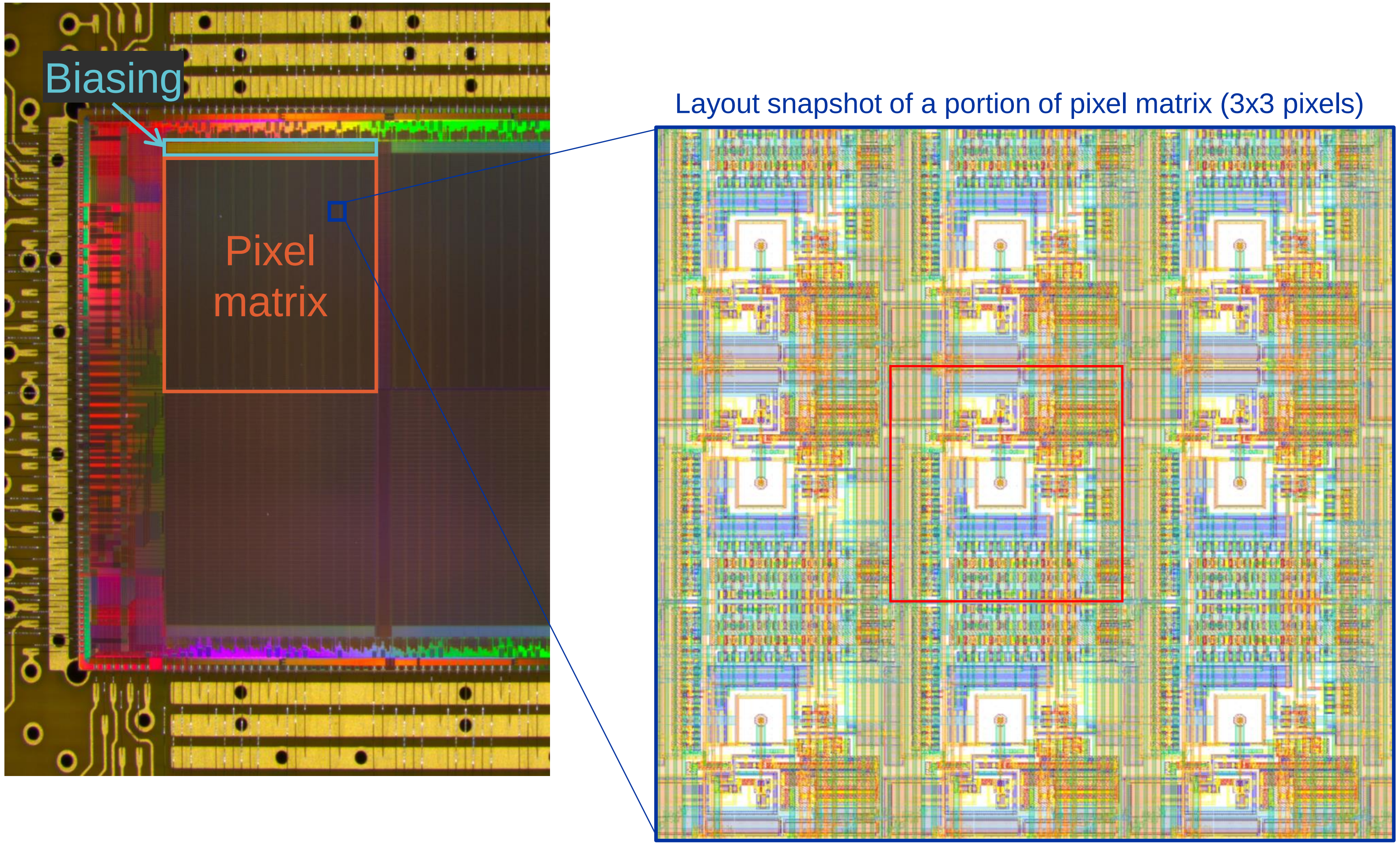
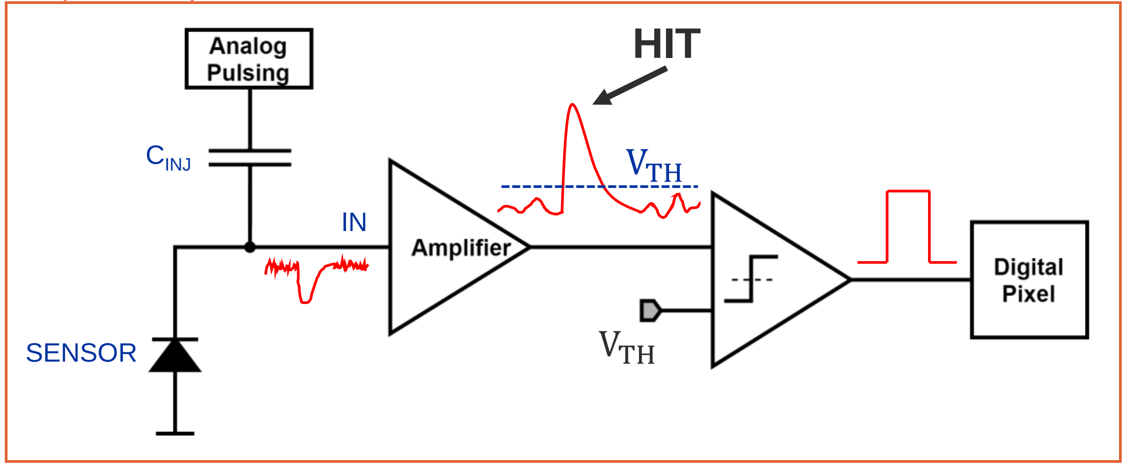


- Sensor electrode shielded up to fourth metal.
- Sensor capacitance few fF (~**1fF** - **5fF**).
- Pulsing circuitry to test analog front-end performance.

Pixel matrix threshold measured with analog pulsing

Simplified in-pixel readout electronics



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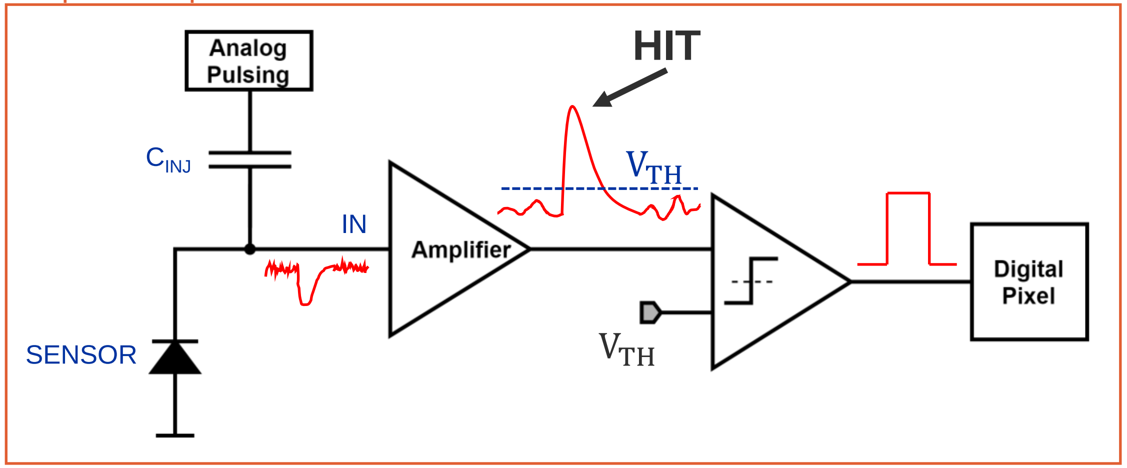

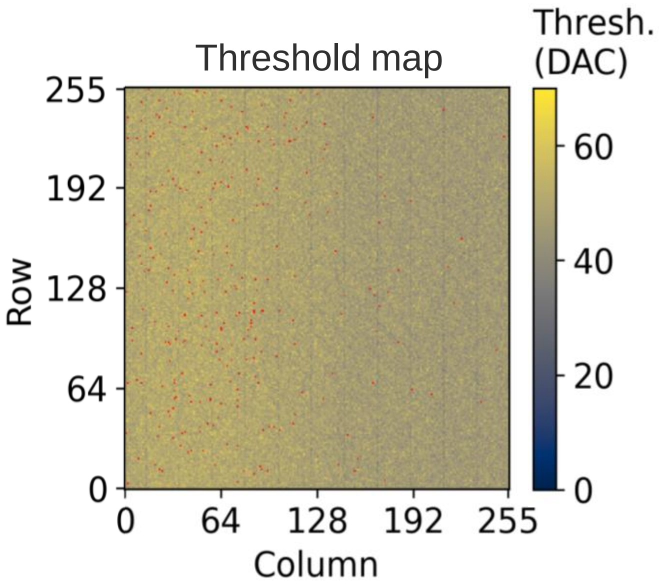

- Sweeping injected charge to measure pixel threshold.
- Threshold map can be plotted.
- Uniform threshold across the matrix is desirable.

Pixel matrix threshold measured with analog pulsing

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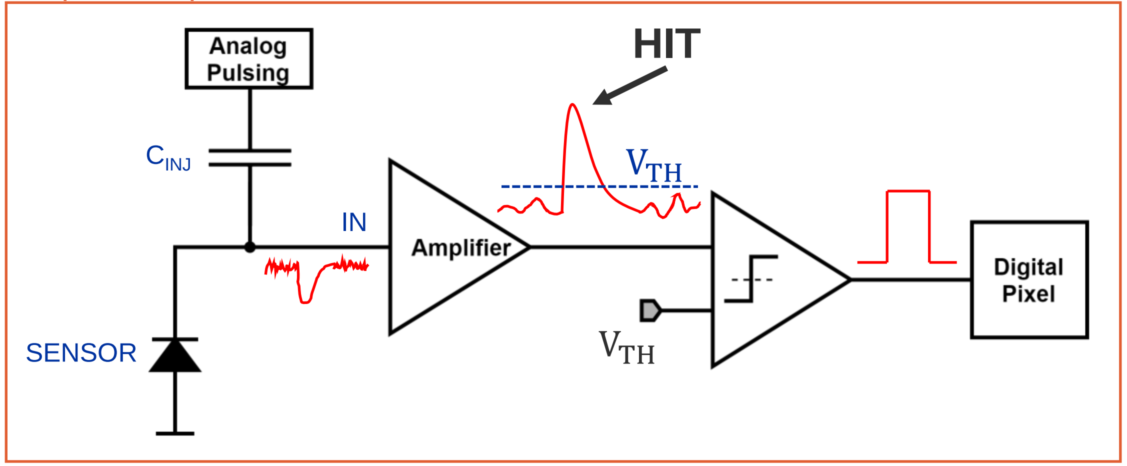

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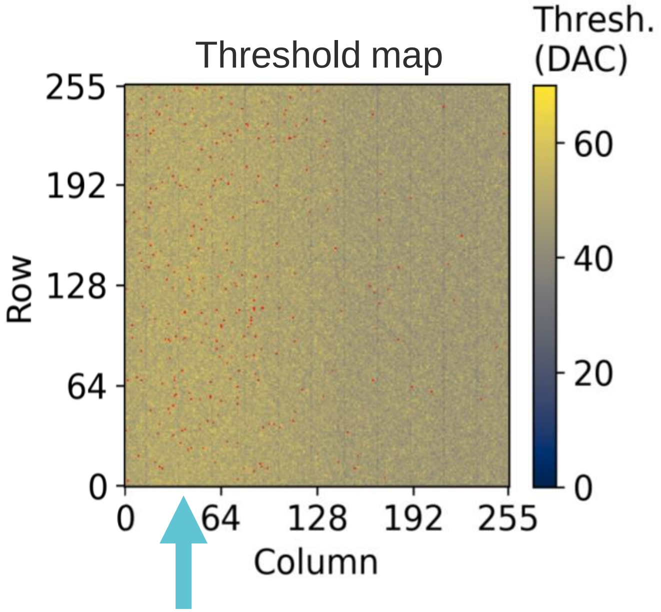

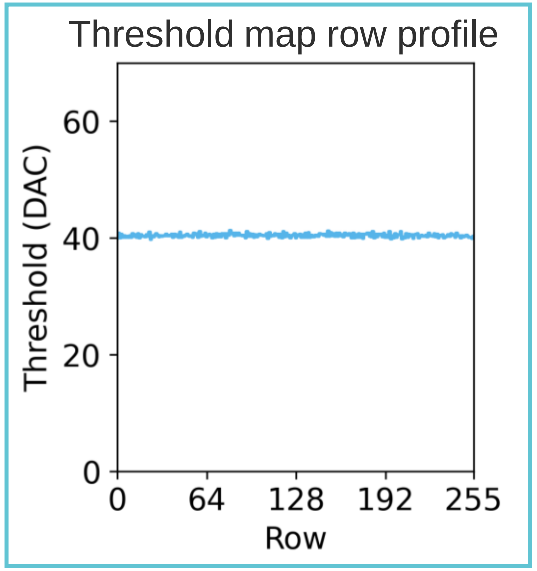

Pixel matrix threshold measured with analog pulsing

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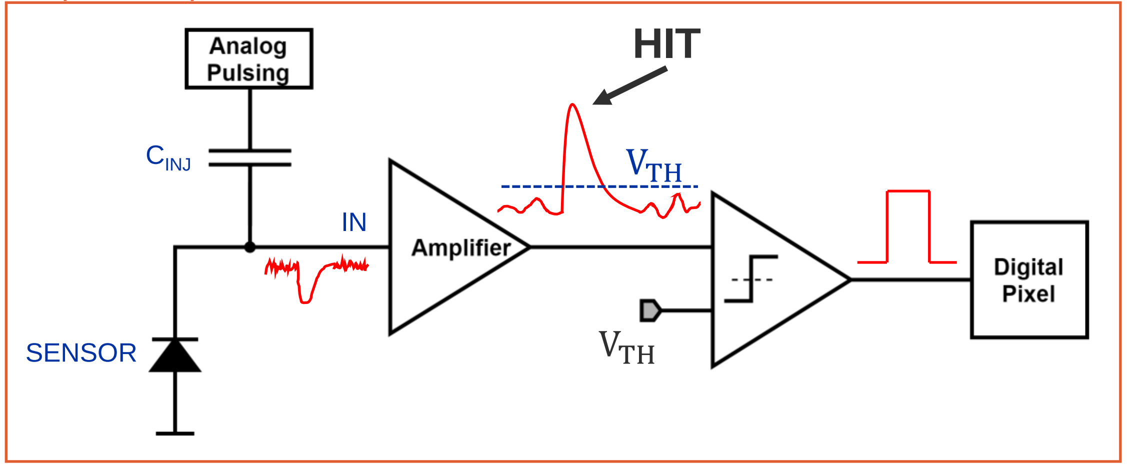

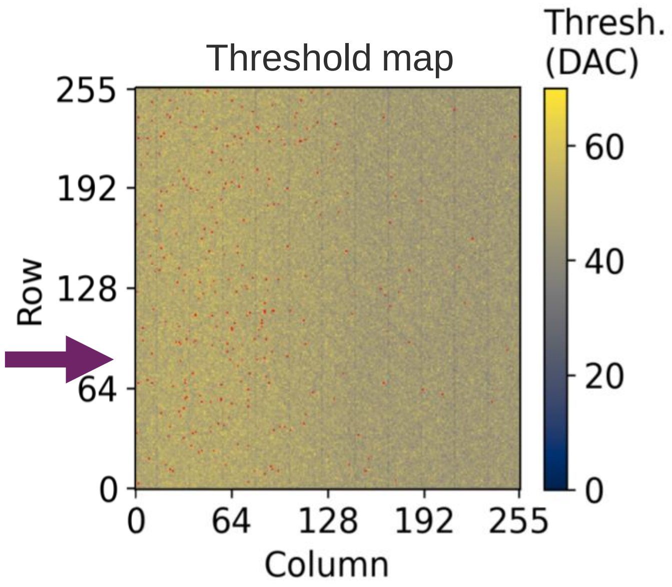

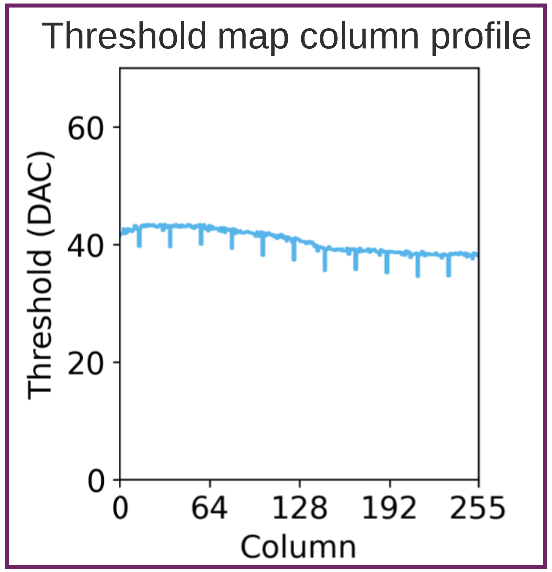

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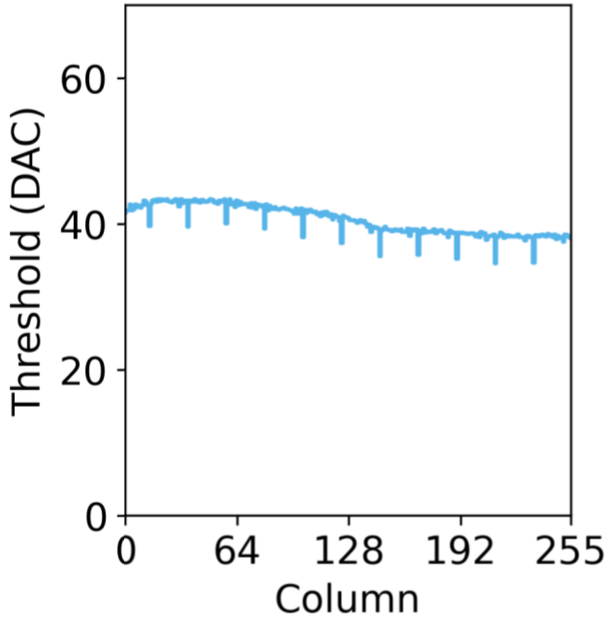
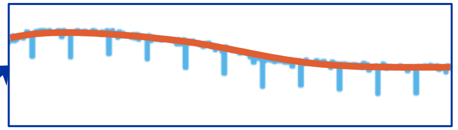
Non-idealities in the threshold column profile

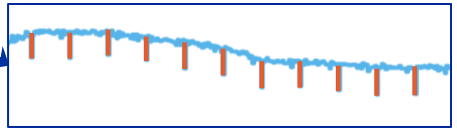


1 DAC code $\cong 4.7\text{mV}$

Two anomalies can be clearly distinguished



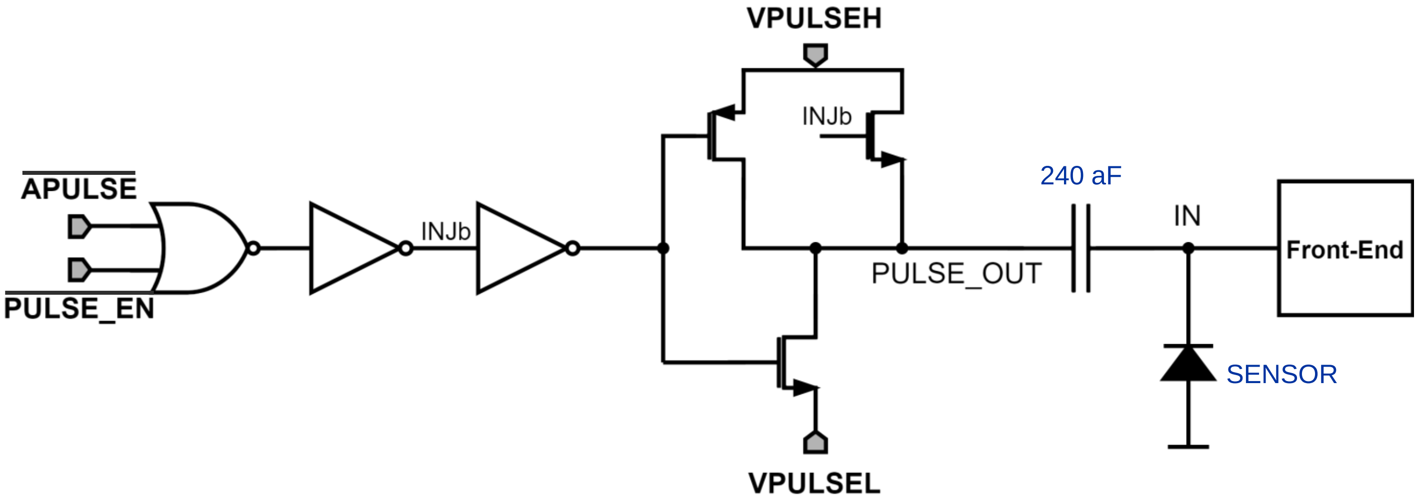
#1 Left to right smooth decrease (~2 DAC codes)

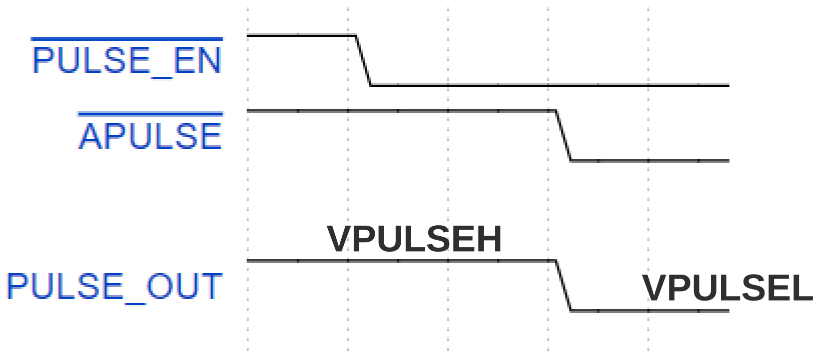


#2 Several downward spikes (~2-3 DAC codes)

Is pixel matrix threshold non-uniform or can these non-idealities be attributed to pulsing circuitry?

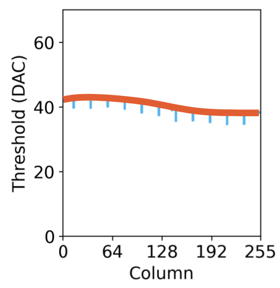
MOSS in-pixel analog pulsing circuitry

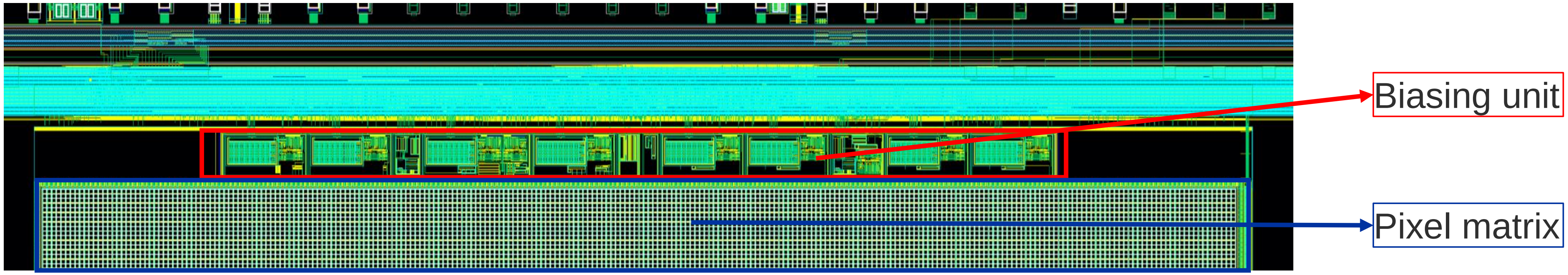




- Two digital signals trigger analog pulsing.
- $Q_{inj} = C_{inj} * (VPULSEH - VPULSEL)$.
- Very small injection capacitance (240aF) to not increase significantly front-end input capacitance.
- **VPULSEH** generated by dedicated DAC in the biasing unit.
- **VPULSEL** connected to VSS in the biasing unit.

#1 Left to right smooth decrease





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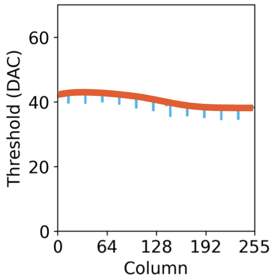
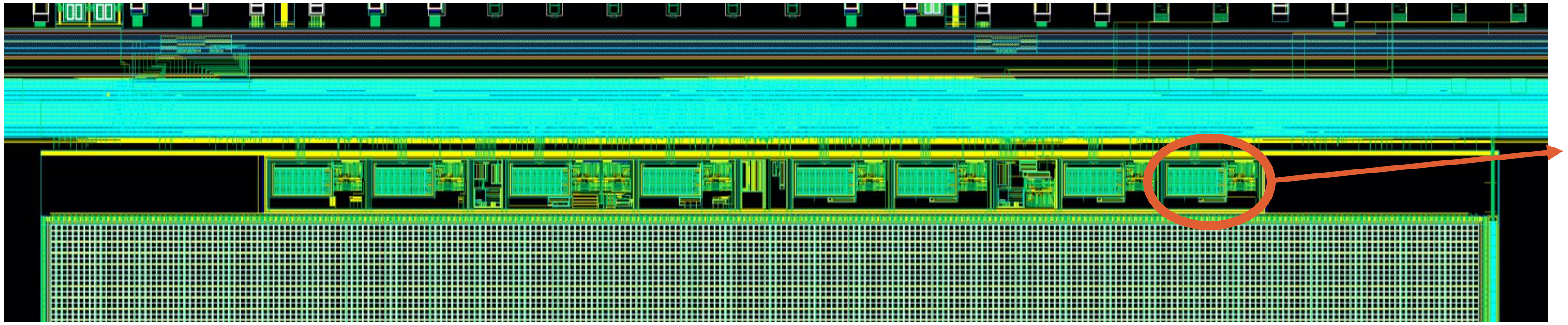
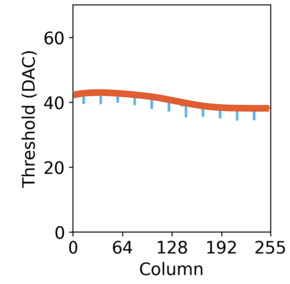
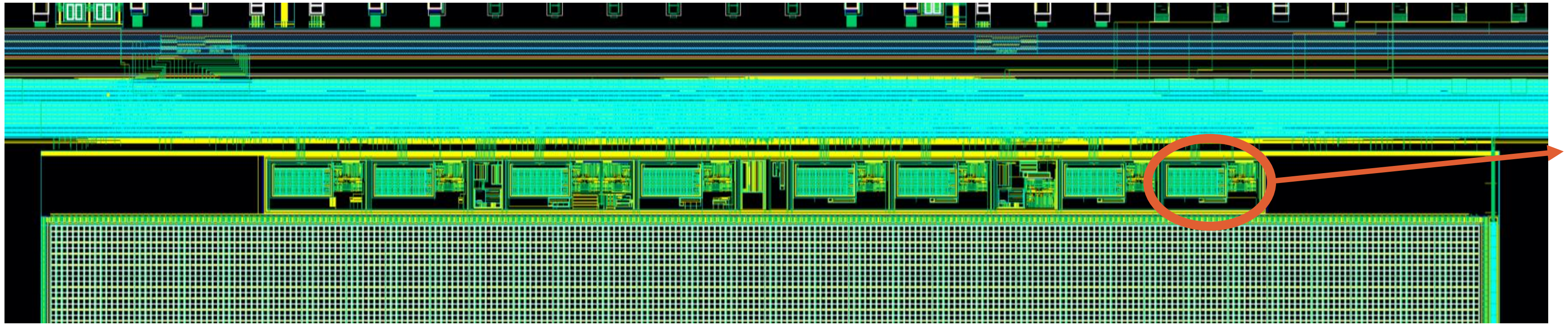




Block generating **VPULSEH** is very off-centred to the right

#1 Left to right smooth decrease





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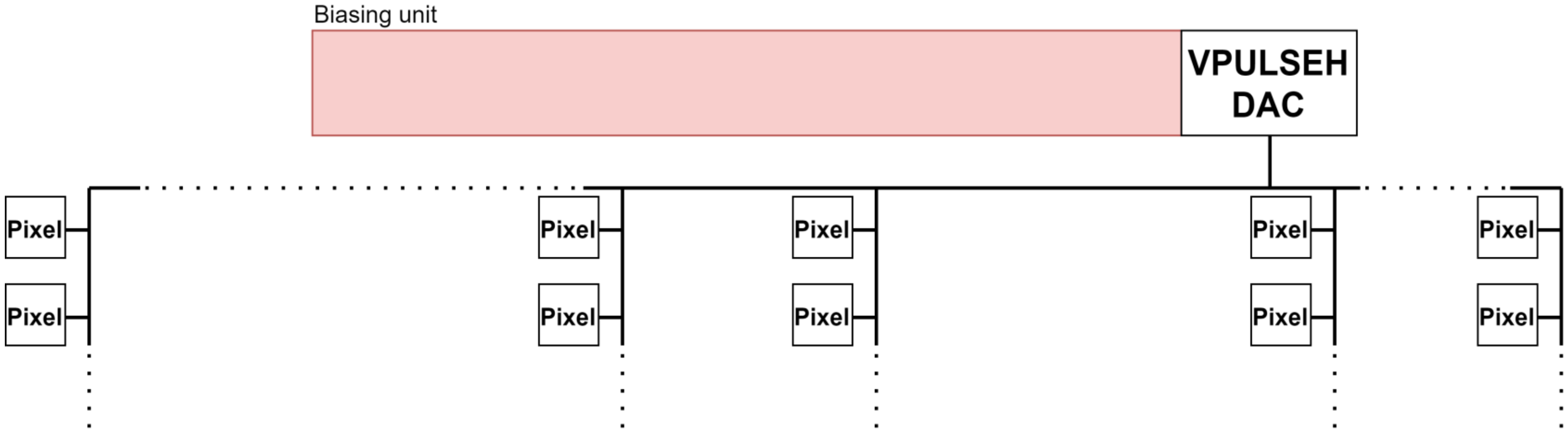
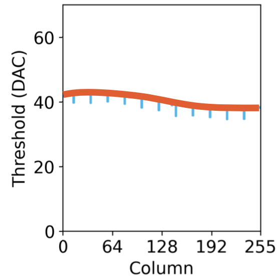


VPULSEH net distribution sketched.
M1 thin horizontal line in common for all columns.

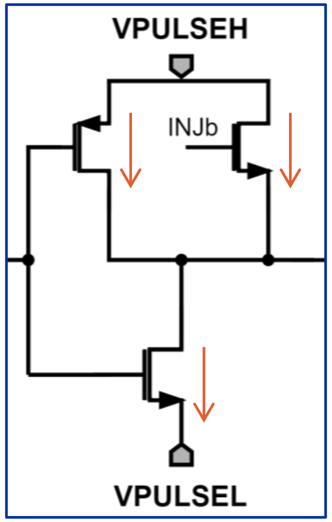
*Illustration not to scale

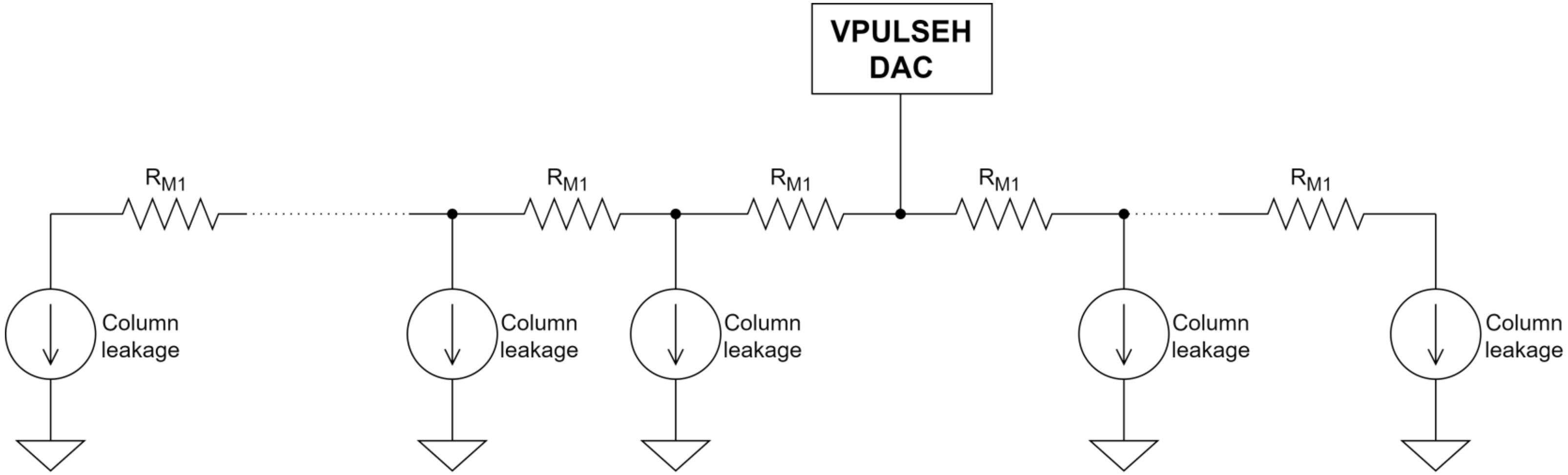
N.B. VPULSEL net follows a very similar path

#1 Left to right smooth decrease



- Leakage on VPULSEH and VPULSEL is sub-threshold leakage.
  - At least 3 orders of magnitude larger than other biases (gate leakage).
- Schematic simulation reproducing VPULSEH and VPULSEL distribution including M1 resistance on horizontal bus.





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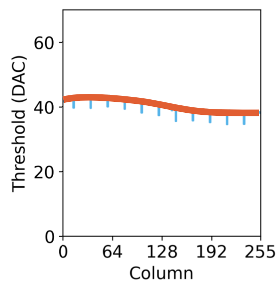
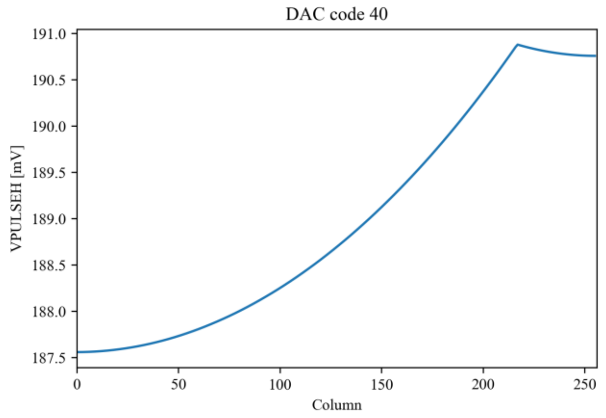
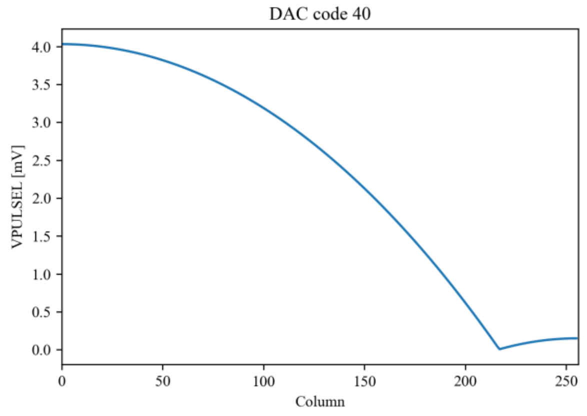
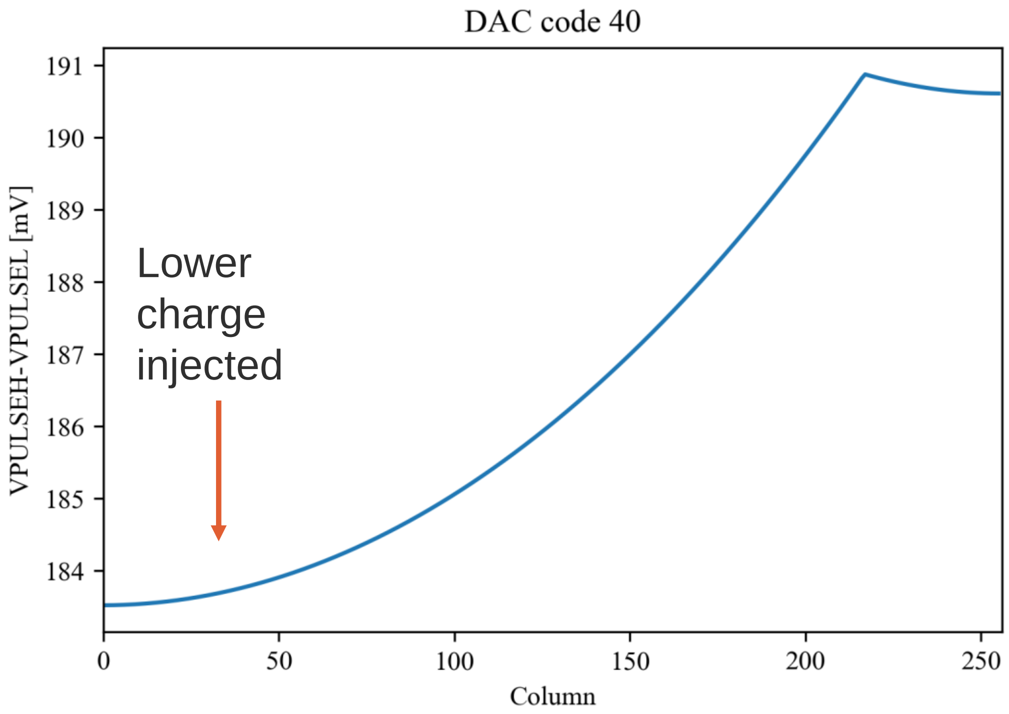


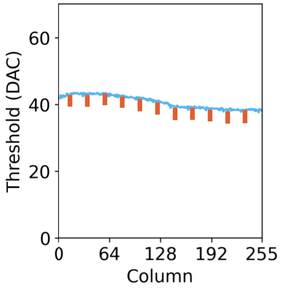




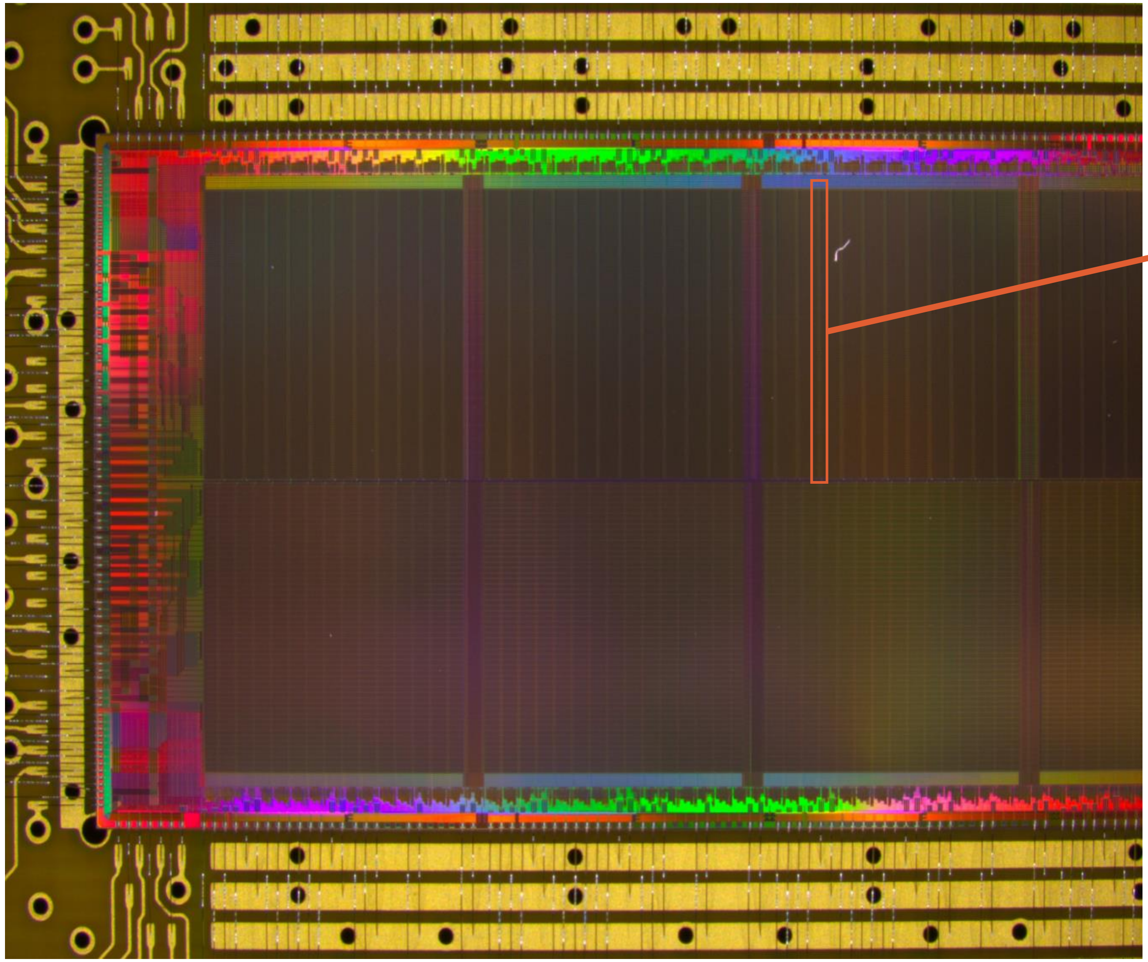


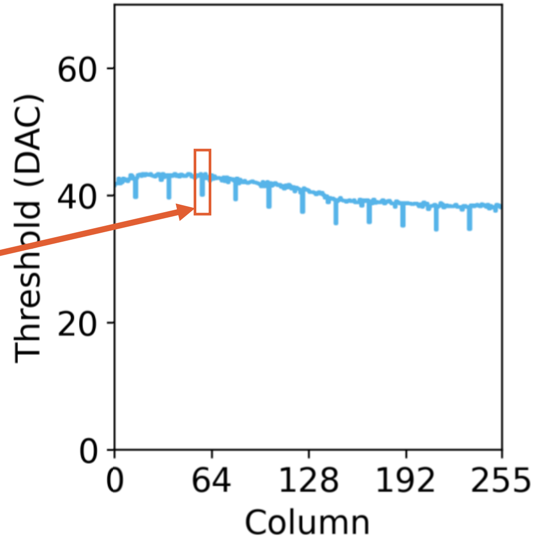
Trend matched!
Lower charge injected results in higher observed threshold

#2 Several downward spikes



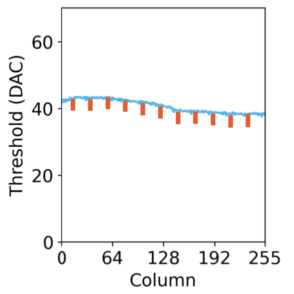
Microscope image of a portion of MOSS



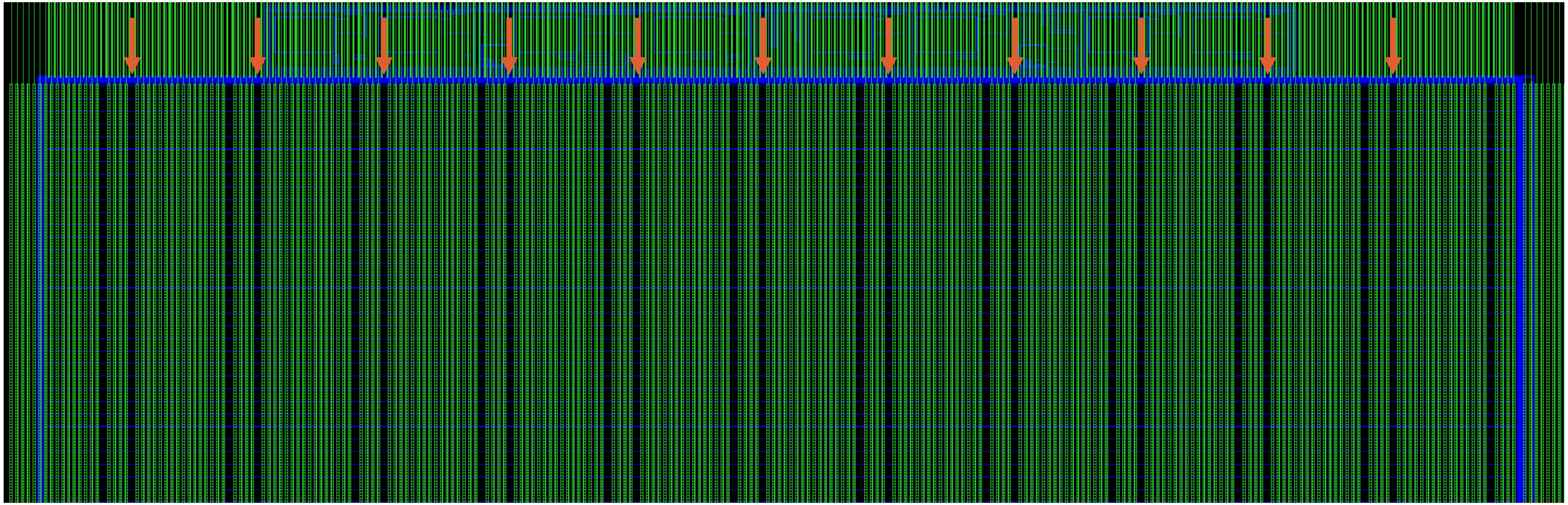


- Visible column pattern on upper metal layers.
- Vertical lines correspond exactly to downward spikes in threshold column profile.
- Correlation is clear but what is the cause?

#2 Several downward spikes

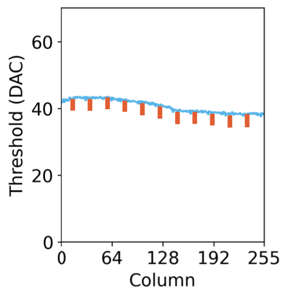


Layout snapshot of M8 (second to last metal) vertical stripes used for power distribution on top of matrix

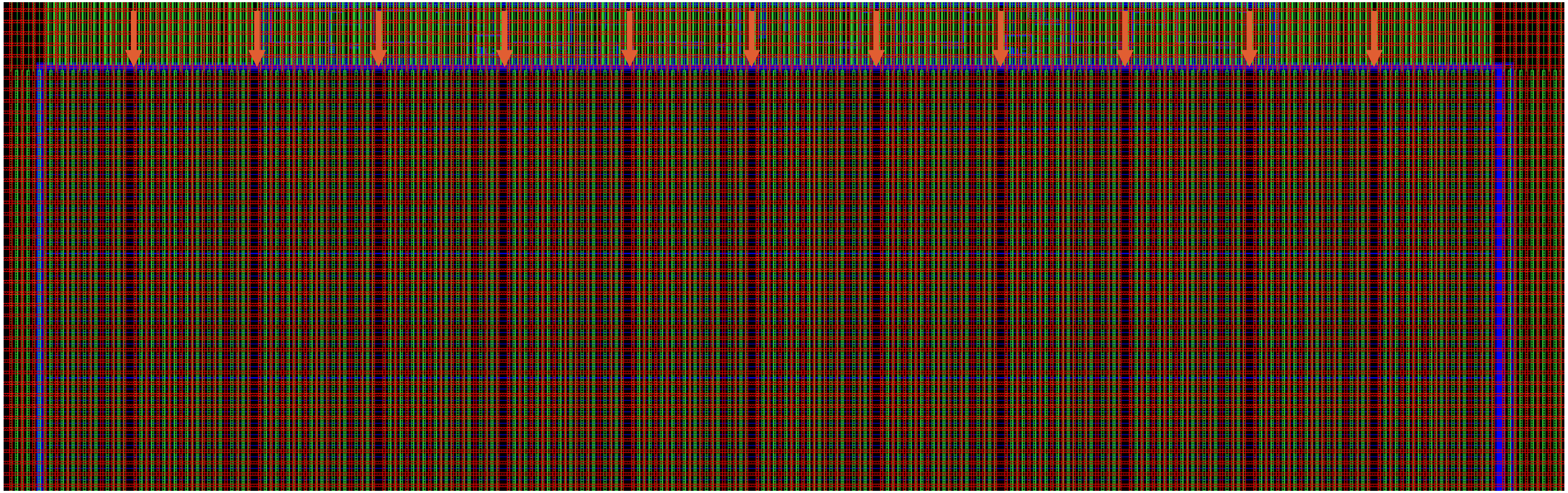


23 empty columns can be identified. 11 of these correspond to downward spikes.

#2 Several downward spikes

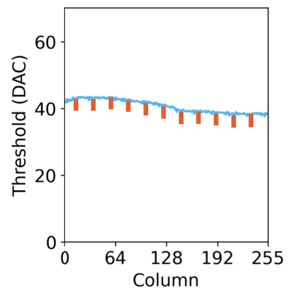


Layout snapshot of M8 and ZA (last metal) power grid on top of matrix

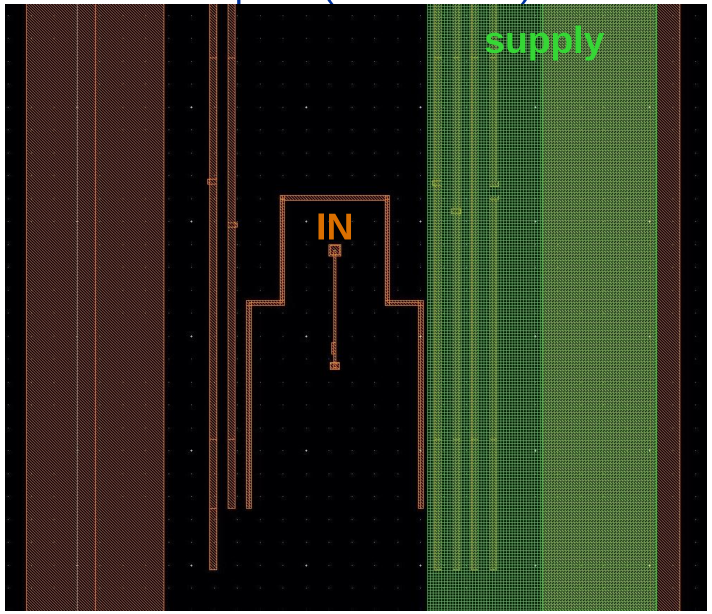


ZA fills some of empty columns. Remaining 11 correspond to downward spikes.

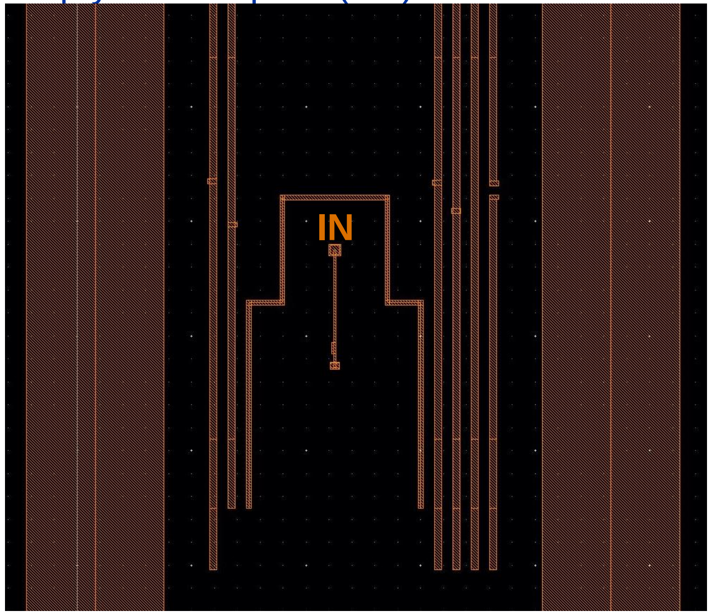
#2 Several downward spikes



Filled column pixel (M4 and M8)

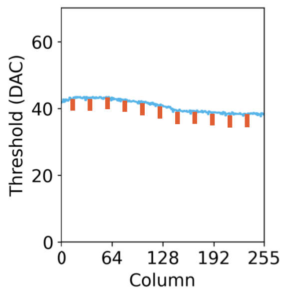


Empty column pixel (M4)

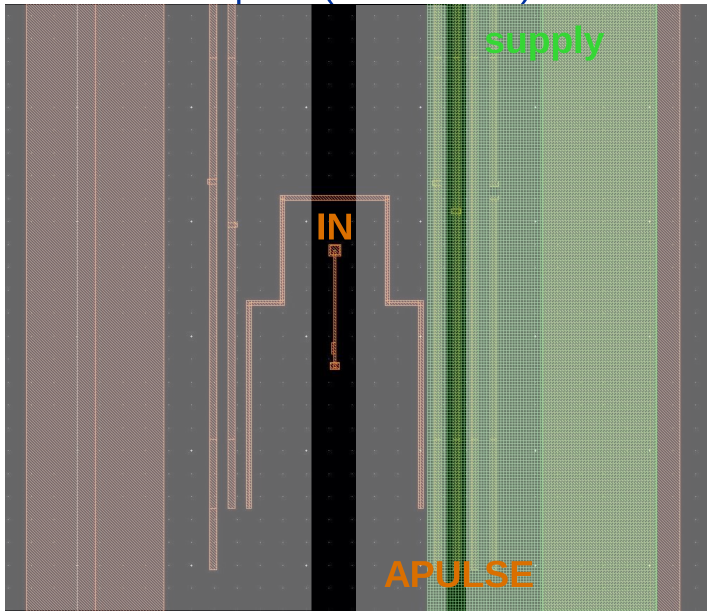


- Two different scenarios:
  - Vertical stripe of top metal (M8 or ZA) is routed on one side of the electrode (filled column).
  - Neither M8 or ZA is drawn on pixel (empty column).
- Parasitics of pixel (analog and digital) are extracted considering the two cases.
- 3D parasitics extractor tool is used for maximum precision.

#2 Several downward spikes



Filled column pixel (M4 and M8)



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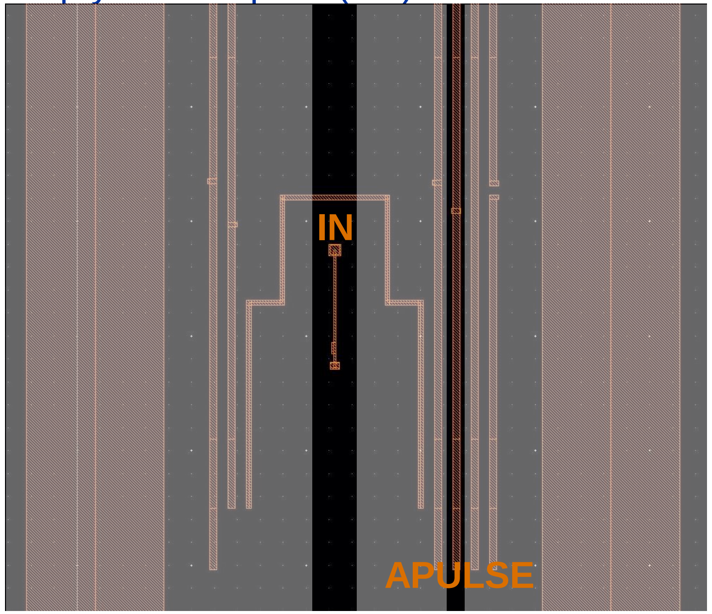
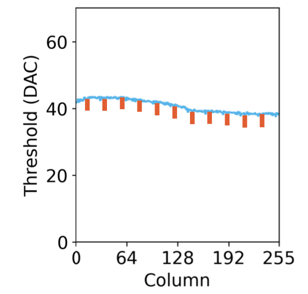


- Pixel without top metals switches at lower pulsing voltage.
- It is found capacitive coupling between **IN** and **APULSE** lines on M4:

#2 Several downward spikes



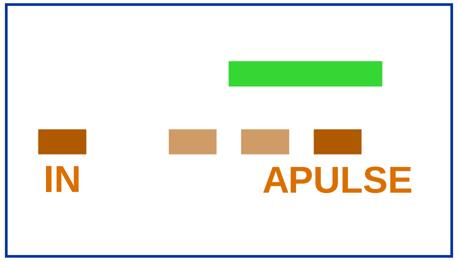
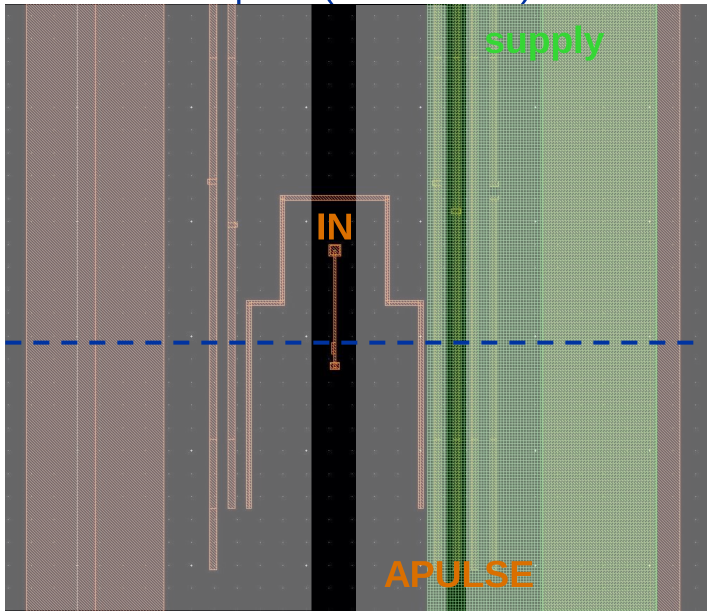
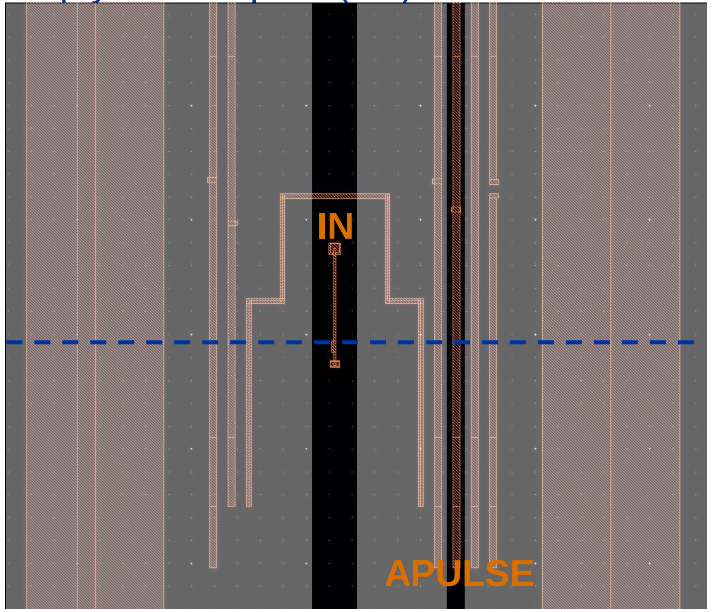


*Illustration not to scale

Filled column pixel (M4 and M8)



Empty column pixel (M4)



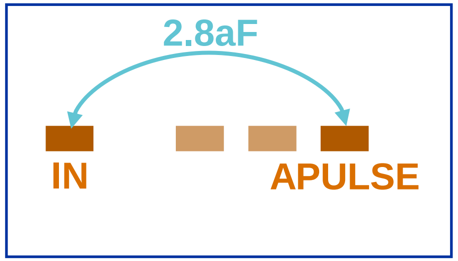
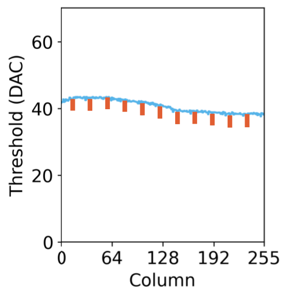


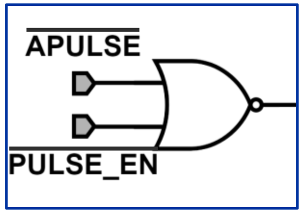
*Illustration not to scale

- Pixel without top metals switches at lower pulsing voltage.
- It is found capacitive coupling between **IN** and **APULSE** lines on M4:
  - 0.2aF with M8/ZA on top that acts as shield.
  - 2.8aF with no metal on top (neither M8 nor ZA).
- **APULSE** is full swing signal (1.2V):
  - Q_{inj} = 2.8aF * 1.2V ≅ 20e- (corresponding to ~2.8 VPULSEH DAC code) unwanted extra injection!

#2 Several downward spikes

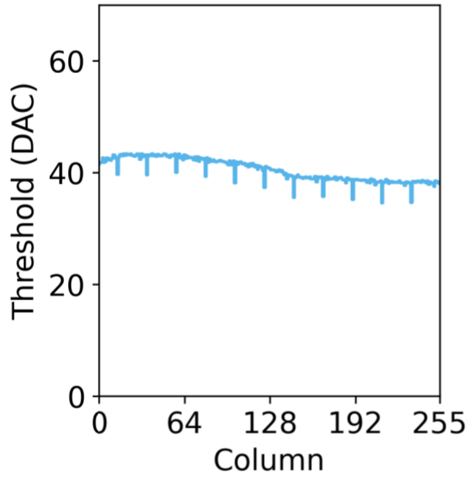


- **Can we believe a ~3aF coupling? Looking for evidence…**
- **APULSE** is coupled with front-end input, but **PULSE_EN** is not.



Standard pulsing procedure

1. **PULSE_EN** is asserted
2. **APULSE** is used to trigger pulsing circuitry



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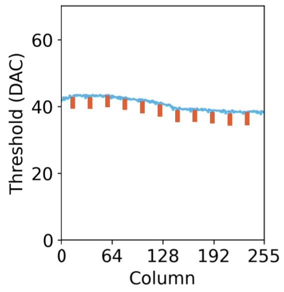

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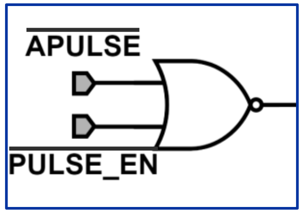

Standard pulsing procedure

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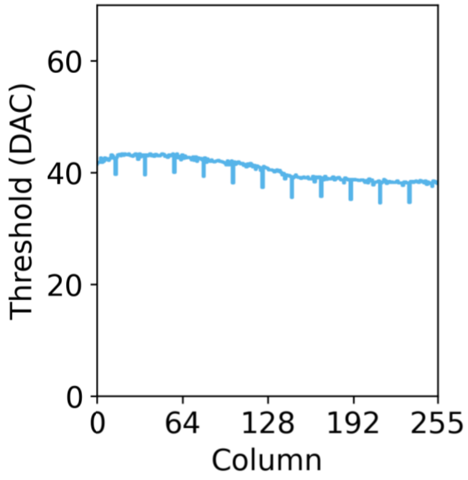
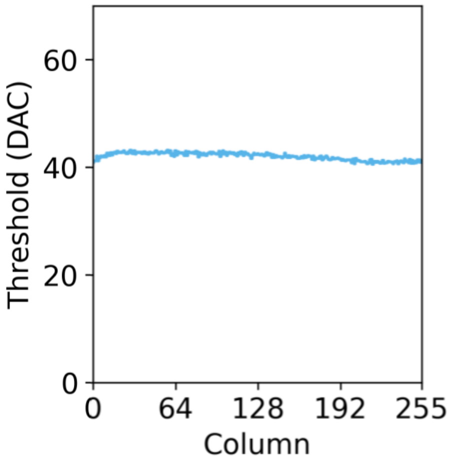


Modified pulsing procedure

1. **APULSE** is asserted
2. **PULSE_EN** is used to trigger pulsing circuitry



Spikes
are gone!

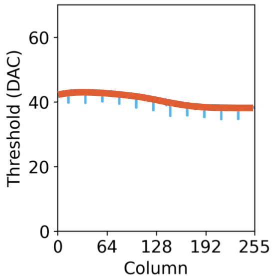
N.B. Detailed implementation uses some tricks to overcome system constraints. Not reproducible on a large scale.

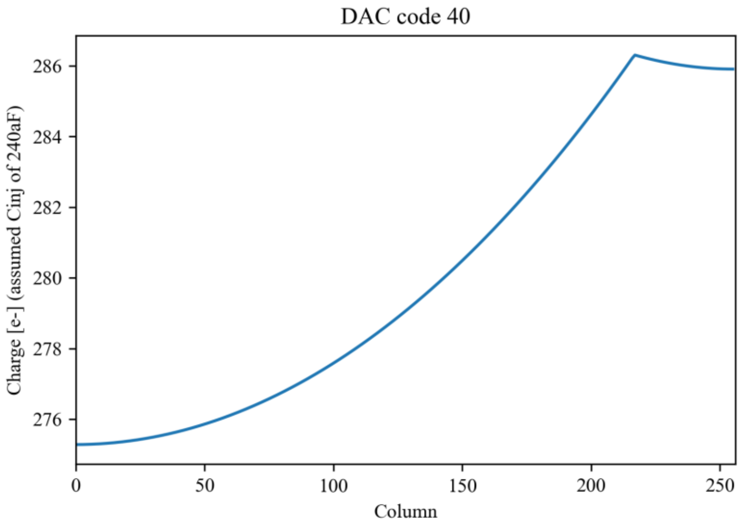
Summary and conclusions

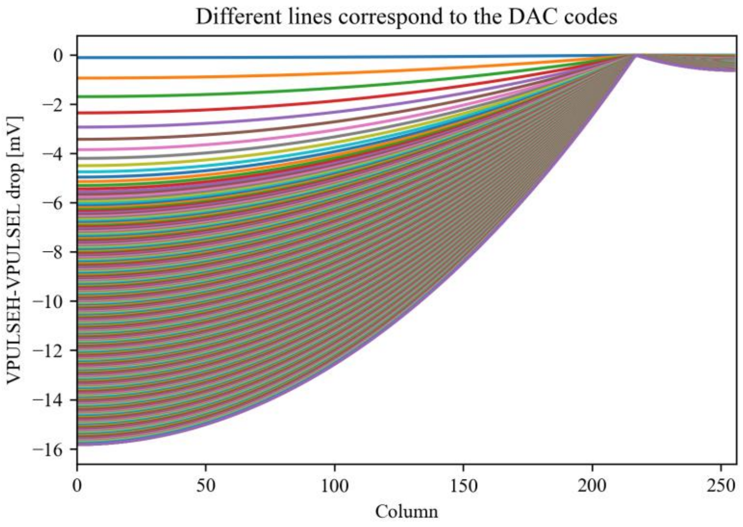
- **MOSS prototype being measured**
  - for feedback for next stitched sensor (MOSAIX)
- **Two non-idealities in threshold map column profile:**
  - Smooth left-to-right trend → sub-threshold leakage on pulsing voltages
  - Several spikes → 3aF coupling between front-end input and pulsing trigger
- **Important learning for the MOSAIX chip:**
  - Pulsing voltages distribution must consider large leakage
  - Small collection electrode MAPS can be sensitive to aF parastitic capacitances
  - Top metals can play pivotal role in shielding digital signals from the sensor electrode
  - Post-layout simulation of pixel required including whole metal stack and considering carefully possible aggressors to analog front-end (using 3D parasitics extractor!)

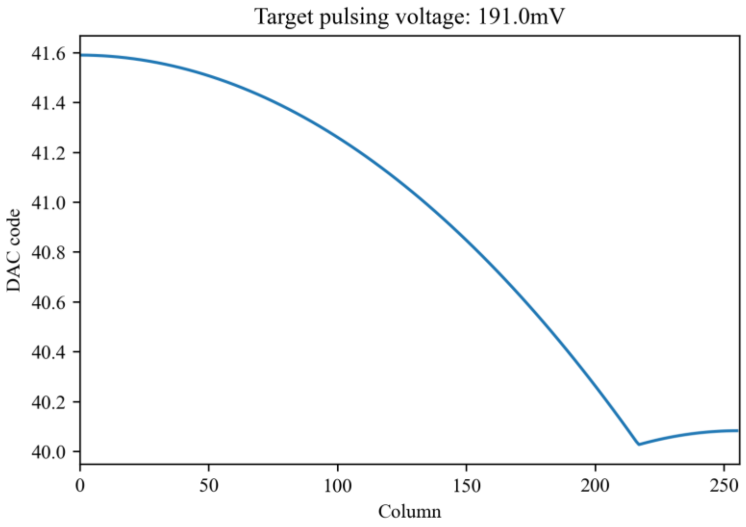
BACK-UP

#1 Left to right smooth decrease



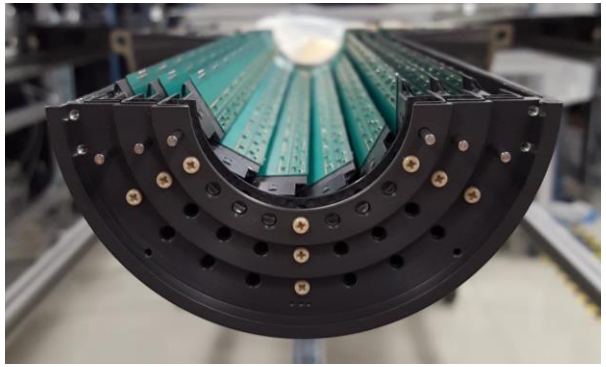






ALICE Inner-Tracker-System upgrade (ITS3)

ITS2 - half barrel



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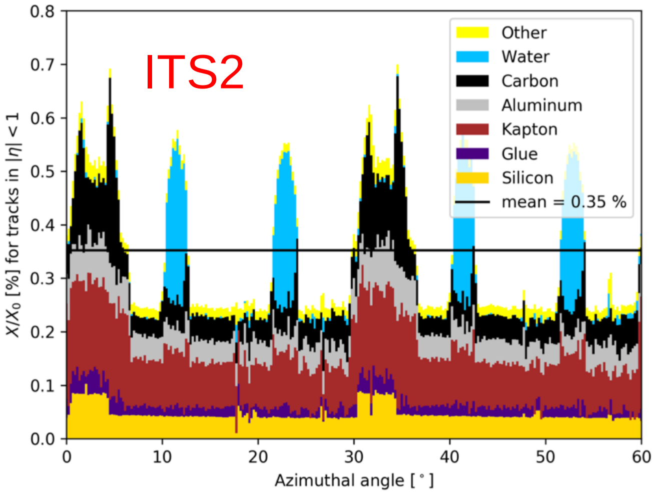
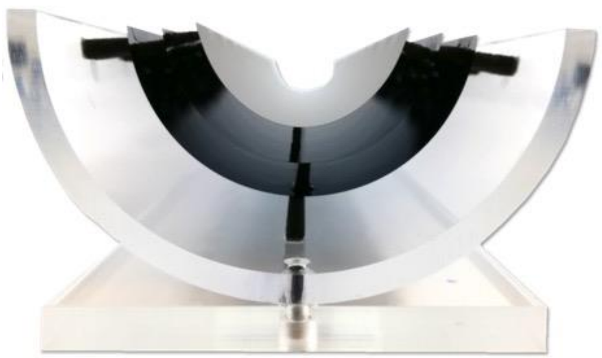


ITS3 - half barrel dummy silicon model



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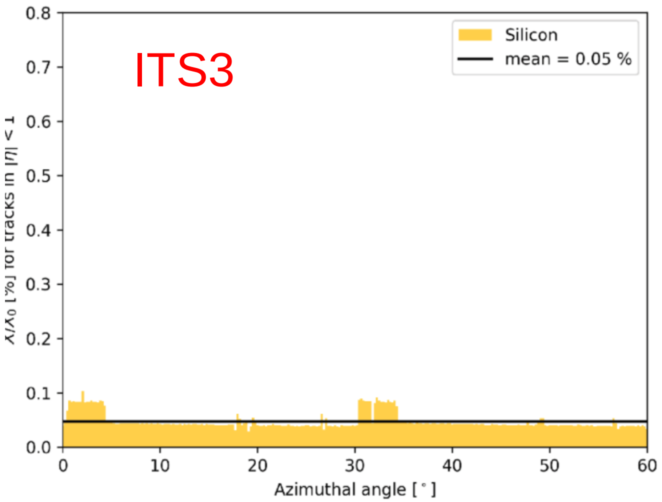


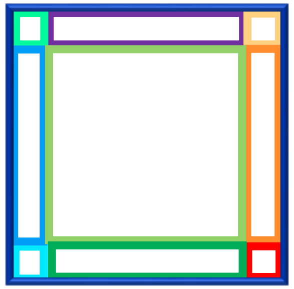
ALICE ITS3 detector:

- wafer-scale stitched sensors (size: $280\ \mathrm{mm} \times 57/75/94\ \mathrm{mm}$).
- thinned down to $< 50\ \mu\mathrm{m}$.
- bent to form truly cylindrical vertex detector.
  → exceptionally low material budget.

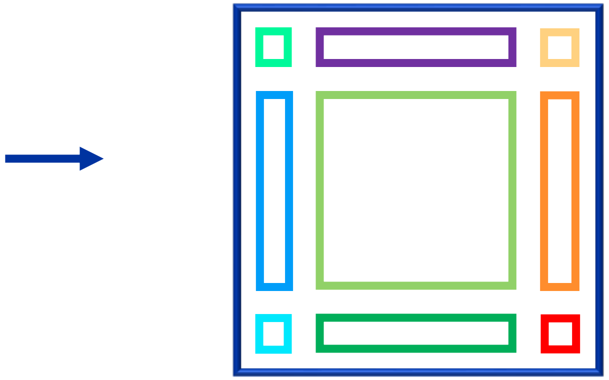
Parameter	Value – ITS2	Value – ITS3
Pixel size	$27\ \mu\mathrm{m} \times 29\ \mu\mathrm{m}$	O($20\ \mu\mathrm{m} \times 20\ \mu\mathrm{m}$)
Silicon thickness	$50\ \mu\mathrm{m}$	$30 - 50\ \mu\mathrm{m}$
Time response	$< 10\ \mu\mathrm{s}$	$< 1\ \mu\mathrm{s}$
Matrix power density	$40\ \mathrm{mW\ cm^{-2}}$	$20\ \mathrm{mW\ cm^{-2}}$
Particle rate	$1.5\ \mathrm{MHz\ cm^{-2}}$	$2.2\ \mathrm{MHz\ cm^{-2}}$
NIEL fluence	$10^{13}\ \mathrm{n_{eq}\ cm^{-2}}$	$10^{13}\ \mathrm{n_{eq}\ cm^{-2}}$
TID	700 Krad	1 Mrad

Stitching technique

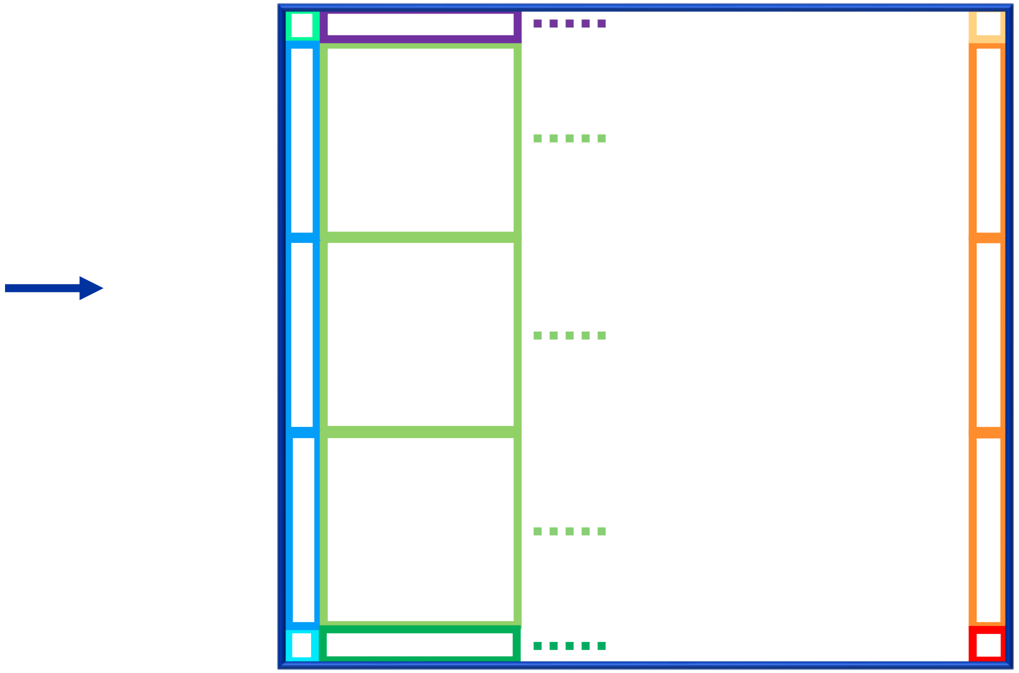
- Chip size is traditionally limited by reticle size (a few cm^2).
- Stitching allows to produce larger chips with the aligned exposures of reticle sub-frames over the wafer.



reticle

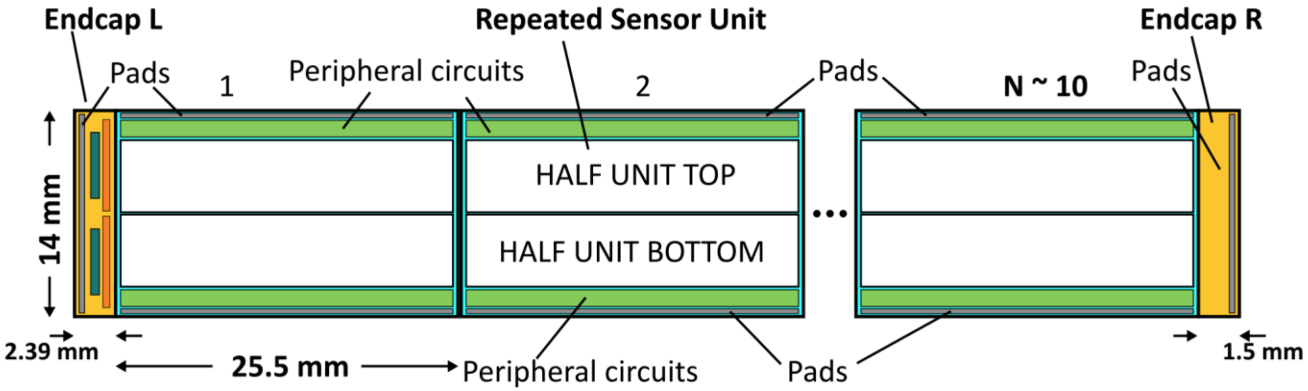


split reticle

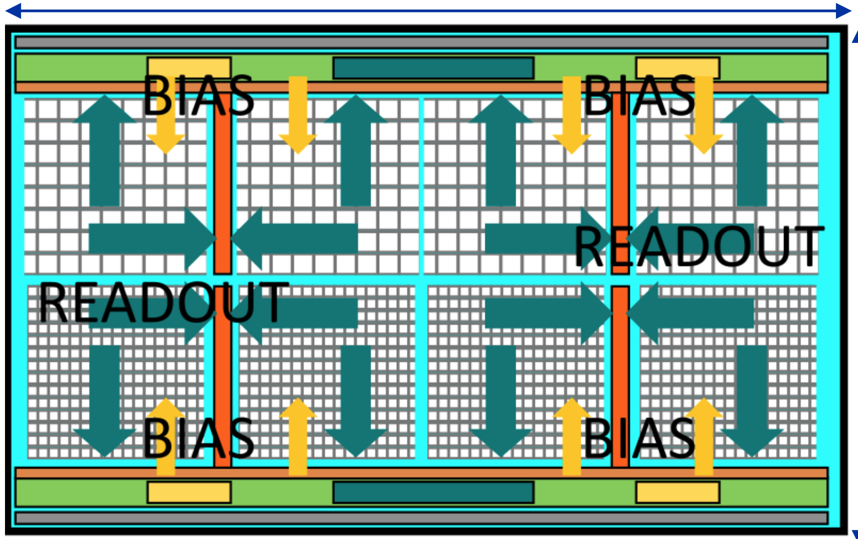


stitched object

Monolithich Stitched Sensor (MOSS) ASIC



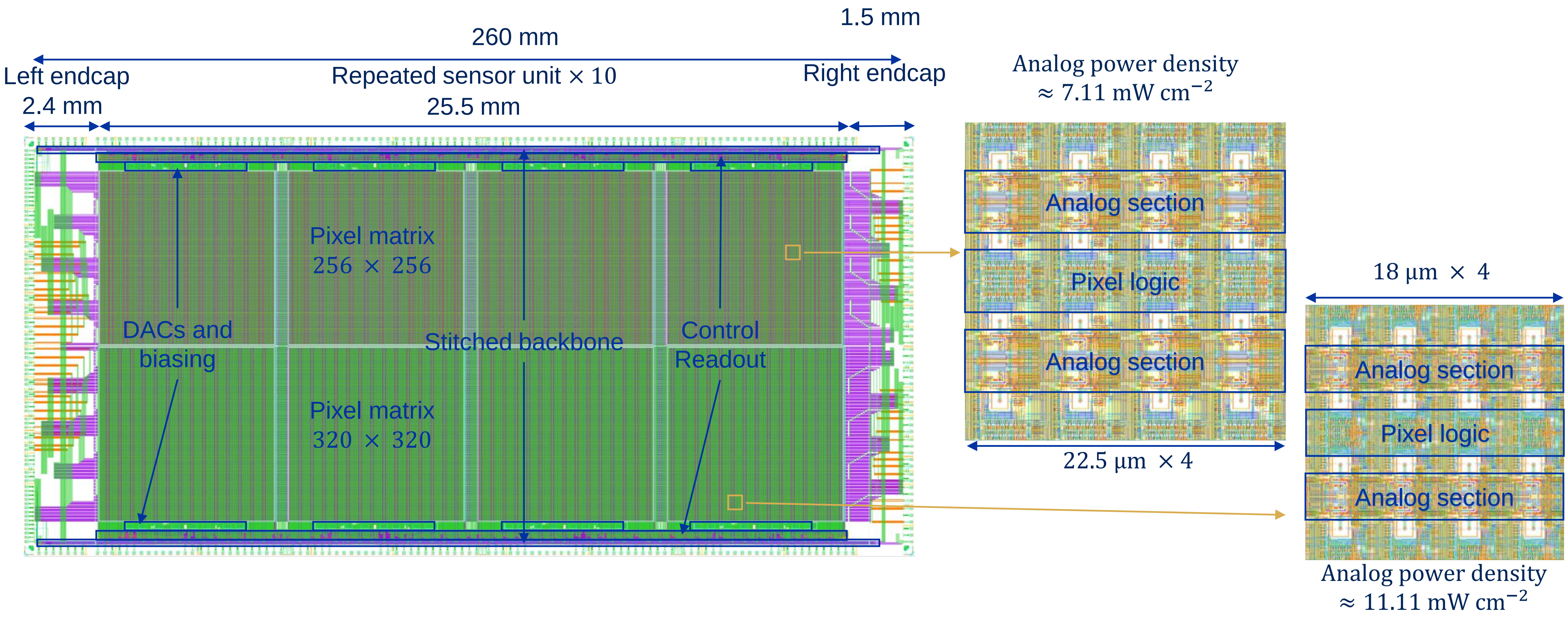
Repeated Sensor Unit (RSU)



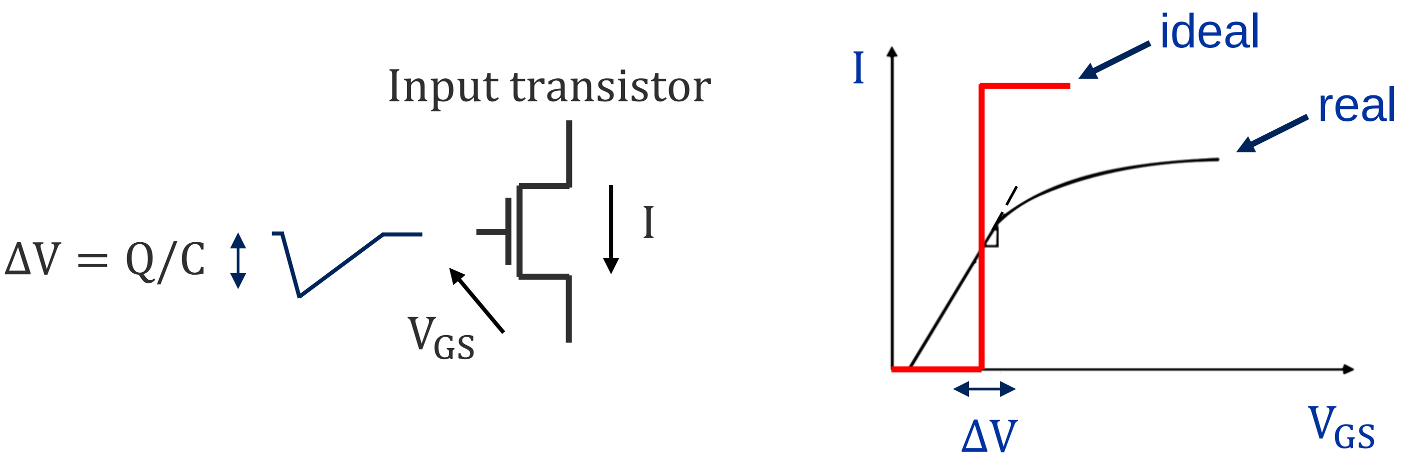
- **4** regions in the **top half** unit
  - Contains array of 256 x 256 pixels with 22.5 um pixel pitch
- **4** regions in the **bottom half** unit
  - Contains array of 320 x 320 pixels with 18 um pixel pitch

Each region has an independent and self-standing biasing unit

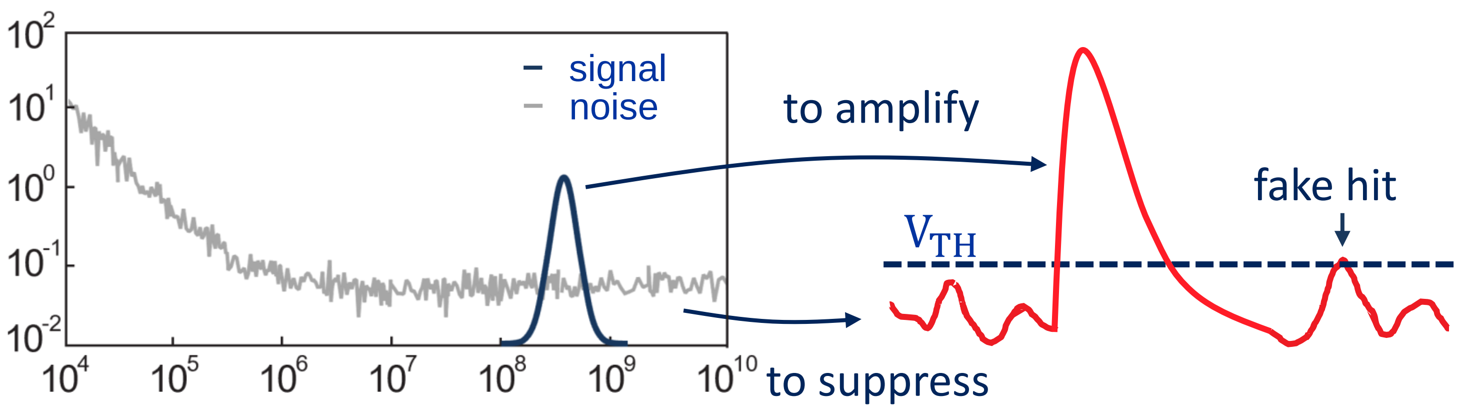
MOSS ASIC Repeated Sensor Unit (RSU)



Signal amplification and discrimination



- Signal needs to be amplified to allow sufficient current output swing.



- Noise is intrinsic in all physical systems.
- Main challenge in microelectronics is to amplify the signal, filtering the noise components with an optimal power budget.

Importance of small sensor capacitance

Input signal → $S = \frac{Q}{C}$

Input noise (dominated typically by the thermal noise of input transistor) → $\sqrt{4K_BT\frac{2}{3}\frac{1}{g_m}}$

$SNR \approx \frac{Q}{C}\sqrt{\frac{3g_m}{8K_BT}} \propto \frac{Q}{C}\sqrt{g_m} \propto \frac{Q}{C}\sqrt[m]{P}$ with $m = 2$ in weak inversion and $m = 4$ in strong inversion.

$P \approx \left(\frac{Q}{C}\right)^{-m}$ with $2 \leq m \leq 4$ depending on the operating point of the input transistor.

→ higher Q/C allows for a lower power consumption for a given SNR and bandwidth.

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