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Investigation of non-idealities of pulsing circuitry in the MOSS monolithic sensor

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The MOSS wafer-scale monolithic sensor, designed for the vertex detector (ITS3) of the ALICE experiment, features a pixel input capacitance of ˜5fF. Such a small input capacitance is needed to reach a satisfactory SNR with a low-power analog front-end (30nW/pixel). This makes the design of the pulsing circuitry needed to characterize the front-end performance particularly challenging. As an example, measurements of the front-end of MOSS are presented, showing that even a parasitic capacitance < 5aF can significantly alter the charge injection from the pulsing circuit. In this contribution, design methods and solutions to address these challenges are detailed.

Summary (500 words)

The MOSS (Monolithic Stitched Sensor) is a prototype monolithic sensor ASIC designed for the upgrade of the three innermost layers of the ALICE Inner Tracking System (ITS3) at CERN. It is designed using a 65nm CMOS imaging technology and exploits the stitching technique, covering an area of 25.9cm x 1.4cm within a single die. Power and data transmission are integrated on chip, allowing the minimization of the detector material budget. One of the consequences is the extremely low power reserved for the analog front-end, in the order of 30nW/pixel. Using a ˜1µm2 collection electrode, the MOSS features a sensor capacitance of ˜5fF. Assuming that the input transistor is in weak inversion and that its current dominates the front-end power consumption, the Signal-to-Noise ratio (SNR) of the front-end is proportional to $Q/C\sqrt{(g\_m)} \propto Q/C\sqrt{P}$, where Q is the collected charge, C is the input capacitance, gm is the transconductance of the input transistor and P is the front-end power consumption. Minimizing C is therefore necessary to maximize the SNR within the allocated power budget. This led to the choice of a ˜5fF sensor capacitance for the MOSS to achieve the target of >99% orthogonal MIP detection efficiency with <0.1pixel-1s-1 fake-hit rate (it can be shown that increasing the SNR reduces the fake-hit rate for a given detection efficiency).

A pulsing circuitry is required to characterize the front end, allowing the injection of a known amount of charge into its input. Such circuitry couples to the front-end input through a capacitor, whose capacitance must be significantly lower than the sensor capacitance not to degrade the SNR. In the case of MOSS, the pulsing capacitance is ˜240aF. This contribution highlights the challenges of designing the pulsing circuit for a monolithic active pixel sensor. To show this, it presents measurement results of the MOSS prototype ASIC and shows examples of non-idealities introduced by the pulsing circuitry in the distribution of the measured charge threshold along the columns of the pixel matrix. Furthermore, it describes the investigation methods and solutions to overcome them.

Two main non-idealities have been identified in the measured charge threshold along the columns of the pixel matrix of the MOSS: a smooth decrease of the threshold from left to right along the matrix; the presence of eleven downward spikes in the threshold distribution along the columns. The first effect is associated to leakage current on the pulsing biasing lines. This has been confirmed by means of schematic simulations. Post-extraction simulation of the pixel revealed the second artefact to be capacitive coupling (˜3aF) between the front-end input and one of the digital lines controlling the pulsing. The extraction of the pixel parasitics is done including all the layers of the process metal stack and employing a high-accuracy parasitics extractor. The 3aF capacitance causes an undesired injection of 20e- at the front-end input. The understanding of these

non-idealities is crucial for the development of the next prototype, and it represents an important lesson for the design of monolithic active pixel sensors with small collection electrodes.

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