Cleopatra : A 12-Channel Recycling Integrator ASIC for the Readout of Hydrogenated Amorphous Silicon Detectors in Radiotherapy Dosimetry

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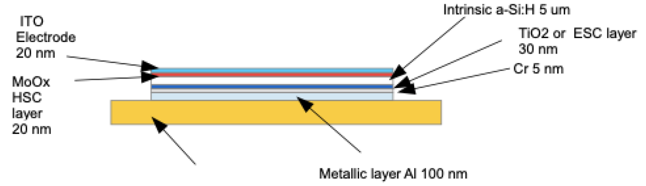
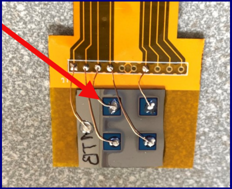
HASPIDE project

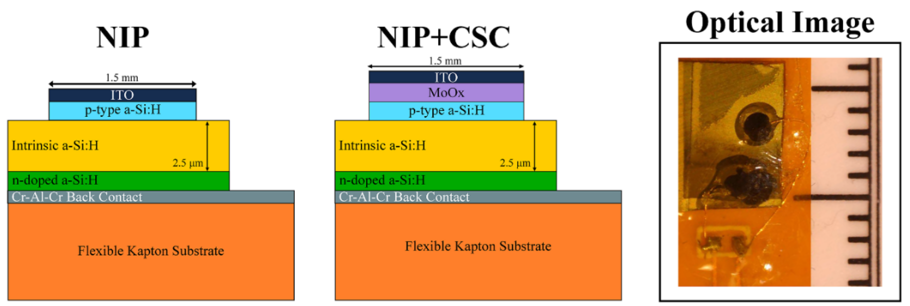
- Development of Hydrogenated amorphous silicon (a-Si:H) detector :
  - Very good radiation hardness
  - Deposition on flexible substrates (Polyimide)
- Possible applications :
  - Beam dosimetry and profile monitoring
  - Neutron detection (Boron deposition)
  - Space application





Beam dosimetry

- Microbeam Radiation Therapy (MRT) and FLASH therapy both show improved treatment efficacy and radiobiological effectiveness of X-ray therapy
- Key point : peak-to-valley dose ratio, radiation tolerance



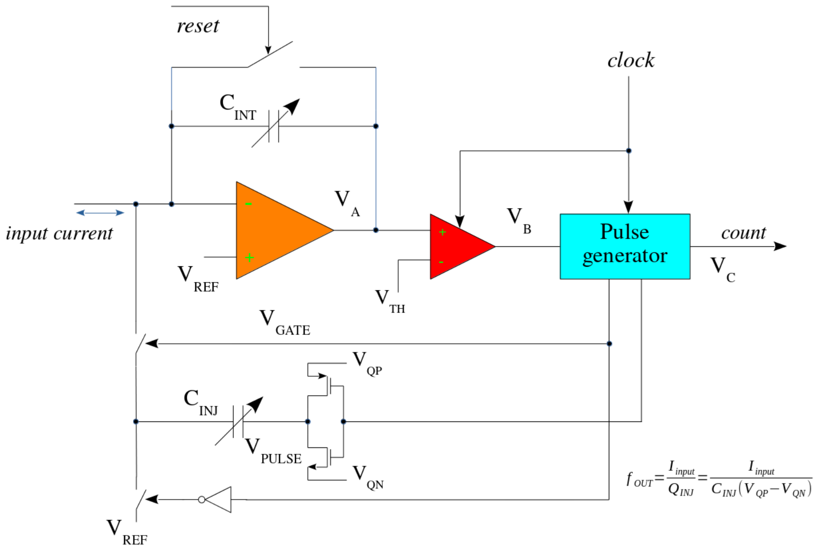
M.Large et al.,
Dosimetry of microbeam radiotherapy by flexible hydrogenated amorphous silicon detectors,

2024 Phys. Med. Biol. 69 155022

Architecture for beam dosimetry and monitor requirements

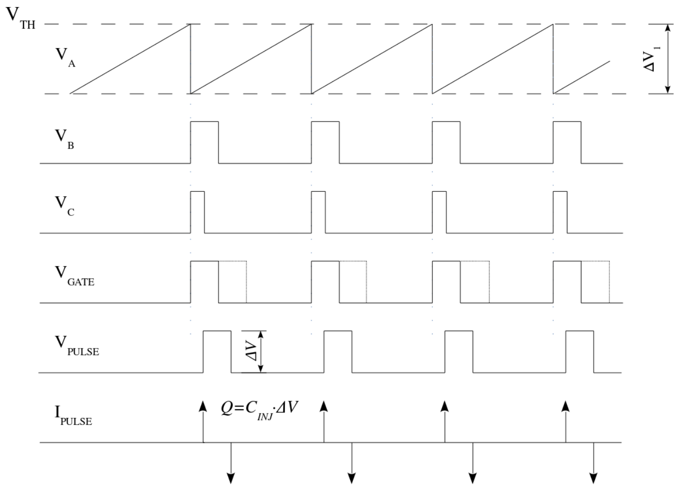
- Requirements
  - Input resistance $\leq$1 kΩ
  - Input capacitance 1$\div$50 pF
  - Input current 100 pA$\div$2 μA
  - Readout time from 400 μs down to 60 ns
- Selected architecture
  - I$\rightarrow$f converter followed by U/D counter
  - Based on the recycling integration principle (for large dynamic range)
  - Technology CMOS 28 nm
    - Small parasitic capacitance
    - High max frequency
    - Radiation tolerance
    - Key element : input opamp
  - Max clock frequency *(simulated)* : 640 MHz
  - 12-channel prototype for evaluation

Channel architecture



$$f_{OUT} = \frac{I_{input}}{Q_{INJ}} = \frac{I_{input}}{C_{INJ}(V_{QP} - V_{QN})}$$

Subtraction principle



$$f_{OUT} = \frac{I_{IN}}{C_{INJ}\Delta V}$$

$$\Delta V = (V_{QP} - V_{QM})$$

$$f_{MAX} = \frac{f_{CLK}}{4}$$

$$I_{MAX} = \frac{f_{CLK}}{4} C_{INJ}\Delta V$$

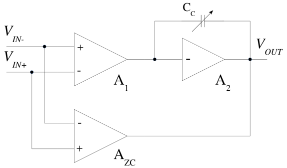
- *no 1st order dependence on* V_{REF}, V_{TH}
- *digitally controlled polarity*

Design of the integrating stage

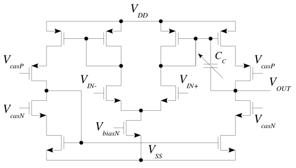
Three different OTA configuration have been designed :

- Two stage OTA with active feed-forward compensation (FF)
- Current-mirror topology with cascoded output (CM)
- Current-mirror topology with active gain boots (CMB)

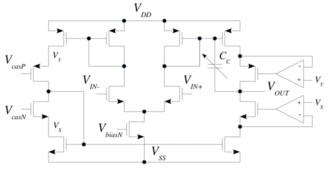
Trade off between bandwidth (maximum conversion frequency) and gain (detector capacitance)



(FF)

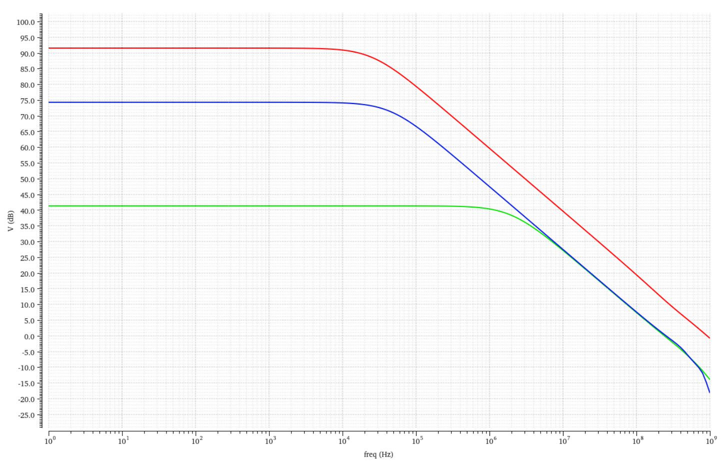


(CM)



(CMB)

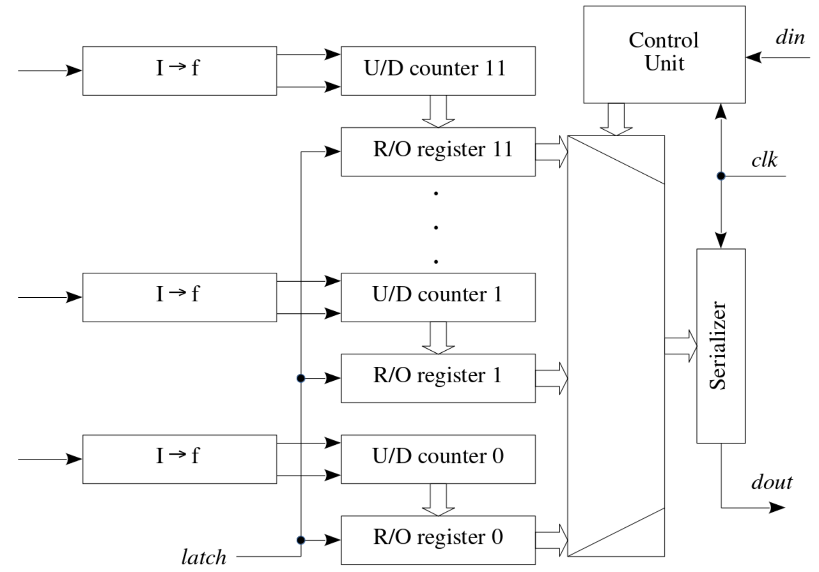
OTA bandwidth



- Power(FF) : 100 μW
- Power(CM) : 30 μW
- Power(CMB) : 90 μW

- GBW(FF) : 900 MHz
- GBW(CM) : 240 MHz
- GBW(CMB) : 260 MHz

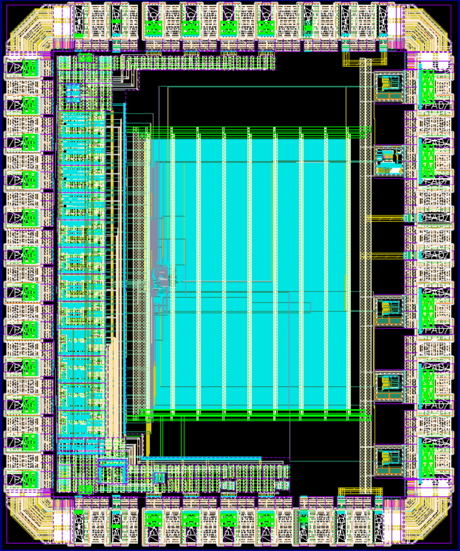
Cleopatra architecture

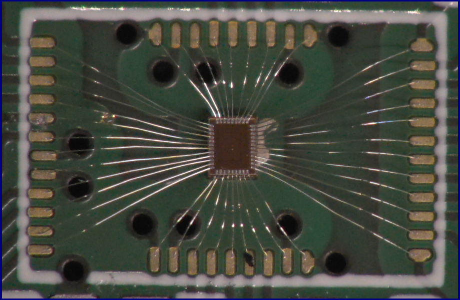


Digital interface

- pseudo SLVS based, fully differential
- Signals
  - Reset$\pm$ (synchronous), clock$\pm$
  - Latch$\pm$: store all counter values into registers
  - Din$\pm$, Dout$\pm$: serial interface working at half clock frequency
  - Address$<6:0>$: chip address, internally hardwired in the prototype
- Seven configuration registers :
  - Addressed via custom serial protocol
  - Integration and compensation capacitance selection
  - Injection capacitance selection
  - Polarity selection
  - Data/control register readout selection

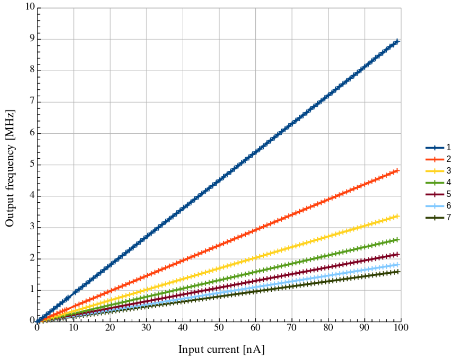
Cleopatra layout

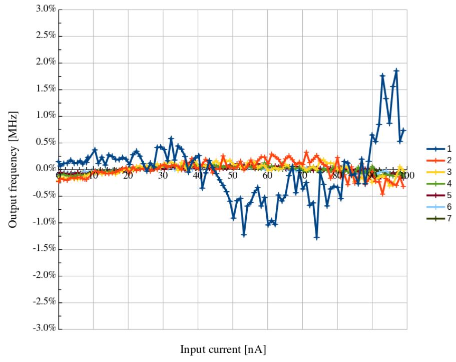




- Technology : CMOS 28 nm
- Die size : 1.1×1.3 mm^2
- SLVS interface
- Clock frequency up to 640 MHz
- Pad limited

Linearity vs injection setting - 1

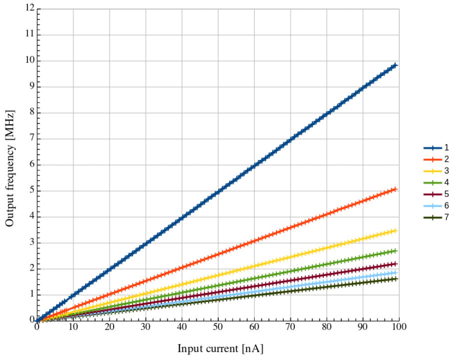




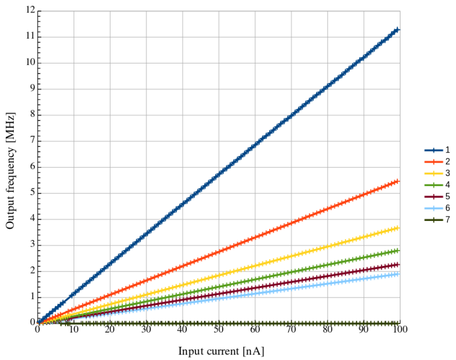
- Injection capacitance : N×20 fF
- Injection voltage : 600 mV
- Clock frequency : 500 MHz

Linearity vs injection setting - 2

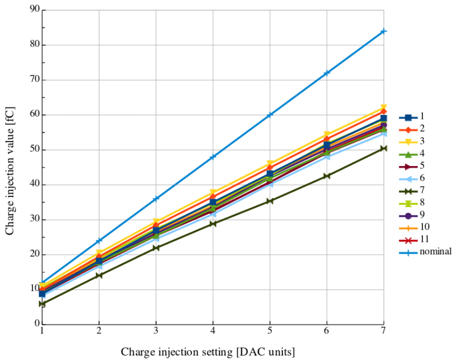
Polarity = 0

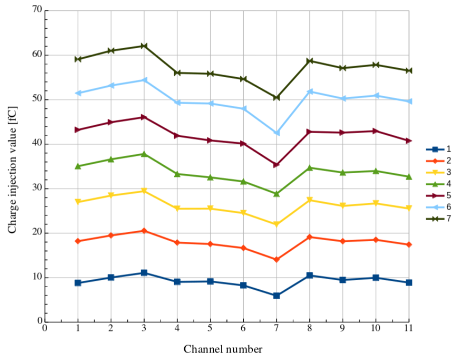


Polarity = 1



Charge quantum measurement - polarity 0

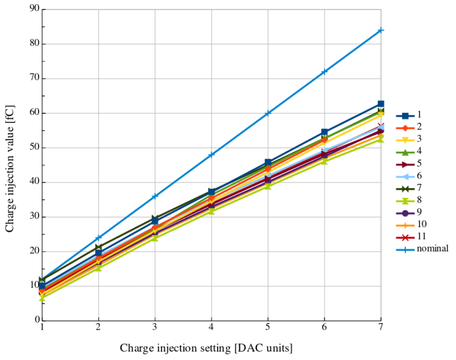


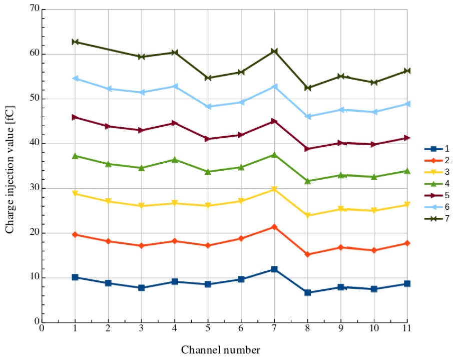


- Slope*(nom)* : 12 fC/DAC code
- Slope*(meas)* : 8.02 fC/DAC code

- CMB : channels 11-8
- CM : channels 7-4
- FF : channels 3-0

Charge quantum measurement - polarity 1



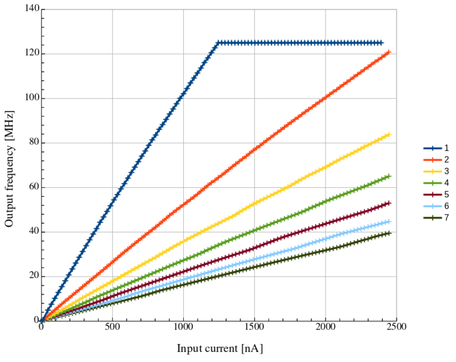


- Slope*(nom)* : 12 fC/DAC code
- Slope*(meas)* : 8.02 fC/DAC code

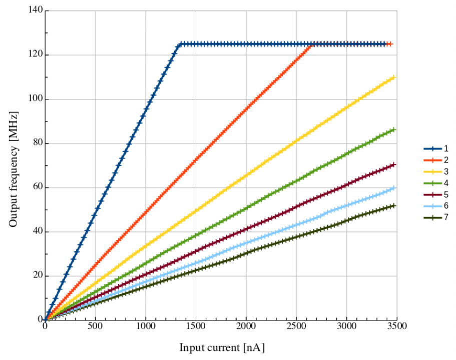
- CMB : channels 11-8
- CM : channels 7-4
- FF : channels 3-0

Linearity - large input current

Polarity = 0



Polarity = 1



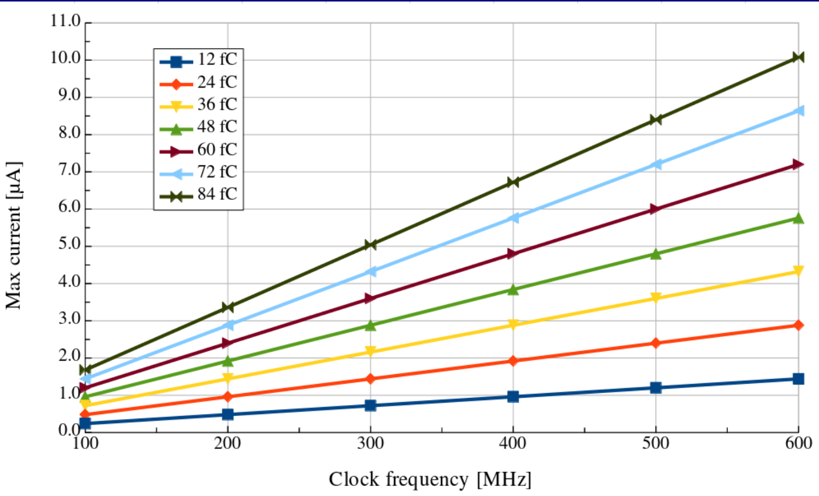
$$\textit{Saturation at } \frac{f_{CK}}{4} = 125 MHz$$

Conclusions

- 12-channels large dynamic range prototype designed in CMOS 28 nm
  - Measurement based on a I$\rightarrow$f conversion
  - Recycling capacitor principle for large dynamic range
  - 3 opamp configurations, all fully functional
  - Linearity in the few % range or better
  - Per channel gain calibration required
- Next activities
  - Tests coupled with the detector
  - Design of a 32-channel version

Spare slides

Maximum current vs clock frequency



Data format

Configuration operation codes

Function	Data 4 bits	Op code 12 bits
Chip Select	1101	$01a_Ba_6a_5a_4a_3a_2a_1a_0 00$
Chip Deselect	0000	00xx xxxx xxxx
Register select	0100	$00010a_6a_5a_4a_3a_2a_1a_0$
Register write	0101	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$
Register read	0110	0000 0000 0000
No operation	1111	0000 0000 0000
Register read word	1000	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$

Data output format

GCR06		**Output word**				
4	3:0	31:28	27:20	19:16	15:4	3:0
0	*n*	1001	*ReadOutReg(n)*			0110
1	*m*	1001	11001100	*m*	*GCR(m)*	0110
0	$n > 11$	1001	1100 1010 1100 1100 1100 1010			0110
1	$m > 6$	1001	1100 1010 1100 1100 1100 1010			0110