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Cleopatra : A 12-Channel Recycling Integrator ASIC for the Readout of Hydrogenated Amorphous Silicon Detectors in Radiotherapy Dosimetry

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The Cleopatra ASIC is a 12-channel prototype ASIC for the readout of hydrogenated amorphous silicon sensors used for real-time dosimetry in radiation diagnostic and radiation therapy.
The architecture is based on a current to frequency conversion based on the recycling integrator principle in order to cover a dynamic range of four orders of magnitude with high linearity.
Three different input amplifier configurations have been implemented in order to check the trade-off between detector capacitance and maximum output frequency.
Cleopatra has been designed in CMOS 28 nm technology and successfully tested in laboratory.

Summary (500 words)

Current and future radiation therapy techniques require high particle fluxes. Therefore, radiation-tolerant detectors are increasingly important in clinical dosimetry. Hydrogenated amorphous silicon (a-Si:H) has been proposed as a suitable material for these applications, due to its high radiation tolerance and low cost.
In parallel, fast readout electronics is required to be able to exploit the advantages of such a sensor. In this paper, a 12-channels readout ASIC prototype has been designed in CMOS 28 nm technology and tested in the framework of the INFN HASPIDE collaboration. The readout architecture consists of a current-to-frequency converter followed by a synchronous 24-bits counter and a temporary storage register. The counter provides the digital measure of the charge released in the detector in a given time window. Its value can be stored in the temporary register and read-out via a bi-directional serial link. The latter is also used to upload configuration parameters. The circuit is designed for a dynamic range between 100 pA and 2 uA, with detector capacitance between 1 and 50 pF.
The current-to-frequency converter is based on the recycling integrator principle : the input current is integrated, thus providing a voltage ramp; when the ramp crosses a threshold, an output pulse is generated. In parallel, a current pulse with constant charge is subtracted from the input, partially discharging the integrating capacitor and thus avoiding the amplifier saturation. The integrated charge in a given time window is thus the product of the number of generated pulses times the amount of charge subtracted. At a first order, the precision of the measurement depends only on the stability of the subtracted charge, which in turn only depends on a capacitor and a voltage value. Therefore very high accuracy can be achieved via calibration. In the Cleopatra prototype, the subtracting capacitor value can be digitally selected from 20 fF to 140 fF in 20 fF steps, while the voltage can be set externally via precise references.
The critical component in terms of the converter maximum frequency is the core amplifier of the input integrator. Therefore, three different architectures have been implemented in order to compare their performances : a two-stage OTA with active-feedback current compensation and a two stage OTA with telescopic second stage with and without gain boosting. The power consumption for the three circuits are 100, 30 and 90 uW, respectively.

The prototype has been tested with clock frequencies of 200 and 300 MHz. A non-linearity around 1% has been measured in the range 1-350 nA for all 7 subtracting capacitor settings. The measured subtracting charge value ranges between 9.2 and and 61 fC for a voltage of 600 mV, i.e. 25% lower than the theoretical value. An improved set-up is under development in order to extend the measurement dynamic range and the clock frequency. Tests with the prototype coupled with a-Si:H sensors are also foreseen in the next months.

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