Power distribution over the wafer-scale monolithic pixel detector - MOSAIX for ALICE ITS3

Szymon Bugiel

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1 Abstract

For the LS3 ALICE ITS3 upgrade the detector material budget reduction has been pushed to the limit by proposing a system composed almost exclusively of silicon wafer thinned to 50 µm. This improves performance, but adds complexity to the ASIC design. It requires a wafer-scale module with embedded power delivery network and on-chip data transfer, which were usually done through flexible printed circuit cable.

This contribution covers different aspects of the power delivery network design for a wafer-scale detector. It describes the difficulties, shows possible solutions and presents the power scheme design of the full-size ITS3 sensor prototype MOSAIX.

2 Summary

MOSAIX is the full-size, full-functionality ALICE-ITS3 monolithic pixel detector prototype. It has been designed in the TPSCo. 65 nm technology that offers a stitching technique which allows for a wafer-scale sensor fabrication. For MOSAIX only 1D-stitching is being utilized, resulting in the chip dimensions of 26.6 cm × 1.96 cm. Since the system integration constraints allow for connection only to the short edges, chip powering becomes difficult. Nevertheless, uniformity of the power supply is very important to achieve reliable chip operation and good performance. Thus, it is required to have a strong power network which will not only bring all the necessary power over 13 cm to the middle of the detector, but also mitigates the impact of the accumulated IR-drop.

Static, purely resistive drop over the power network is a fundamental problem. With the connections only on opposite edges and well averaged current consumption one can use a 1D approximation where the maximum DC IR-drop over the rail is given by:

$$V_{drop}{}^{max} = \frac{I_{total} \times R_{total}}{2}$$

where R_{total} is the power rail resistivity (from pads to the middle of the chip), and I_{total} is the combined current consumption of that section. Despite the low power consumption over the sensitive area (below 40 mW/cm^2) and the use of a thick metal layer, the $V_{drop}{}^{max}$ can reach up to 100 mV (on each supply and ground net). This can be either actively compensated with regulators distributed over the chip or the entire design needs to be robust enough to cope with varying conditions. For MOSAIX both approaches were evaluated and finally the latter was chosen.

Another big concern for the large area devices is yield. With the high circuitry density one cannot neglect manufacturing faults leading to short-circuits. Without precautions any local short over the power supply can lead to full sensor malfunctioning. Two countermeasures were exploited to mitigate that. A straightforward solution is to maximize the spacing between the power nets. For that purpose dedicated DRC (Design Rules Checking) rules have been introduced. They ensure significantly larger spacing (at least 4 times) than the minimum allowed by the foundry. This is relatively easily applicable to the top metals, but implies a stronger penalty when applied to lower metals. To maintain high circuitry density over the pixel array its power grid has been decoupled from the global network. The local circuitry is being powered from the local supplies that are derived from the global ones via configurable power switches. Each MOSAIX has been divided into 144 completely independent tiles that can be switched off individually in order to disconnect any faulty unit. This also allows to keep the local power uniform (less than 3 mV of the combined DC IR-drop), which results in the almost negligible threshold variation over the tile (comparable with pixel noise).

This contribution describes in detail the powering scheme chosen for the MOSAIX sensor ASIC. It summarizes the experience gained during the design and from the measurements of the first stitched wafer prototypes, MOSS and MOST.