

Power distribution over the wafer-scale monolithic pixel detector - MOSAIX for ALICE ITS3

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on behalf MOSAIX design team and the ALICE collaboration

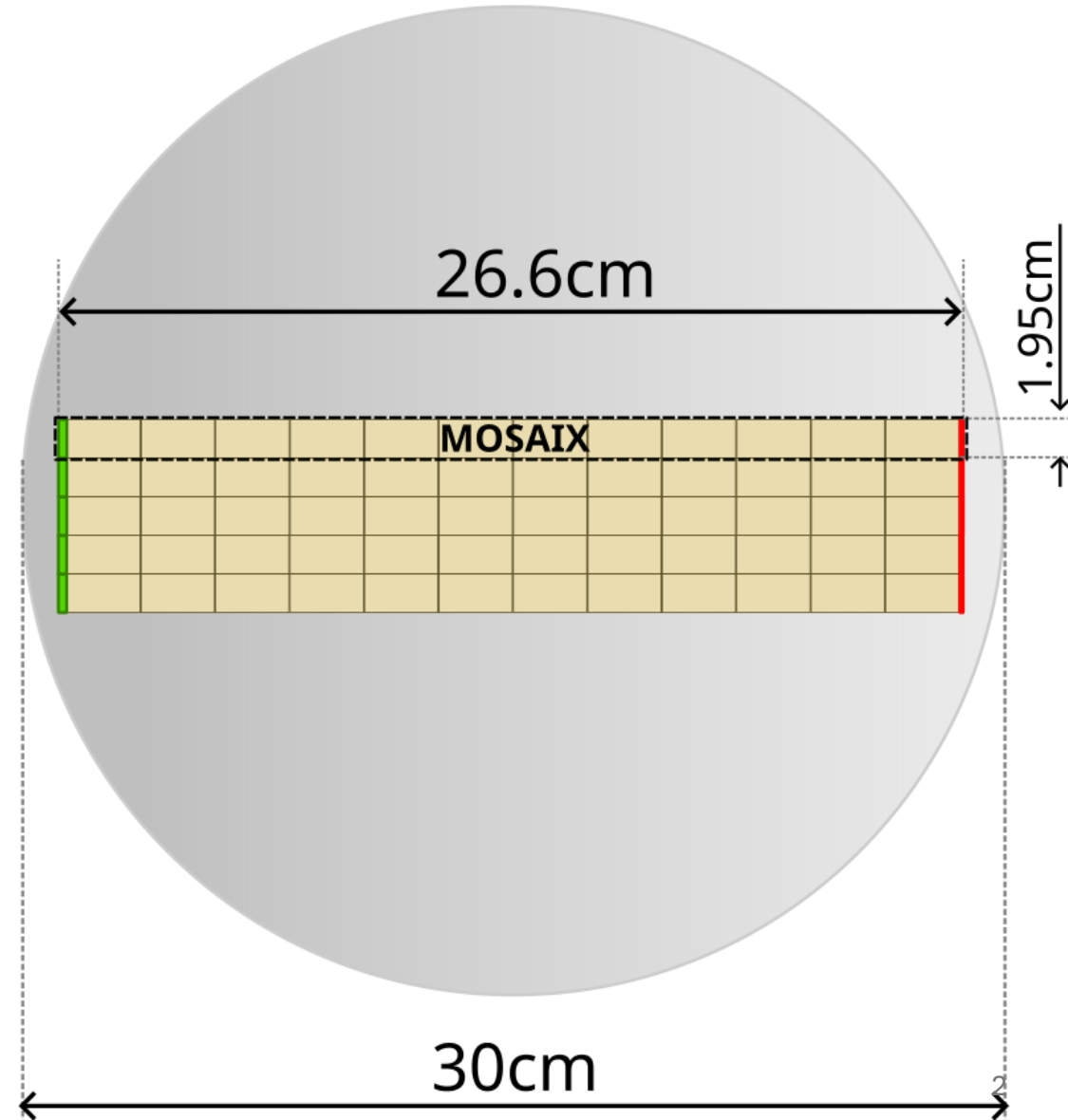
TWEPP 2024
02 October, 2024

➤ Wafer-scale chip design challenges covered in this talk:

- 1) How to ensure high yield?
- 2) How to distribute the power over the chip?
- 3) How to validate power grid performance?

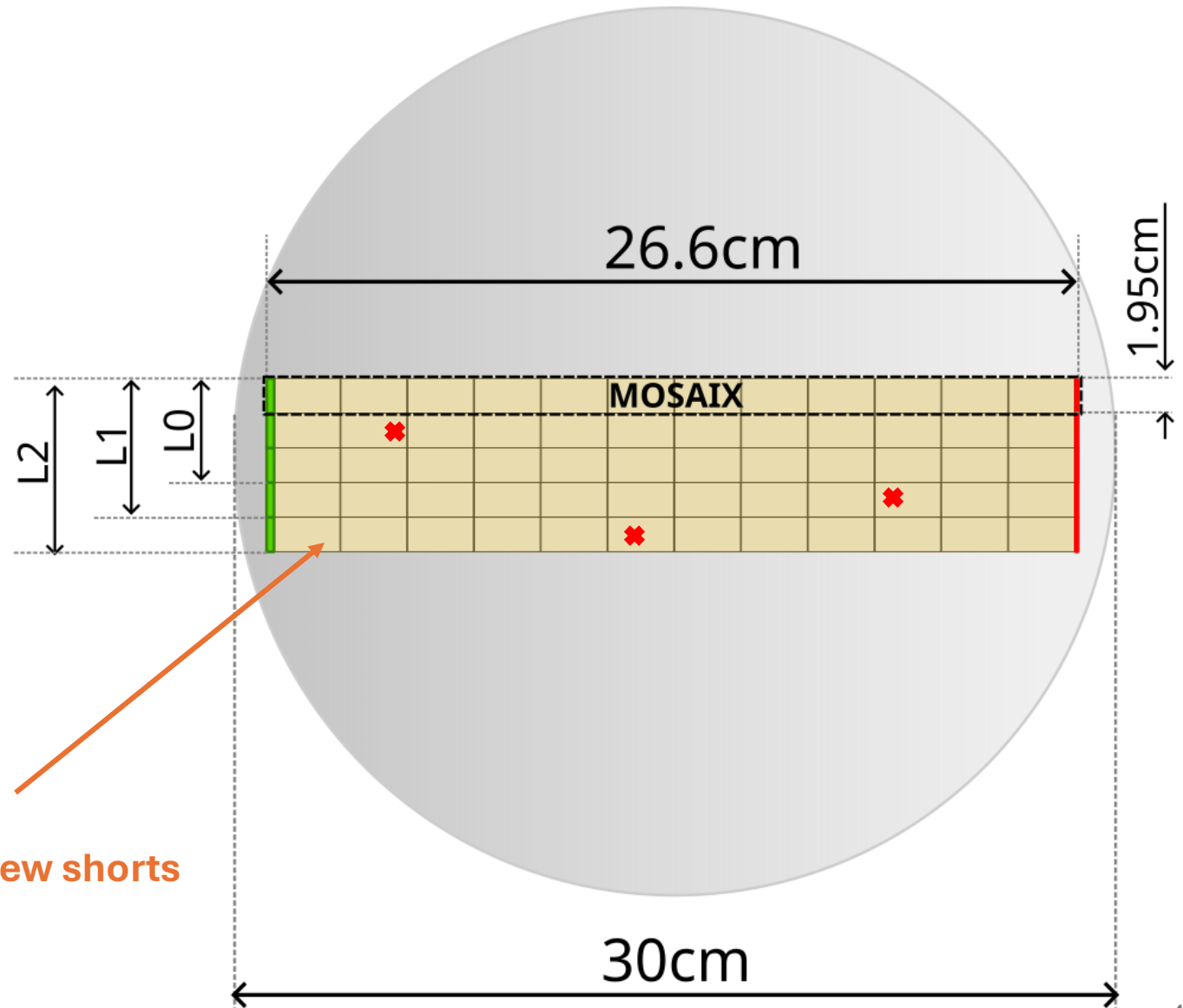
➤ MOSAIX detector:

- full-size prototype of the ALICE ITS3 sensor
- 26.6cm x 1.95cm
- Monolithic
- TPSCo 65nm



How to cope with chip-killing defects?

- Alice ITS3 layer: 26 cm x 6-10 cm devices
- **Yield needs careful assessment!**
- Operation with few defects must be possible
- Shorts probability to be minimized

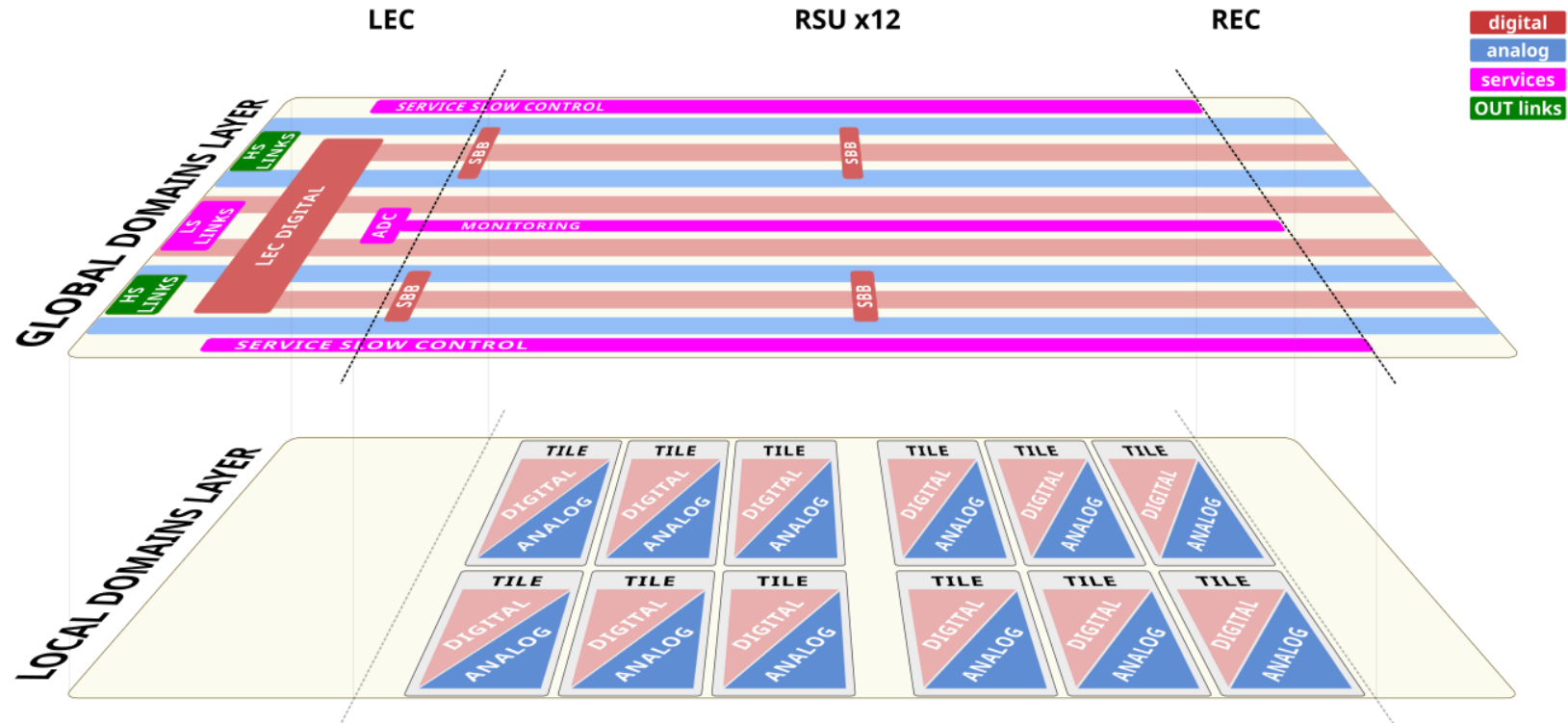


Without countermeasure's
--> yield gets very low with few shorts

Yield: Power planning – power segmentation

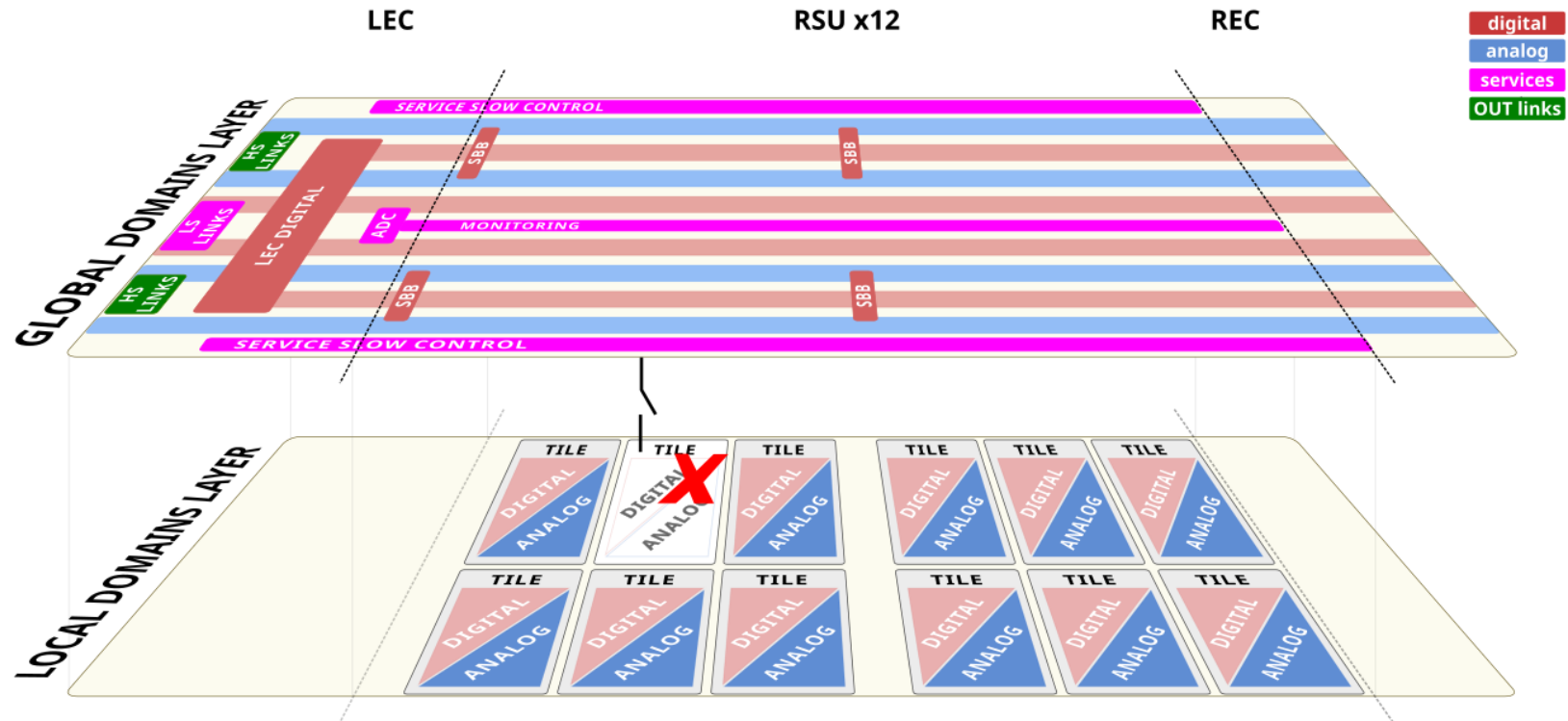
➤ Two powering layers

- GLOBAL
 - **very robust**
 - supplies only configuration circuitry
- LOCAL
 - powers most of the chip
 - **segmented** into 144 independent tiles
 - allows **defects isolation**



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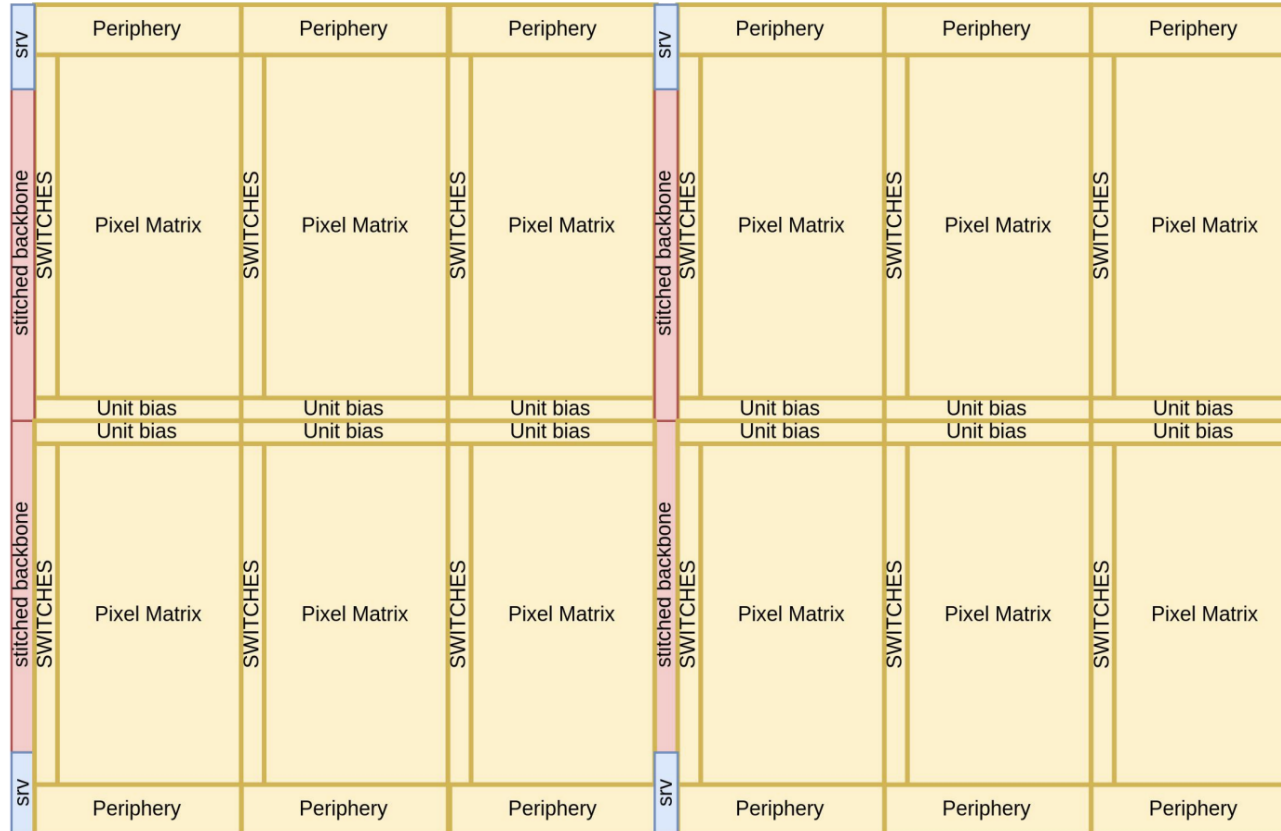


➤ Safe power-up procedure:

- Separate services power domain
- Tile's power for configuration before others supplies are ON

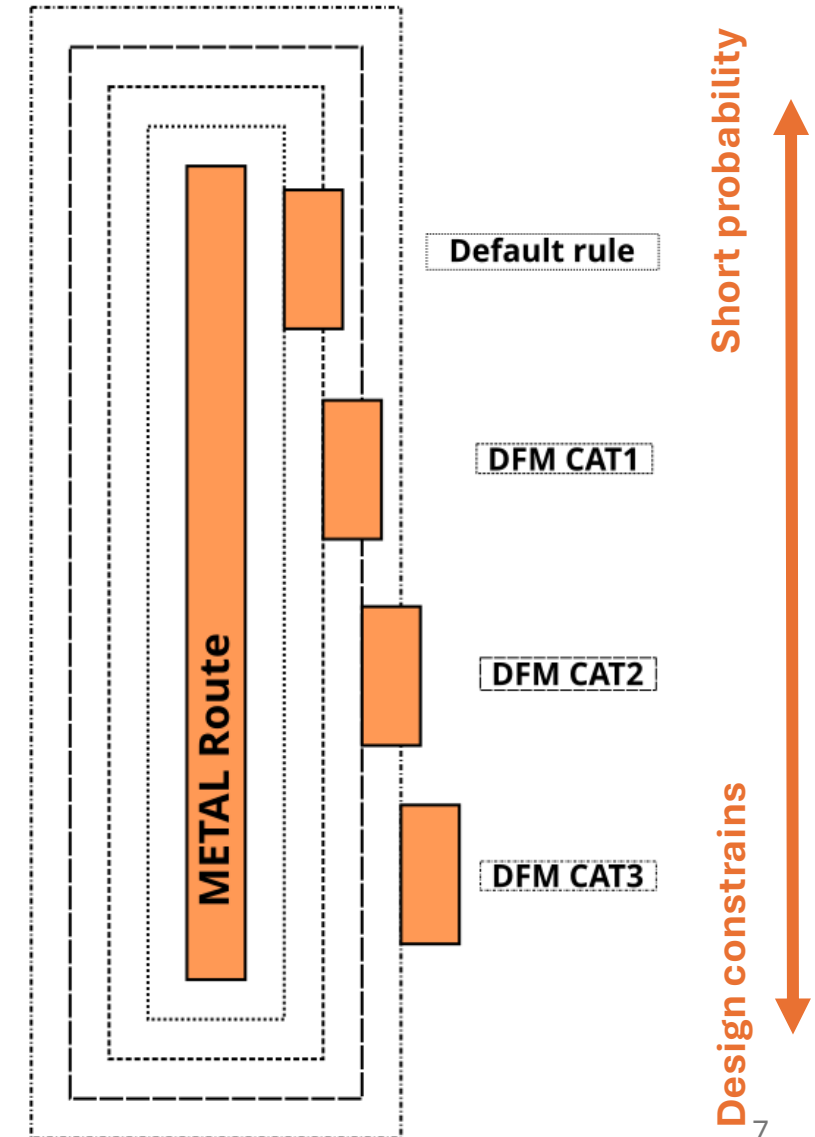
Defective tile adds 0.7% of dead area, but chip maintains functional!

- Sub-blocks are categorized by their failure impact
 - CAT1** – minor impact, pixel/pixel group malfunction
 - CAT2** – moderate impact, could cause full tile malfunction
 - CAT3** – high impact could affect the performance of entire chip
 - Complemented with **custom DRC rules** for design checks (width / spacing / via enclosure / via count)



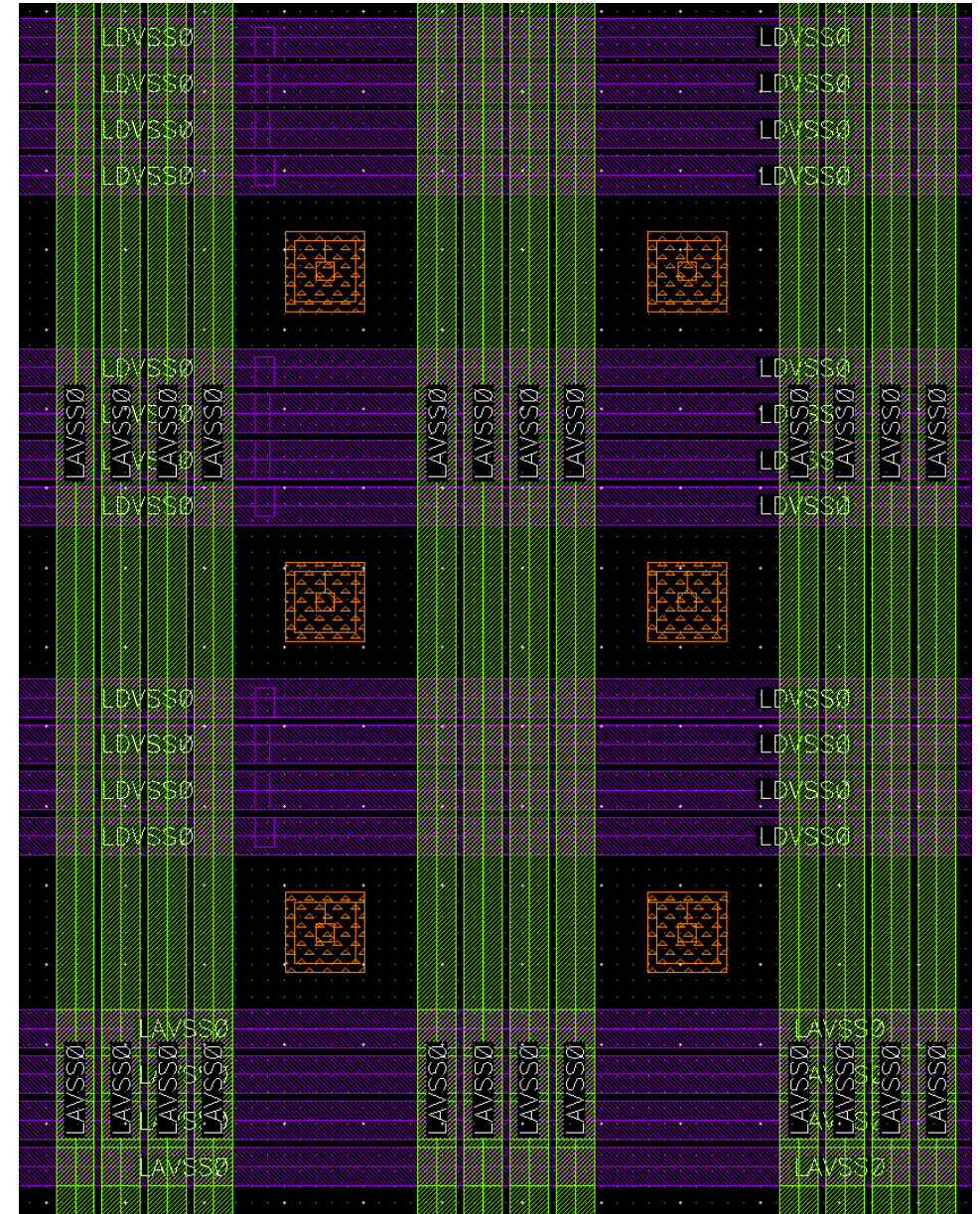
Repeated Sensor Unit floorplan

Eg. Custom metal min spacing rules

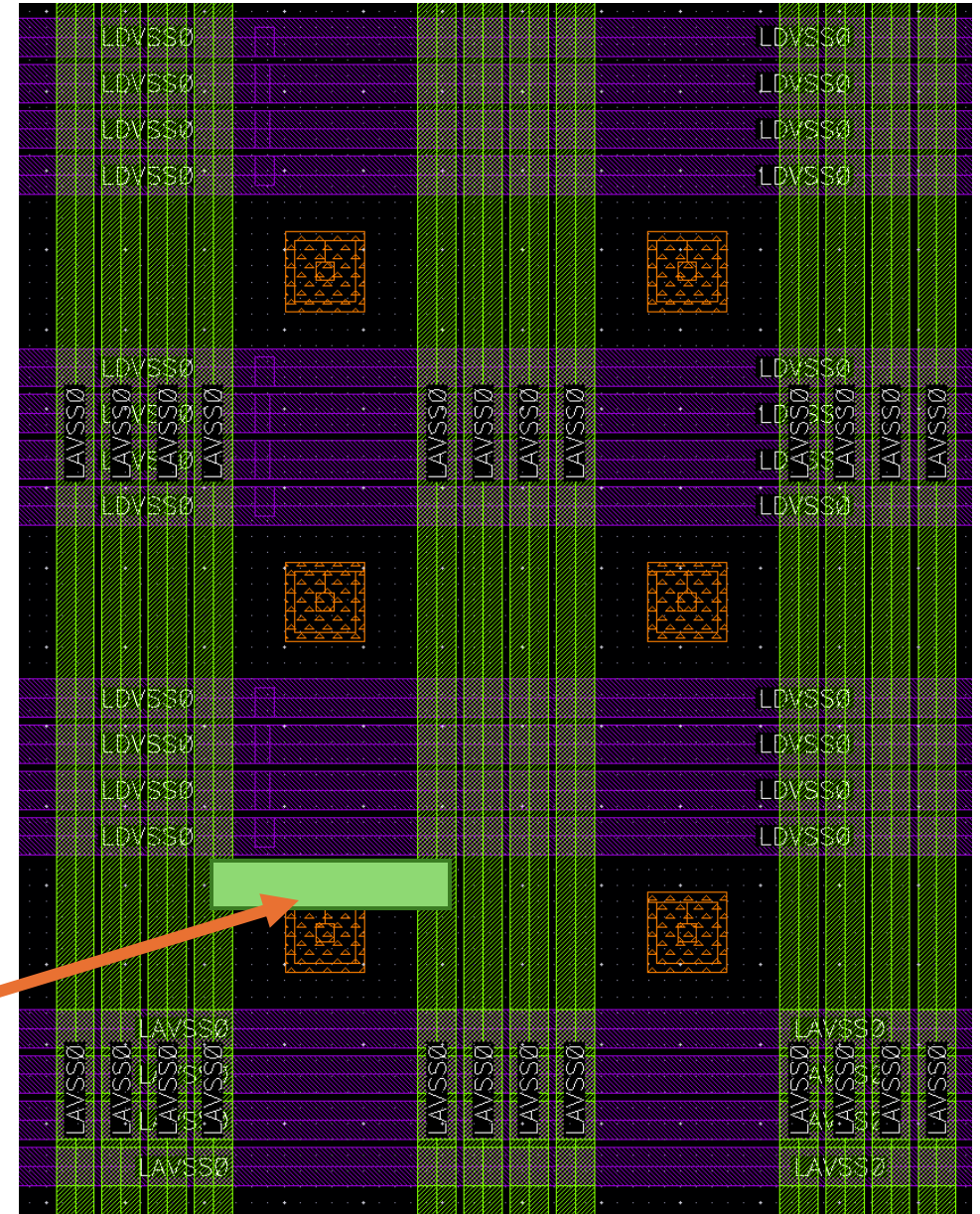


Yield: Conservative design

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- Power nets spacing constrained even further
 - Connectivity aware custom DRC checks for power grids



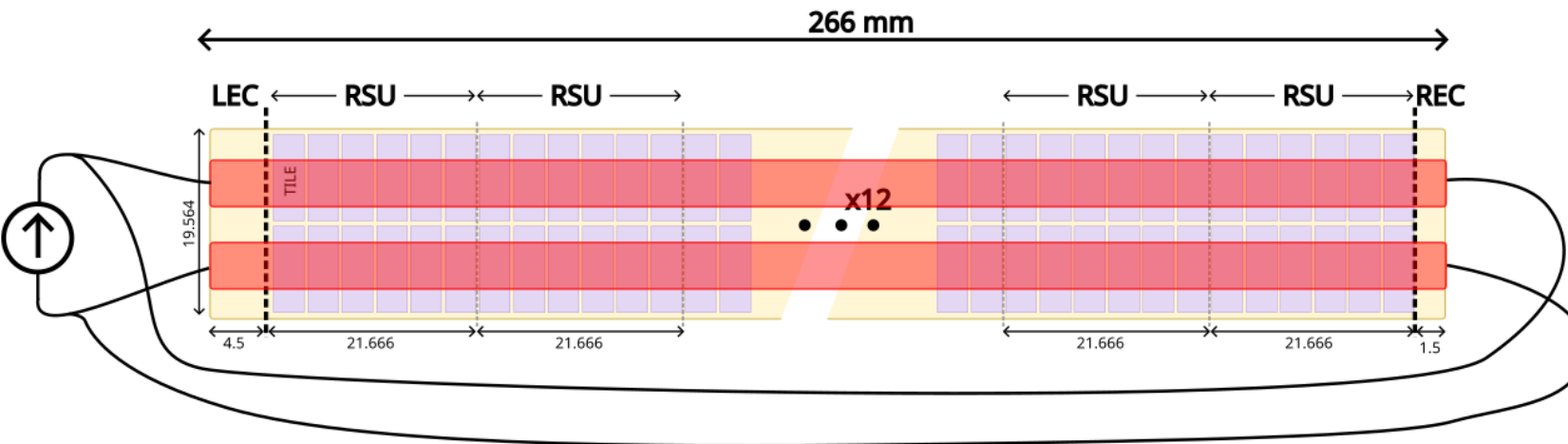
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- Power nets spacing contrained even further
 - Connectivity aware custom DRC checks for power grids
- Power grid designed for burn-throughs
 - power grid are able to deliver >100 mA to any location
 - See Gregor Eberwein talk



Remaining shorts can be burned-out with high currents

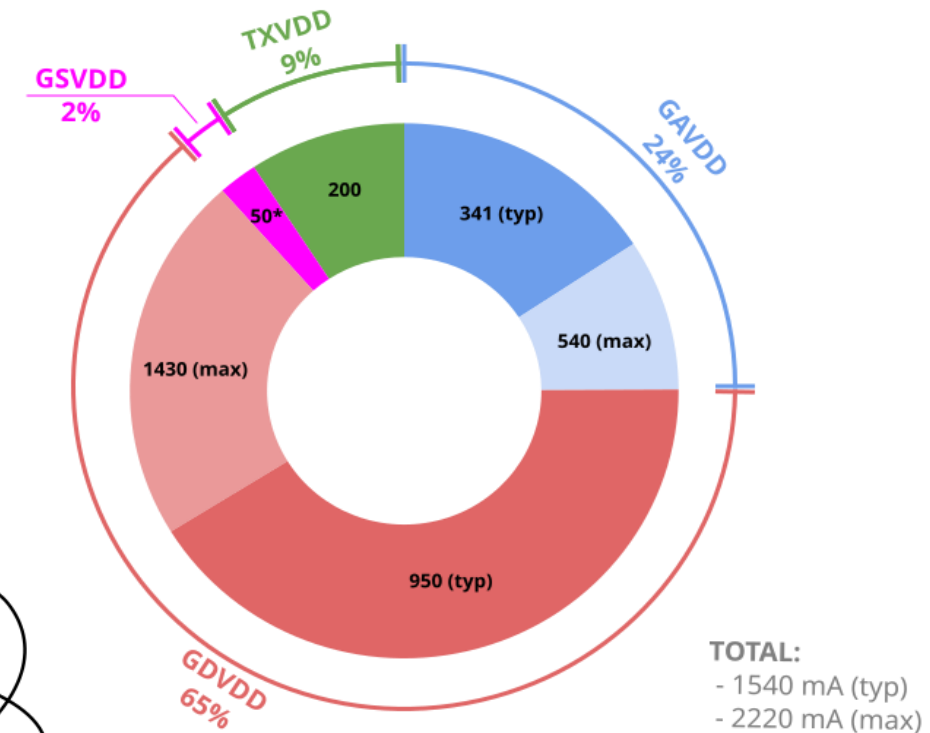
How to distribute the power?

- >2 A via short edge – only 28 supply pads (A+D) on LEC
- Redistributed on-chip over the 26 cm
 - IR drops → challenging despite <math><40 \text{ mW/cm}^2</math>

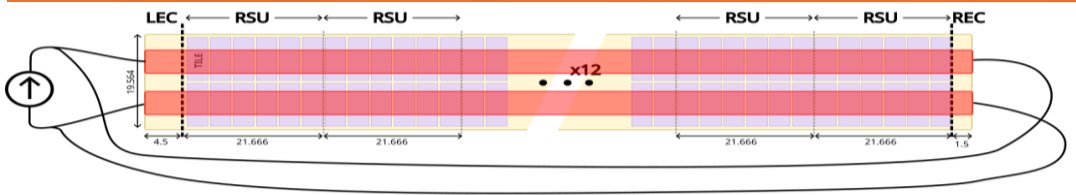


LEC – Left End-Cap
RSU – Repeated Sensor Unit
REC – Right End-Cap

MOSAIX consumption breakdown



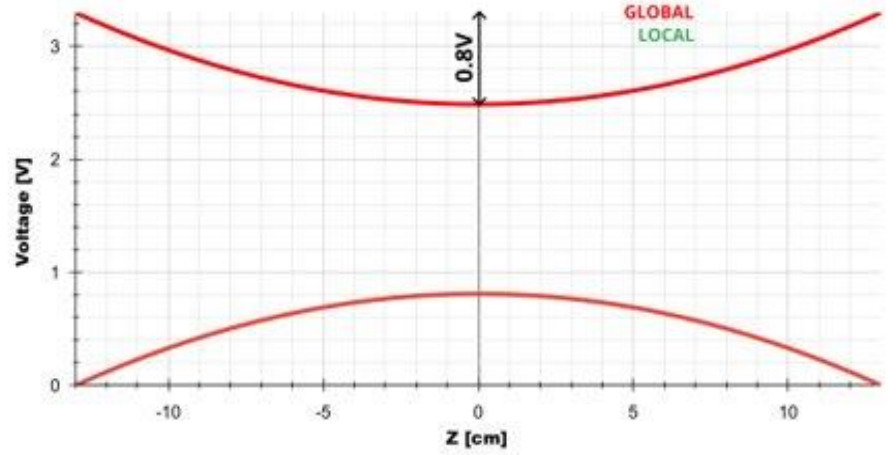
Tiles powering schemes



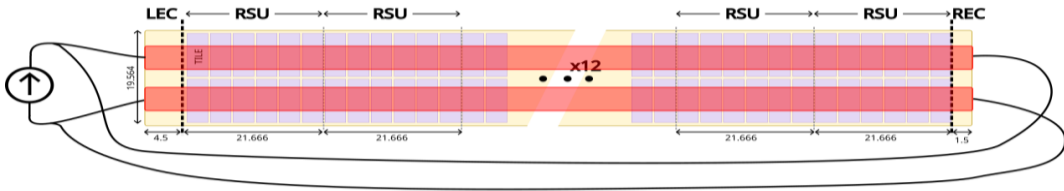
➤ How to derive local power from the global?

- Serial powering:
 - + reduces IR drops
 - ✗ not an option --> common PSUB

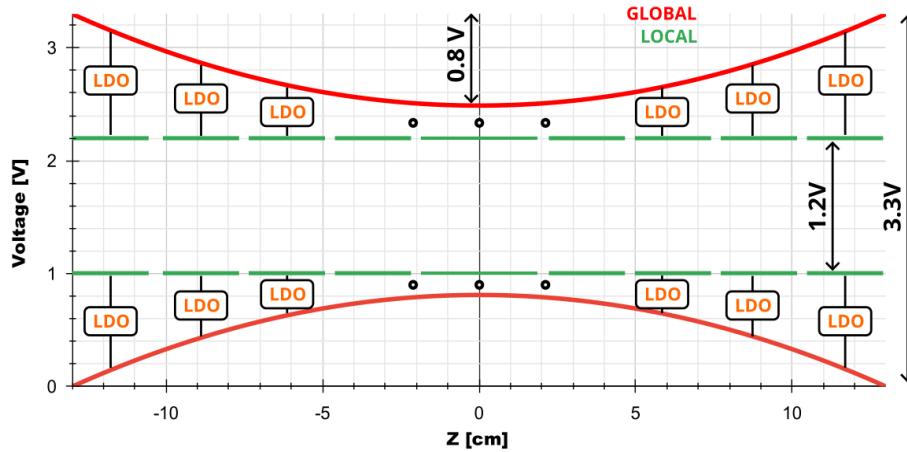
Initial worst case IR drops estimates



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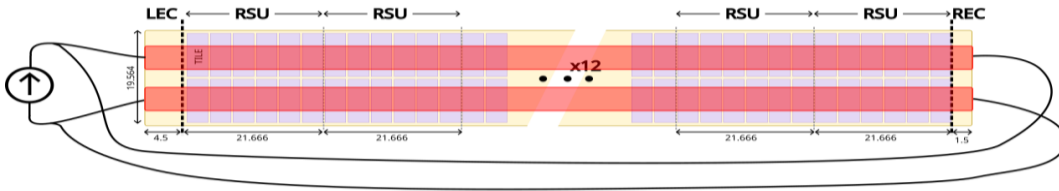
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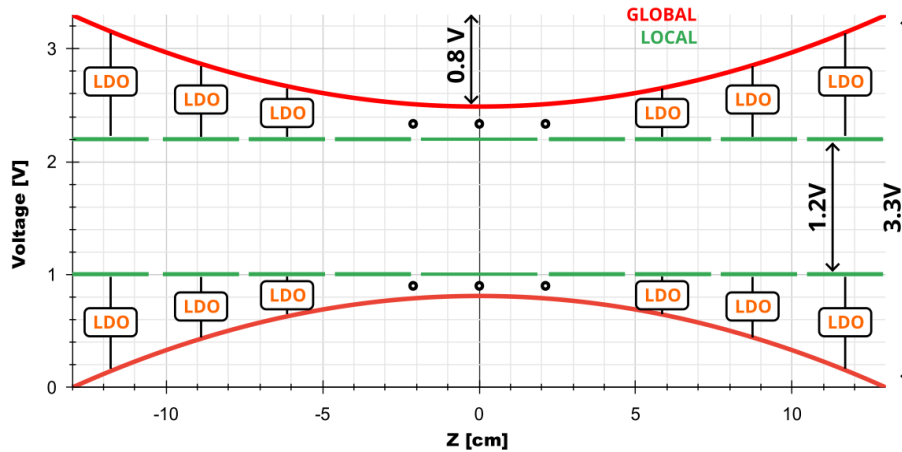
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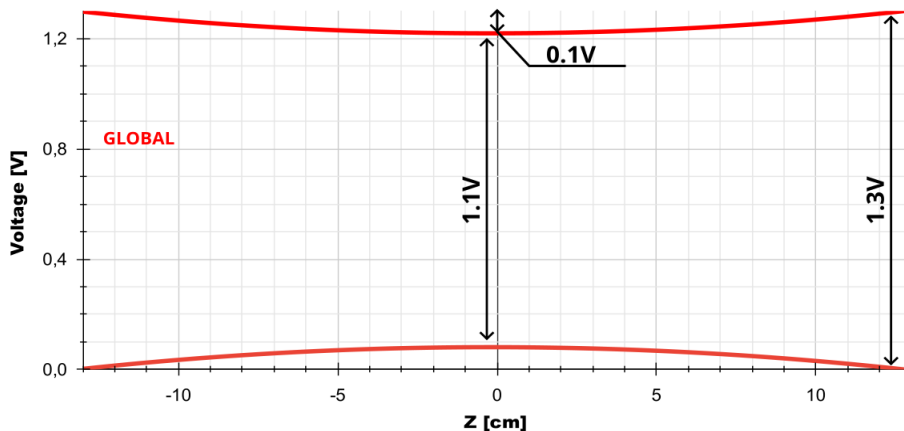
- Per-tile Low-Dropout regulators (LDO):
 - + control
 - + current stability (shunt LDO)
 - needs 3.3 V supply --> power consumption
 - dual-rail regulation
 - complexity --> dead area
 - The only choice with up to 800 mV IR drops (per rail!)



Initial worst case IR drops estimates



Worst case IR drops in new metal stack



➤ How to derive local power from the global?

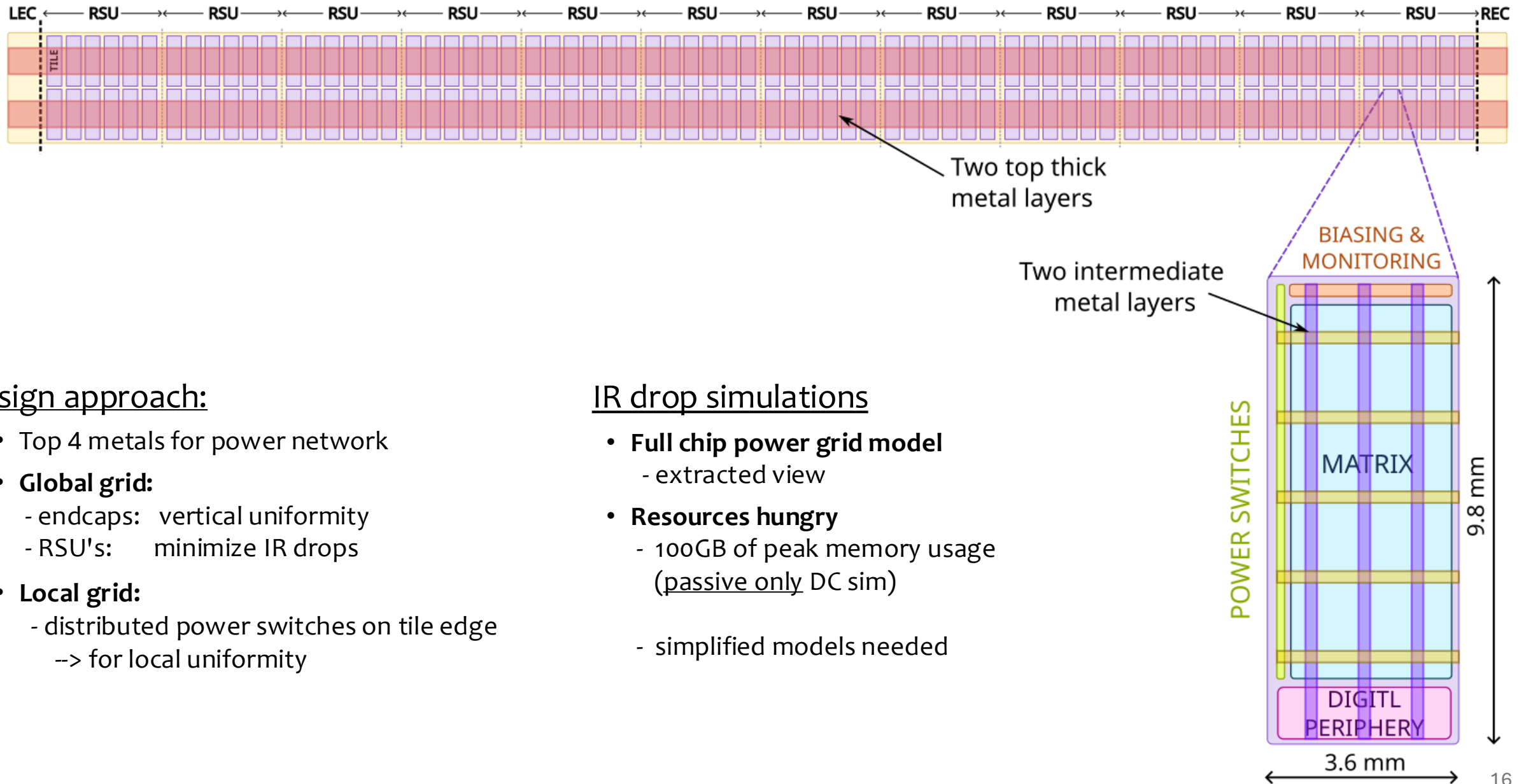
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 - complexity --> dead area
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- Power switches:
 - + simplicity --> least area
 - + power-efficient
 - no control
 - tiles operate at different supplies
 - > [1.2V +/- 10%] operation margins

Power grid design and validation

- Key requirements:
 - **< 100 mV IR drop** on the global power rails
 - **Equalized drops** on analog and digital global supplies
 - **Minimized drop on the local analog** grid
(each mV on supply → 1.5e- threshold difference)

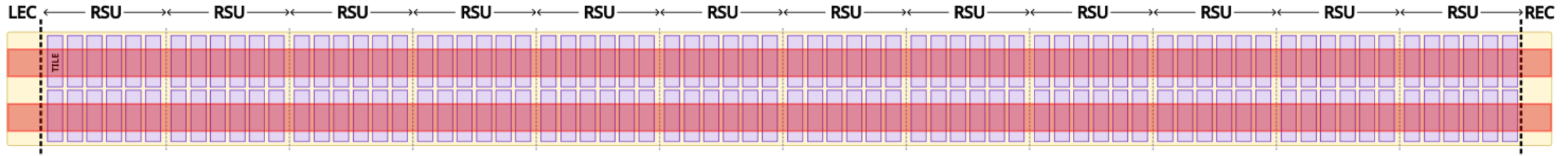


Design approach:

- Top 4 metals for power network
- **Global grid:**
 - endcaps: vertical uniformity
 - RSU's: minimize IR drops
- **Local grid:**
 - distributed power switches on tile edge
 - > for local uniformity

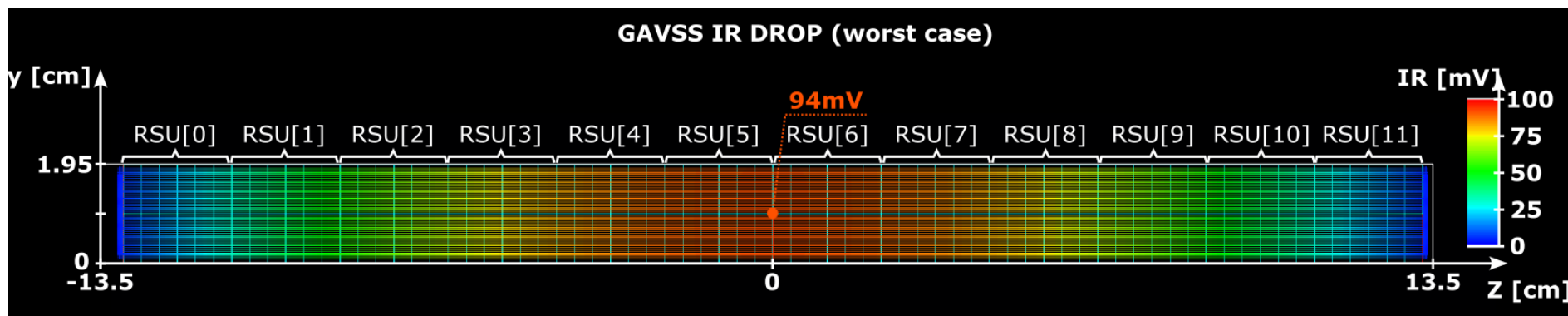
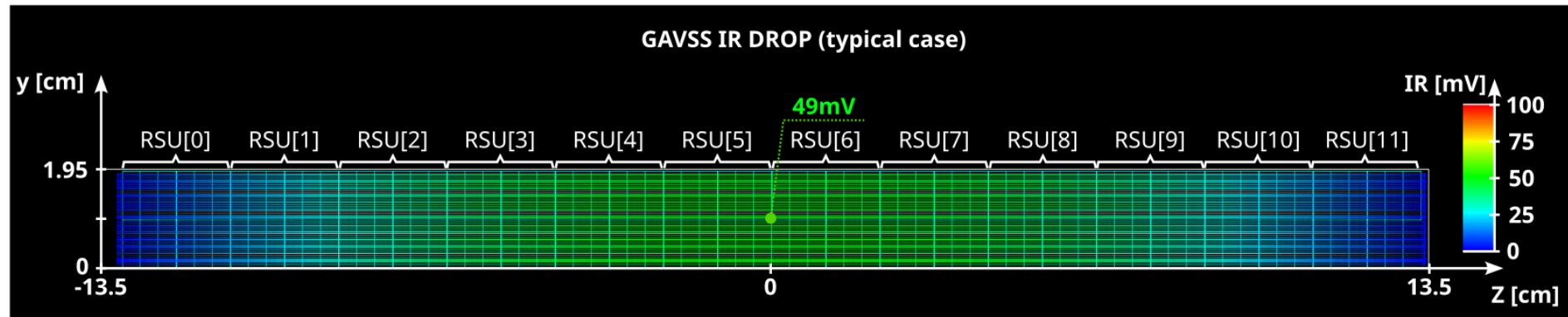
IR drop simulations

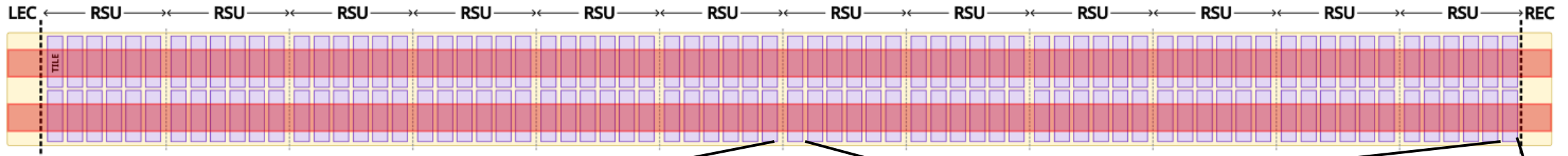
- **Full chip power grid model**
 - extracted view
- **Resources hungry**
 - 100GB of peak memory usage (passive only DC sim)
 - simplified models needed



Results

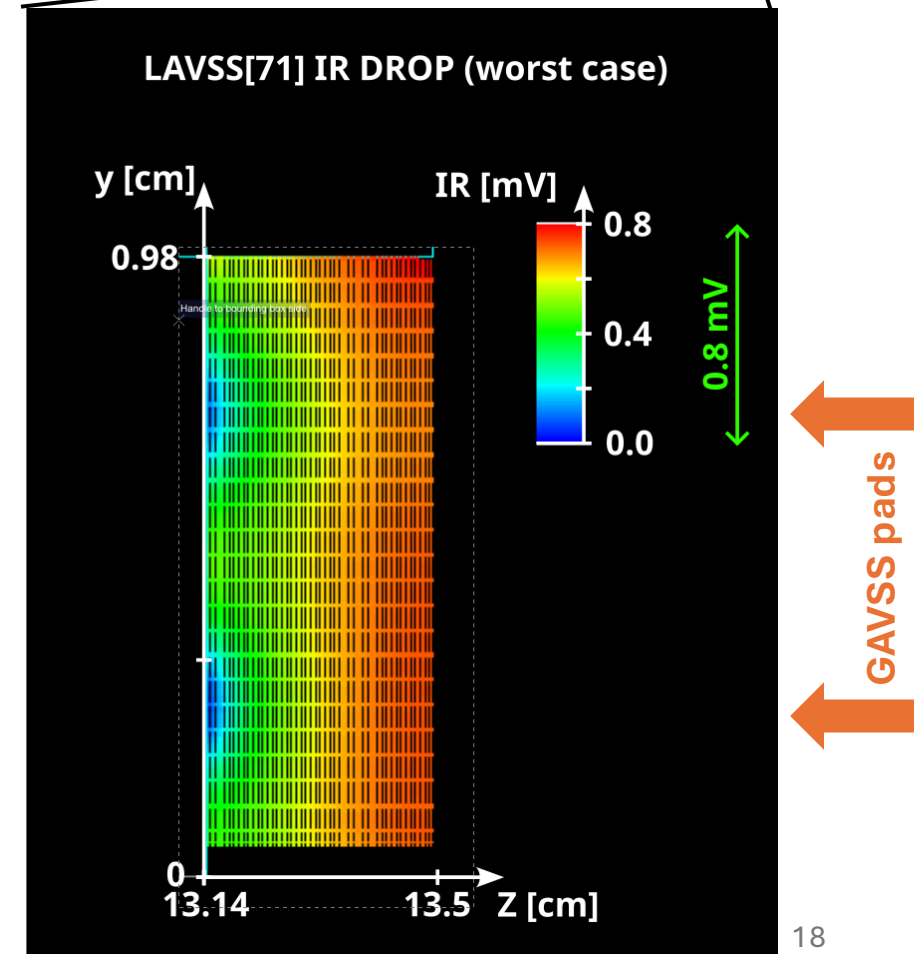
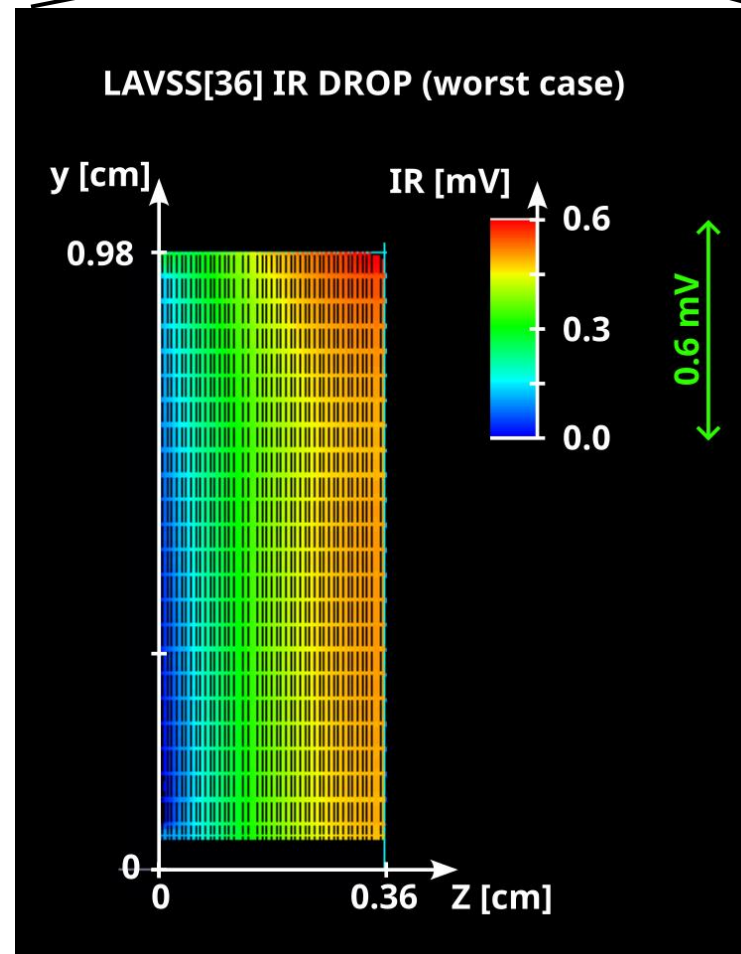
- Simulation results matching preliminary predictions
 - > within specs
- Analog domain
 - typical: **50mV** max IR drop
 - worst: **90mV** (high consumption, worst RC)
- Digital domain [plots in backup]
 - typical: **50mV** max IR drop
 - worst: **80mV**





Results

- **Analog domain**
 - excellent uniformity (< 1 mV spreads)
 - minor impact of global grid (fan-in into pads)
- **Digital domain** [plots in backup]
 - good uniformity (< 1 - 4 mV spreads)
 - some impact of global grid visible (pads locations)



- **MOSAIX now in an advanced design stage**
- **High yield achieved by:**
 - segmentation into the tiles
 - > at **0.7%** chip area **granularity**
 - power grid robustness
 - > spacing between global power stipes
 - failure impact categorizing
 - > with **custom design checks** coded
 - design for burn-through
 - > power grid capable to deliver **> 100 mA for burnout**
- **Different solutions for tiles powering were evaluated**
 - power switches chosen
- **Power grid validated to satisfy specifications**
 - **< 100 mV** worst case IR drop on global supplies
 - local analog supply uniformity within **1 mV**

Backup

➤ ALICE Inner Tracker System Upgrade:

- replacement of a standard stave based modules with truly cylindrical full silicon layers
 - > minimal mechanical support thanks to the stiffens of bent silicon
- 5x lower material budget
- closer to the interaction point

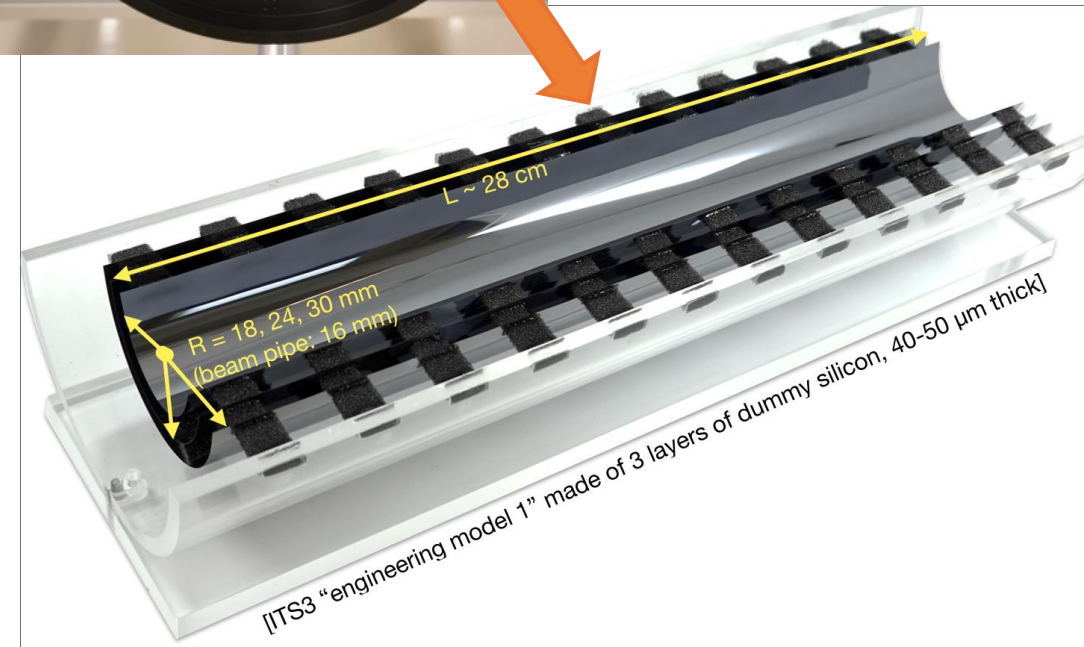
➤ Detector requirements:

- 50 μm thick **wafer-scale monolithic** detector
- extremely **low power** (below $40 \text{ mW}/\text{cm}^2$)
- **powered only from the endcaps**
- **bare silicon:**
 - no off-chip power reinforcement
 - no off-chip data links

ITS2

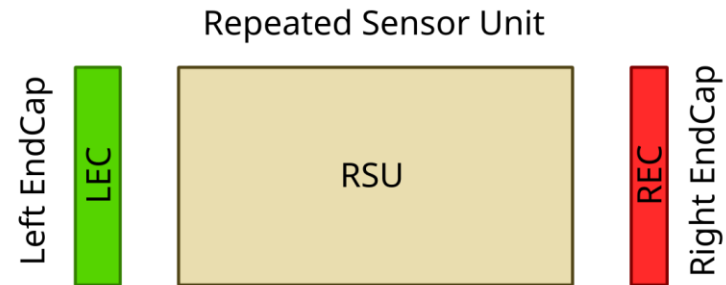


ITS3

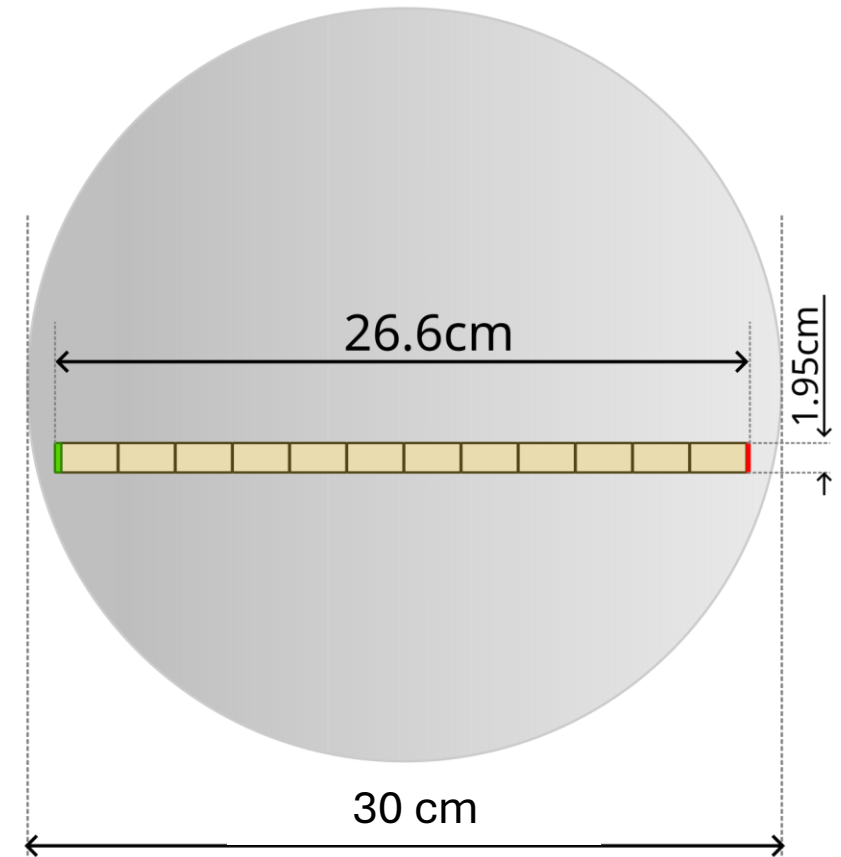


➤ Wafer scale detector? --> Stitching technique

- Dividing a reticle into a separate units:



- Stepping the lithography process with the repeated unit such that the connectivity on the edges is maintained
- Adding endcaps on the sides
--> **Single MOSAIX chip: 26.6cm x 1.95cm**



Tiles powering features

Power switches needs to be configured before main global supplies are ON

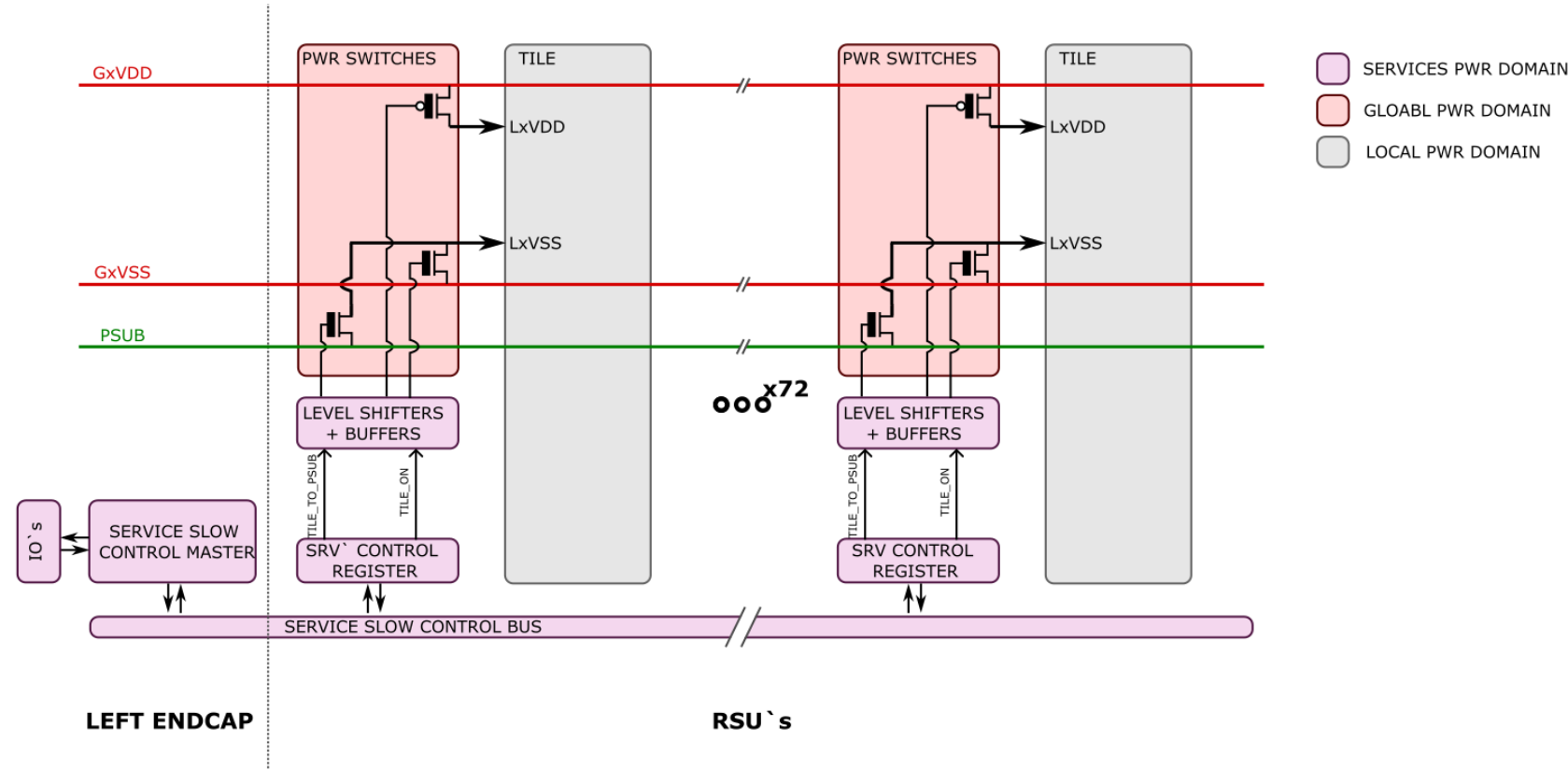
- Services slow control:
 - defines power status for every tiles
 - Services domain powered up before other global supplies

SEE immune power control

- SET immune transmission
- Triplicated tile power state control registers

Tiles needs to be allowed to float to PSUB

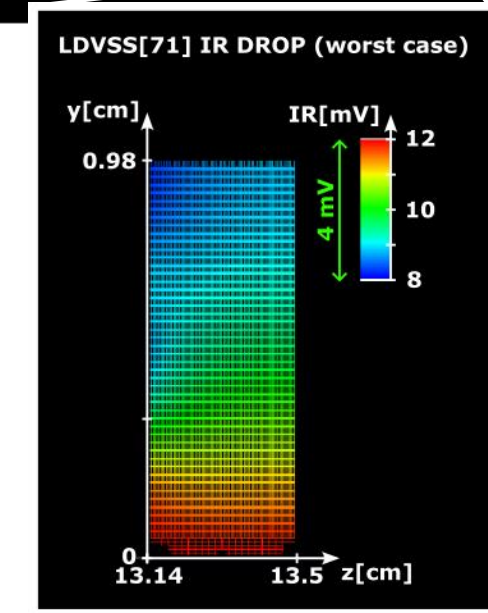
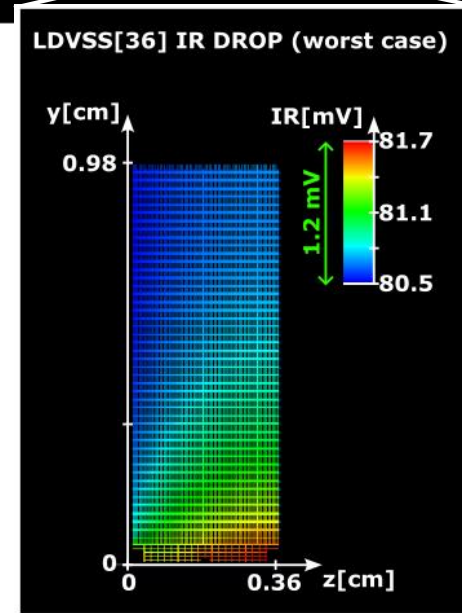
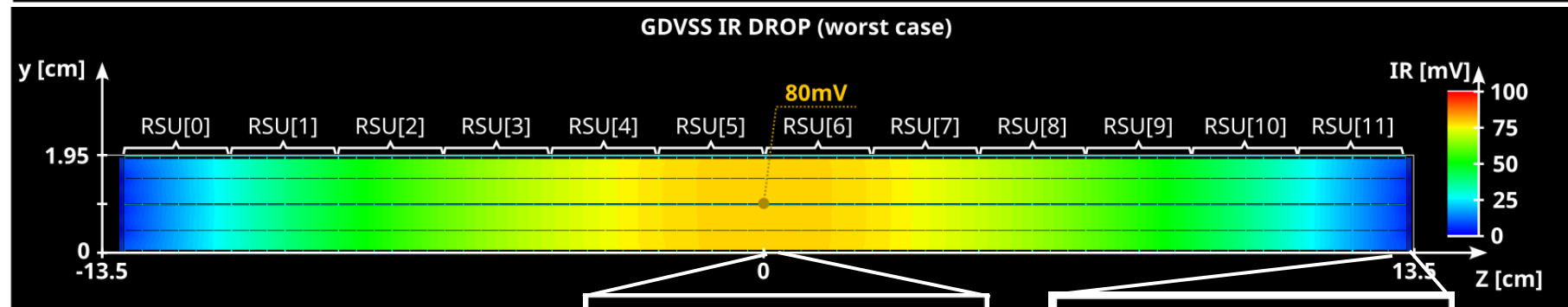
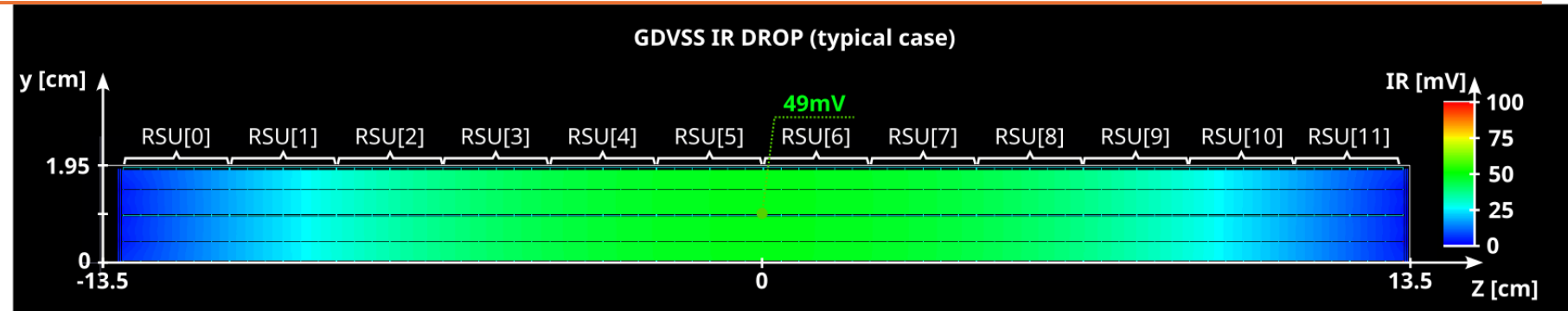
- OFF tiles can be either remain floating or be actively tied down to PSUB (negative voltage down to $-2V$)
 - > power switches are thick oxide devices
 - > there is a need of a level shifter
- Back-to-back diode between local grounds to ensures safe local cross-domain signaling with 1.2V devices



Results

- **Digital domain**

- **50mV** drop over the global network in typical case
- can increase up to **80mV** for highest consumption and worst RC corner
- slightly higher local un-uniformity especially next to the endcaps, but still not warring



Off-chip power delivery

➤ Padring:

- up to 20 mV drop over standard power IO's
- > redesigned to increase conductivity towards the core
- > 4x improvement

➤ Off-chip powering:

- up to 20 mV drop on wire bonds
- > customizes bond pads
- > 2x improvement
- 15mV/rail cabling to C side
- Settling accuracy: ~15 mV

➤ With all the improvements we are just within specs!

