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Functional Verification for Endcap Concentrator ASICs in the High-Granularity Calorimeter Upgrade of CMS

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The High-Granularity Calorimeter (HGCAL) of CMS will undergo a major upgrade during the Long-Shutdown 3. The Endcap Concentrators (ECON) ASICs represent key elements in the readout chain, processing trigger (ECON-T) and data (ECON-D) streams from the HGCROC to the LpGBT. The ECONs will operate in a radiation environment with a High-Energy Hadron (HEH) flux of $3 \cdot 10^6 cm^{-2} s^{-1}$.

This contribution describes the Universal Verification Methodology (UVM)-based functional verification of the ECON ASICs focusing on the re-use of existing components to manage the complexity of the verification environment.

Summary (500 words)

The High Granularity Calorimeter is a 47-layer sampling calorimeter that will operate in the CMS detector, upgraded for the High Luminosity (HL) LHC. Covering a 600 m2 area with over six million channels, each equipped with sensor pads ranging from 0.5 to 1.0 cm2, it relies on the HGCROC ASIC to digitize sensor signals. Subsequently, the digitized data undergoes processing and zero-suppression along two independent paths: the trigger path, managed by the ECON-T ASIC, and the data path, managed by the ECON-D ASIC. The former produces Level 1 Trigger (L1) primitives for each bunch crossing, while the latter forwards data packets to the acquisition system at an L1 rate of 750 kHz. These ASICs operate in tandem, sharing a foundational infrastructure, synchronized clocking mechanisms, and input/output protocols, while drawing upon established silicon-proven Intellectual Property (IP) for enhanced efficiency and reliability. Both ASICs will operate in a radiation environment with an HEH flux of $3 \cdot 10^6 cm^{-2} s^{-1}$. Distributed Triple Modular Redundancy (TMR) is implemented to allow the ECONs to operate in the radiation environment.

Given the wide variety of detector configurations and the different operative modes of the two ECONs, functional verification is a must for first-time-right silicon. The UVM verification framework is built to maximise component reuse and avoid duplication of code across identical blocks on the two ECONs. The testbenches were built with the possibility to use different data sources: constrained random data to hit corner cases, physics data to stimulate real-operational scenarios, and data generated using the RTL of the HGCROC ASIC to catch potential inter-chip operational issues. The design was verified using the same testbenches at RTL, triplicated RTL, and gate-level with annotated delays.
The contribution will elaborate on the functional verification strategy employed and how the testbenches were designed for re-use exploiting UVM best practices.

The verification of robustness against Single Event Effects (SEE) was treated as an additional verification goal in the verification plan. Two approaches were used to tackle the problem. First formal verification was used to verify for Single Event Upset (SEU) robustness on single-clock blocks. Later fault injections in simulation were used in the triplicated RTL, SEUs, and gate-level netlist, SEUs and Single Event Transients (SETs).

The first ECON-D prototype was submitted in March of 2023. Comprehensive chip testing and radiation characterization since June have revealed no major issues. Final production versions of the ASICs were submitted for fabrication in December of 2023.

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