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UKRI-MPW1: a High Voltage CMOS pixel sensor for high radiation tolerance

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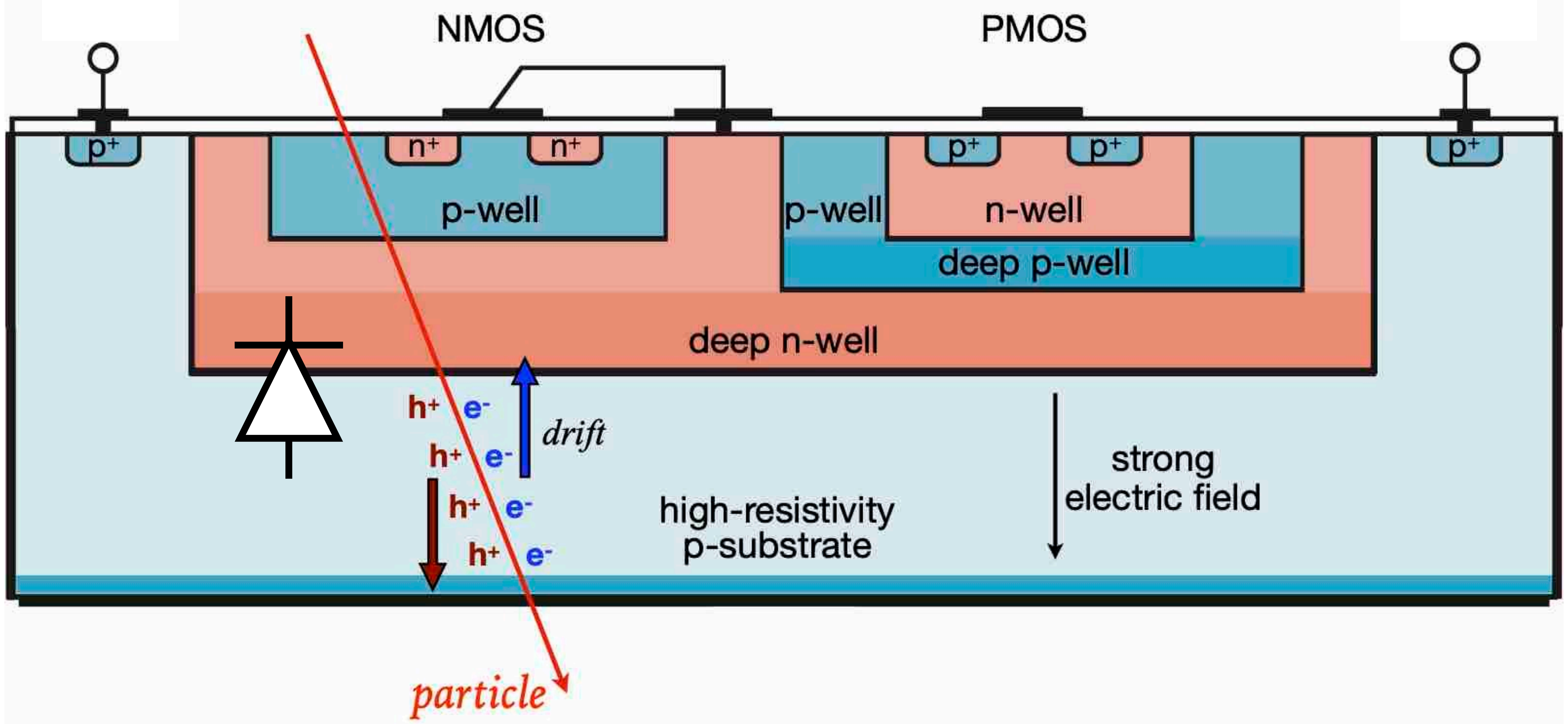
Introduction: HV-CMOS sensor

- Sensing diode and readout electronics are in the same substrate (**monolithic**).
- Single layer structure → **low material budget**.
- High bias voltage forms a wide depletion region (**NIEL radiation tolerant**).
- The Liverpool HV-CMOS group has developed the UKRI-MPW series HV-CMOS prototypes using the **LFoundry 150 nm process**.



Cross-section of a typical large fill-factor HV-CMOS sensor

From UKRI-MPW0 to UKRI-MPW1

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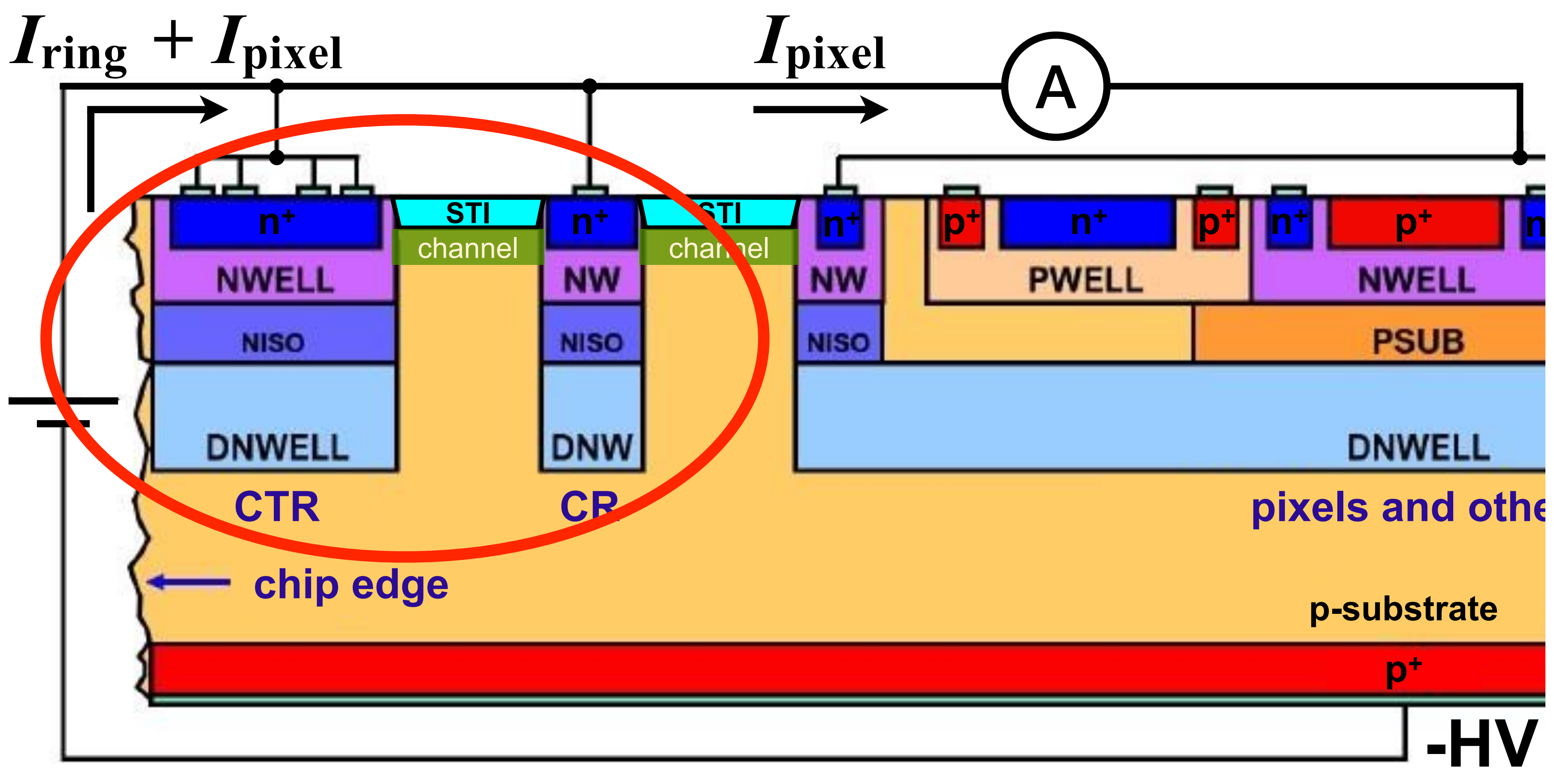
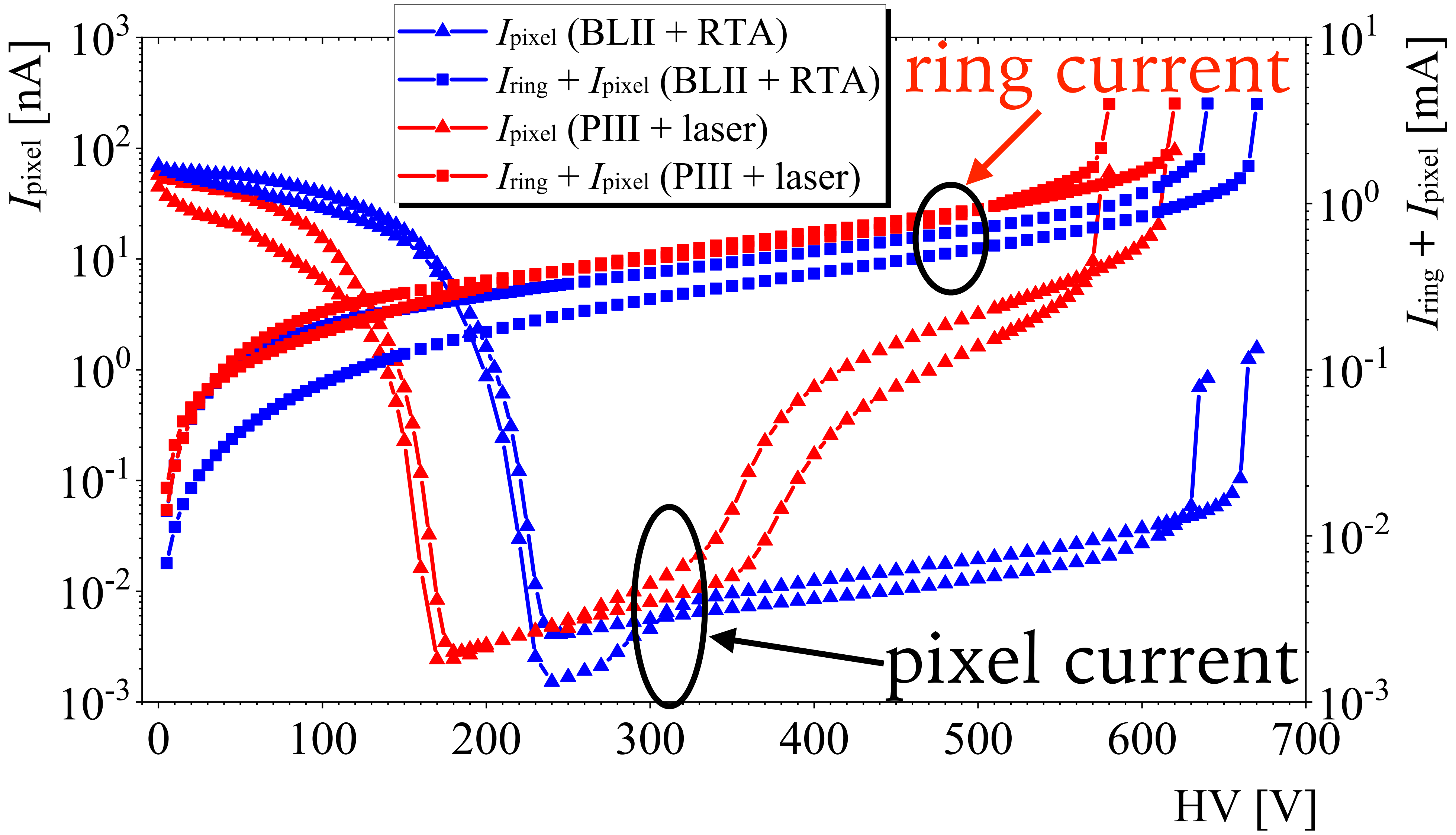
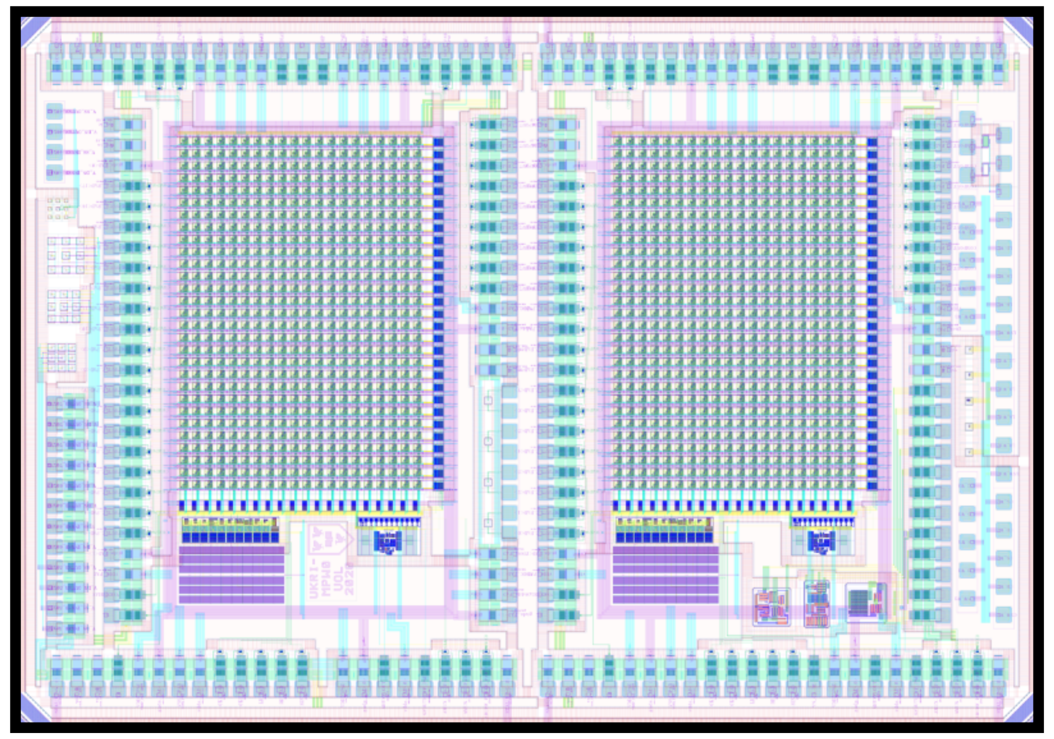
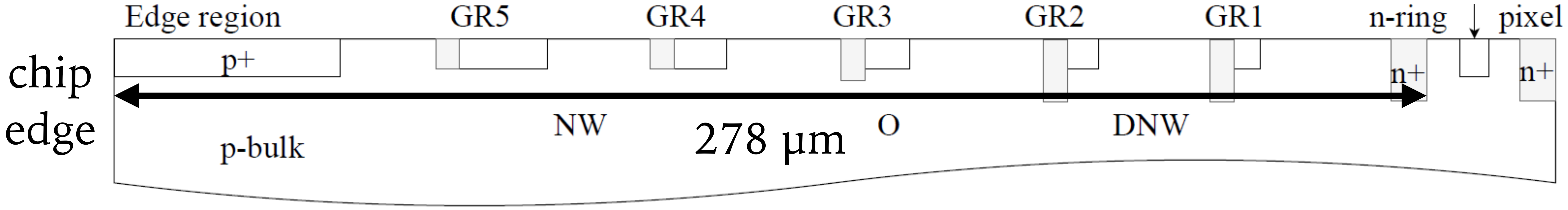
- Presented an HV-CMOS prototype UKRI-MPW0 in TWEPP-2023.
- It has two N-type chip rings -> high leakage current (~ mA) in those rings.

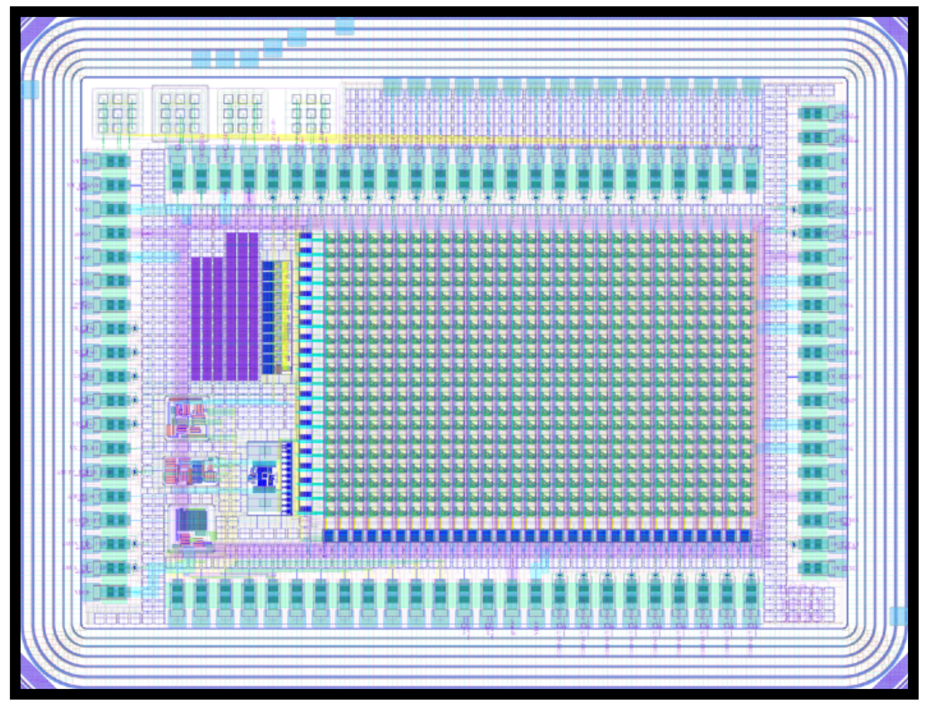





UKRI-MPW0

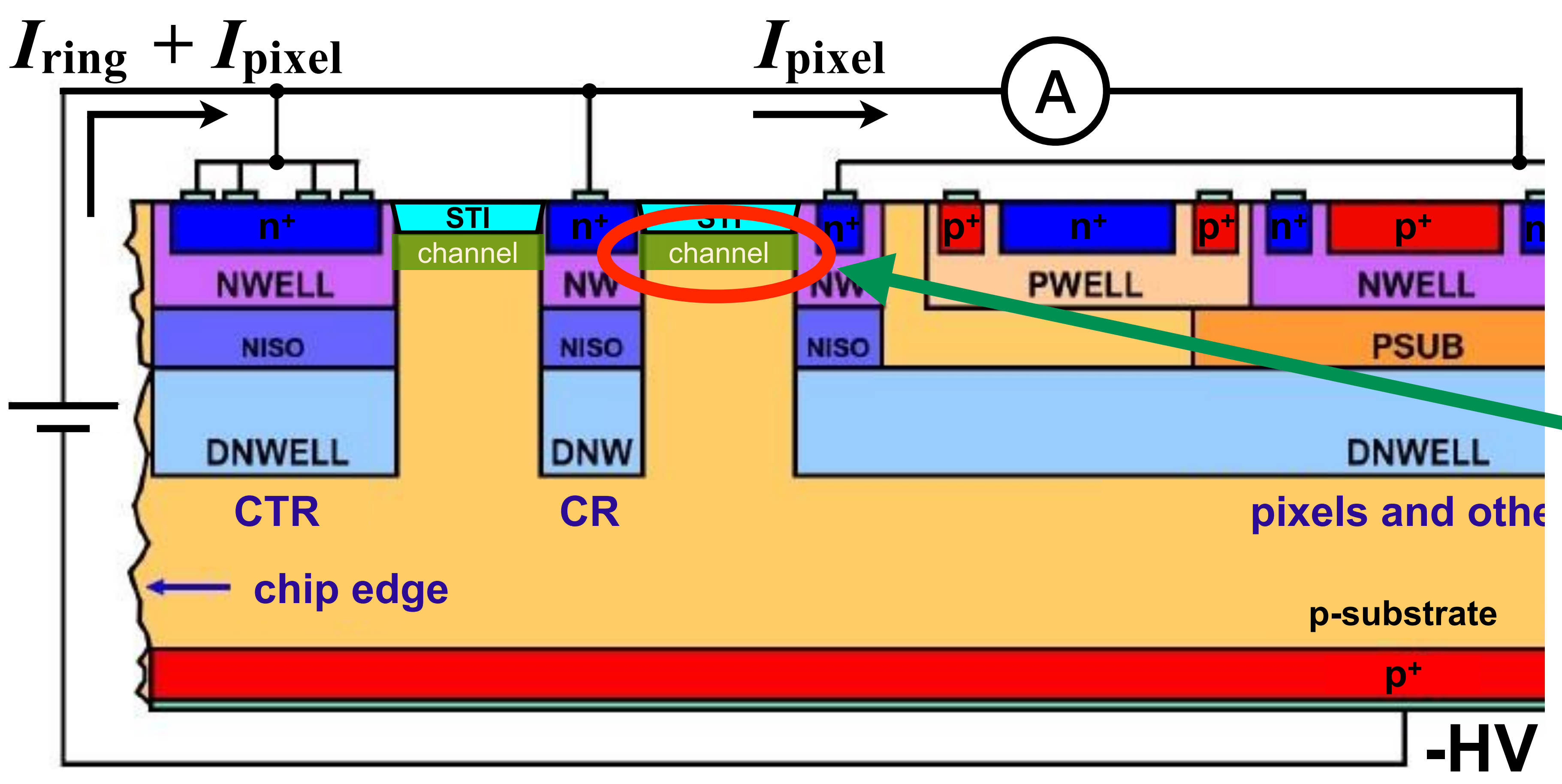
- UKRI-MPW1 employs the multiple P-type + N-type rings structure designed by Bonn for low leakage and high breakdown. (also used in RD50-MPW4)

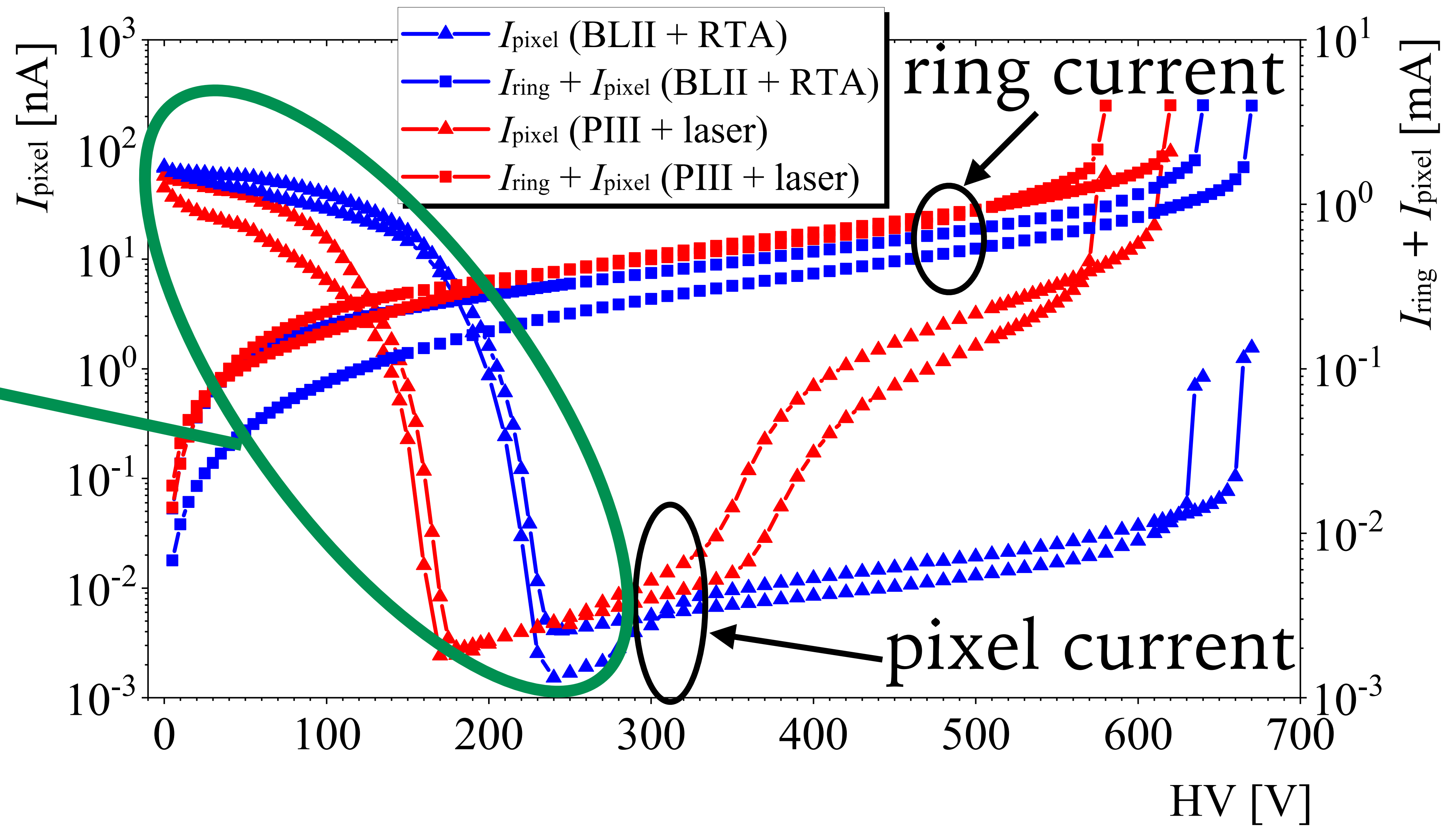


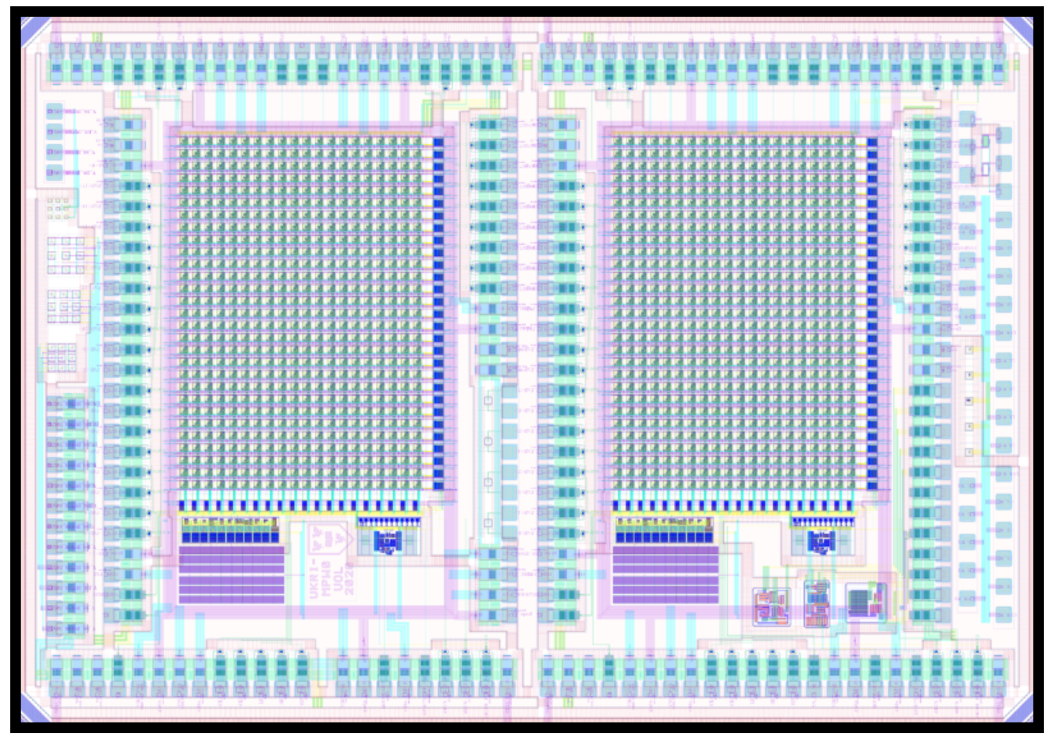

UKRI-MPW1

From UKRI-MPW0 to UKRI-MPW1

- UKRI-MPW0 has no P-type layer between pixel and ring -> parasitic channel under STI.

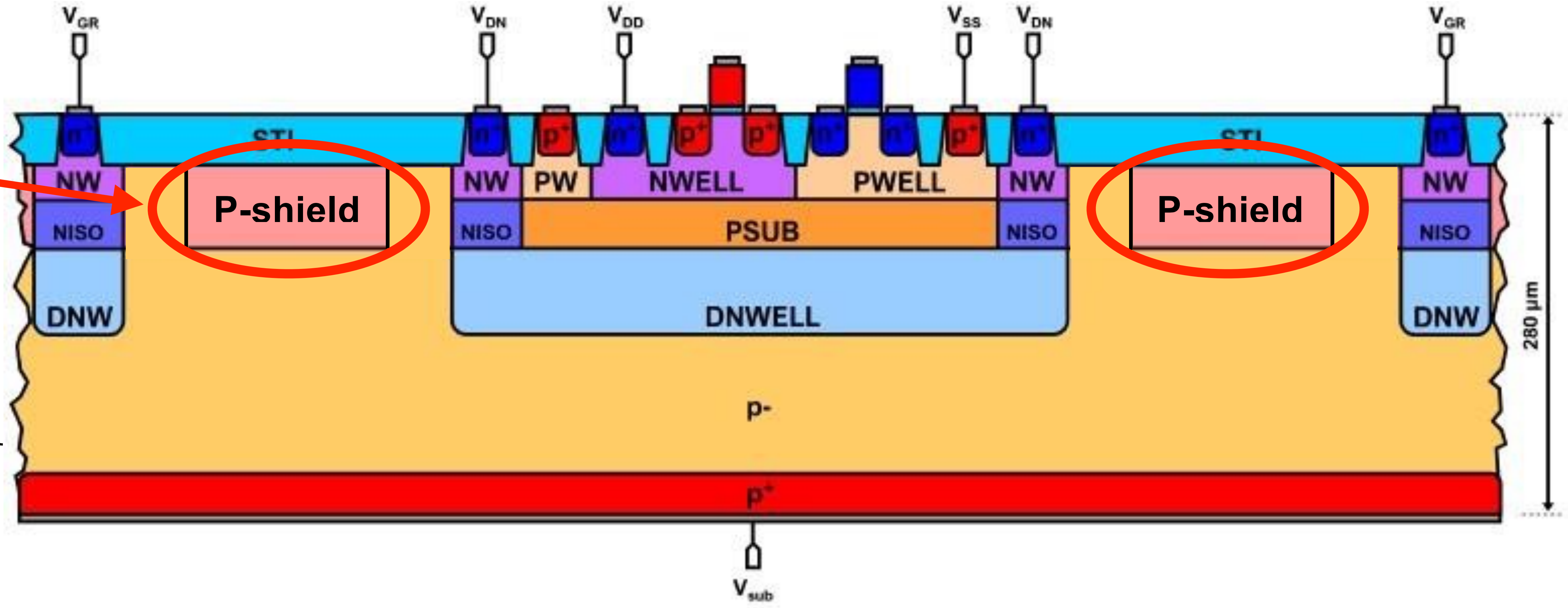


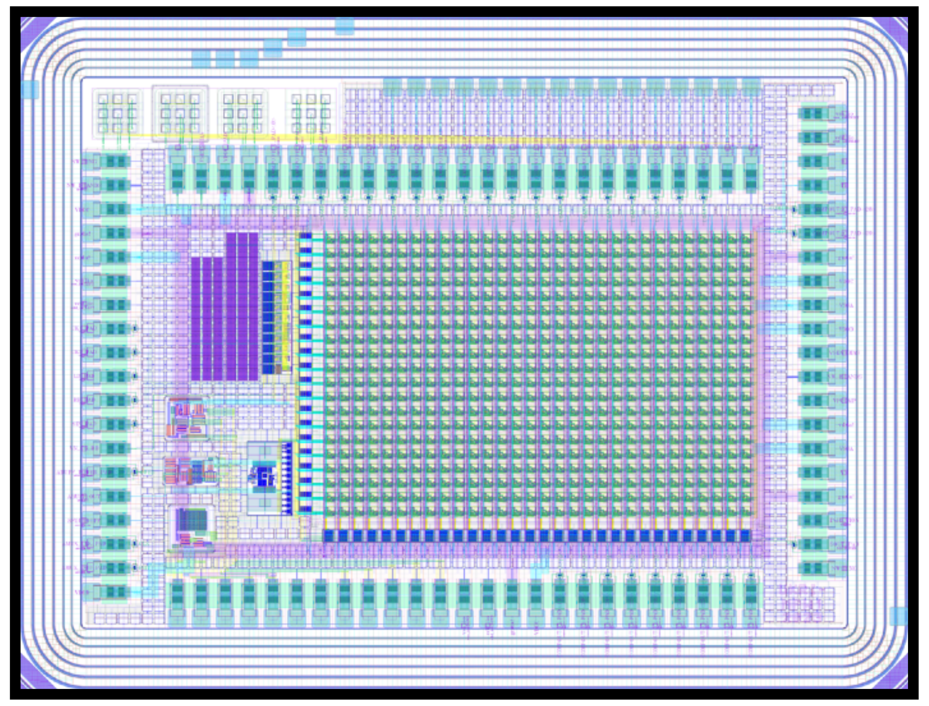




UKRI-MPW0

- UKRI-MPW1 adds customised low-doped P-type layers (P-shield) between pixel and ring to prevent the parasitic channel.
- To mimic p-spay in traditional hybrid sensors

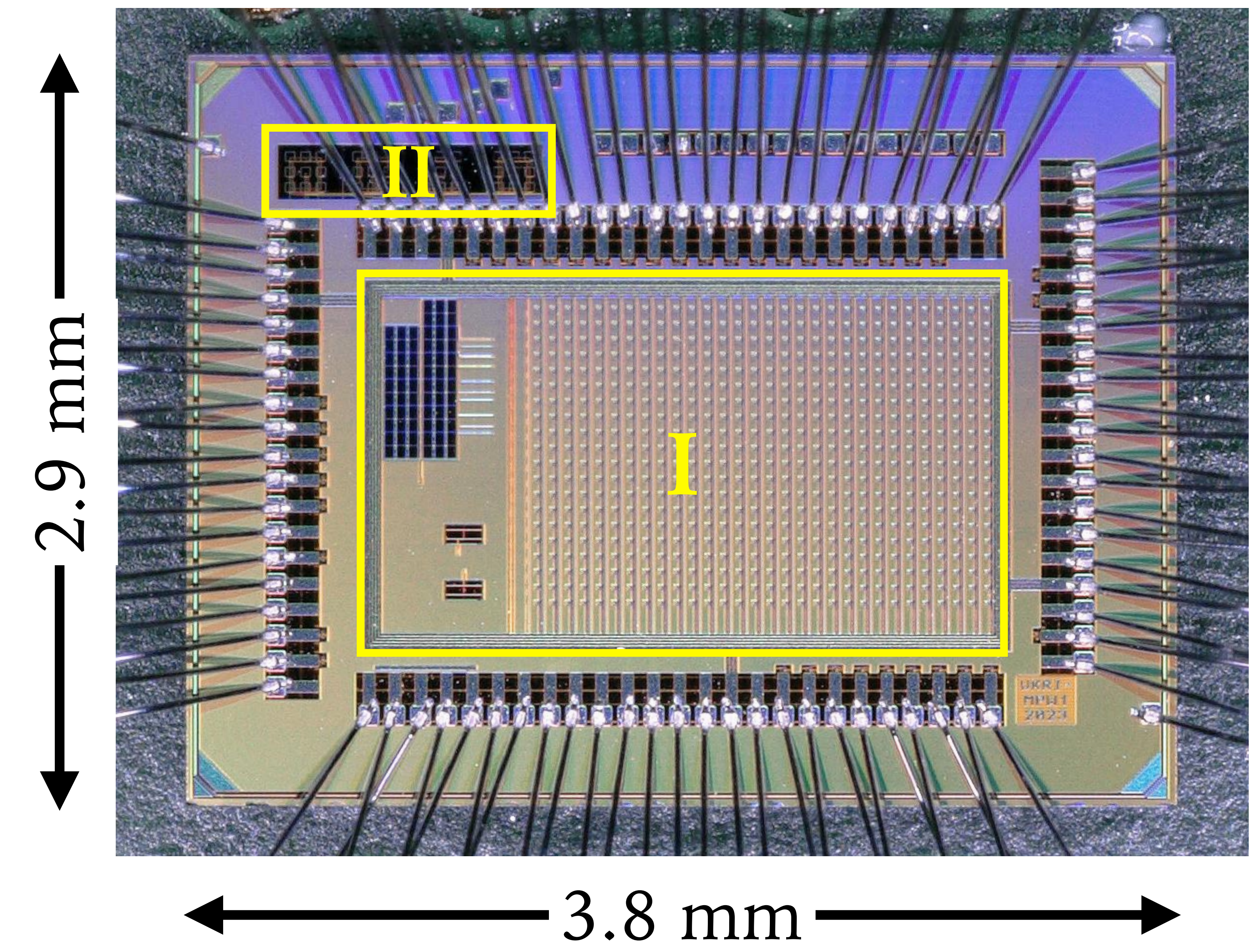


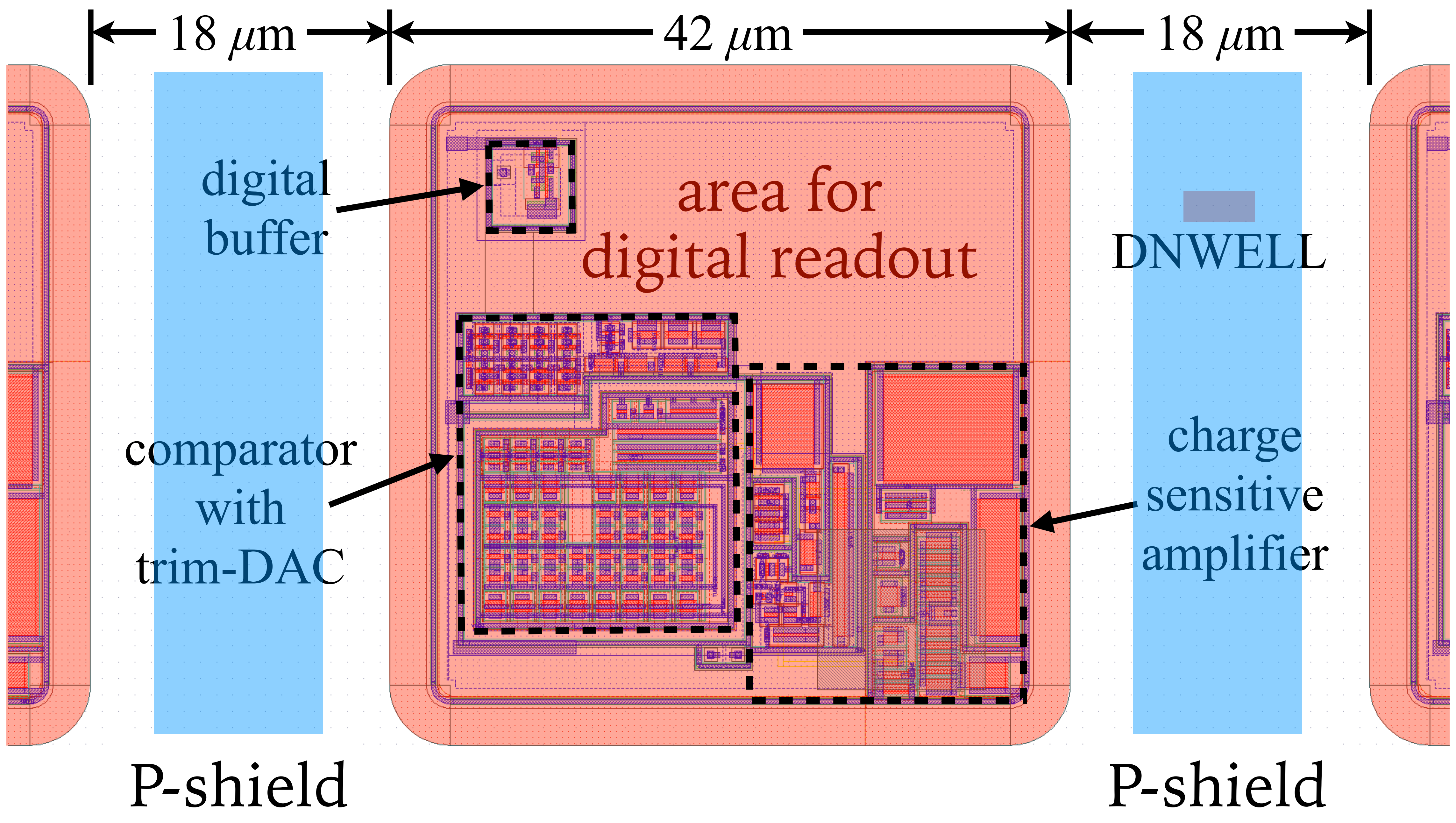


UKRI-MPW1

UKRI–MPW1 more details

- High resistivity (3 kΩ·cm) wafers, thinned to 280 μm.
- Backside processed using Beam-Line Ion Implantation and Rapid Thermal Annealing.
- I. A pixel matrix of 20 rows and 30 columns (60 μm × 60 μm pixel) and test structures are included in the chip
- II. Test structures for I-V and Edge-TCT.

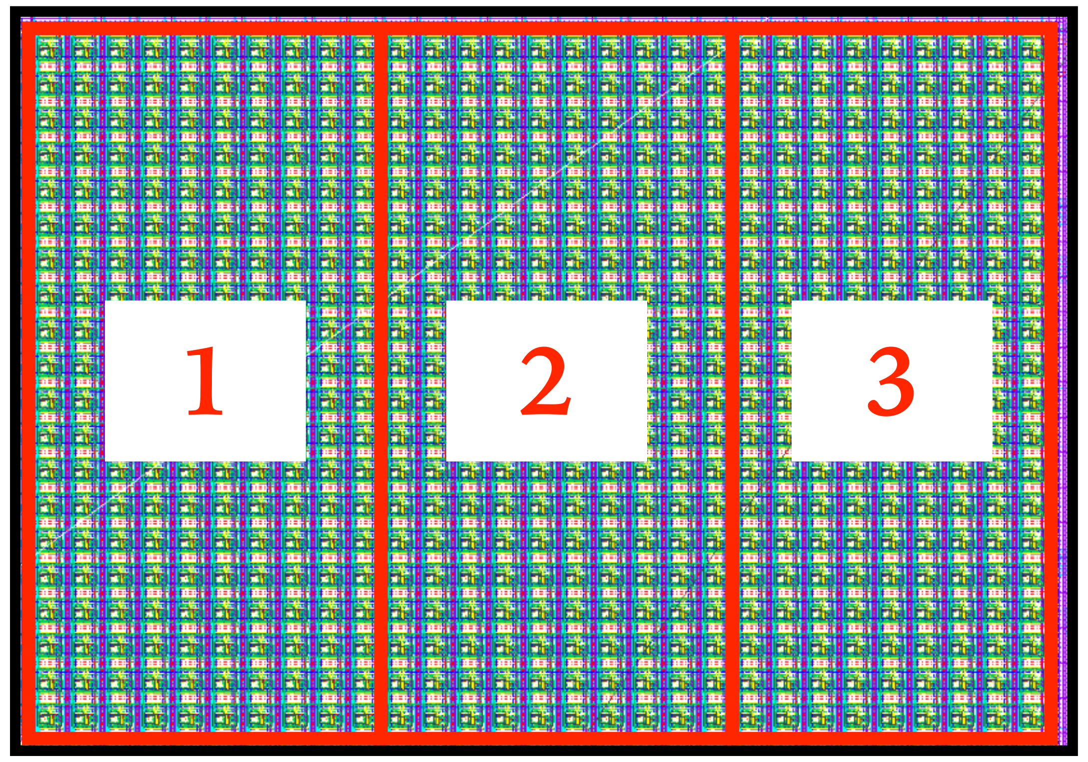


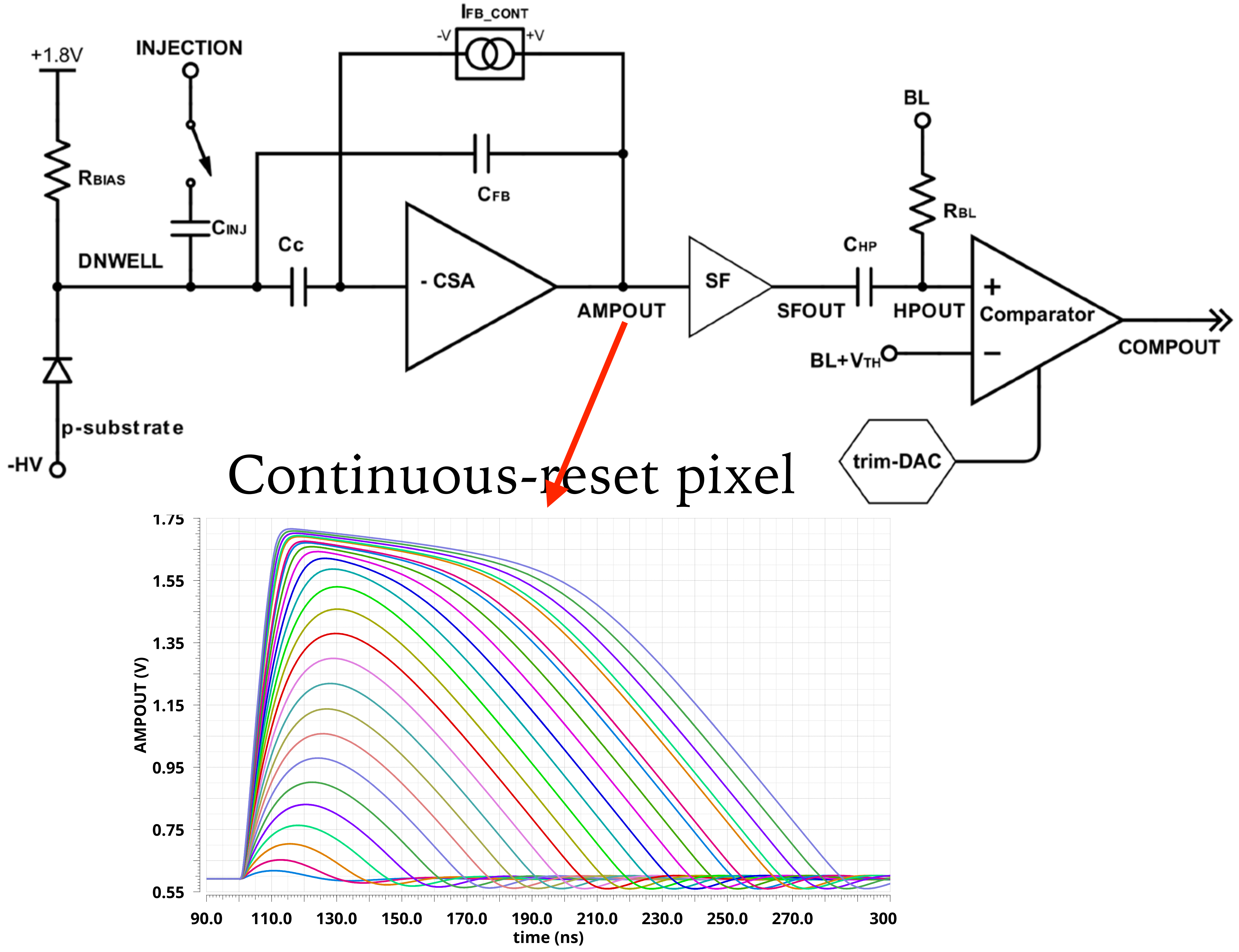


- Each pixel has a Charge Sensitive Amplifier (CSA), a comparator with trim-DAC.
- A buffer to send out comparator output signal.

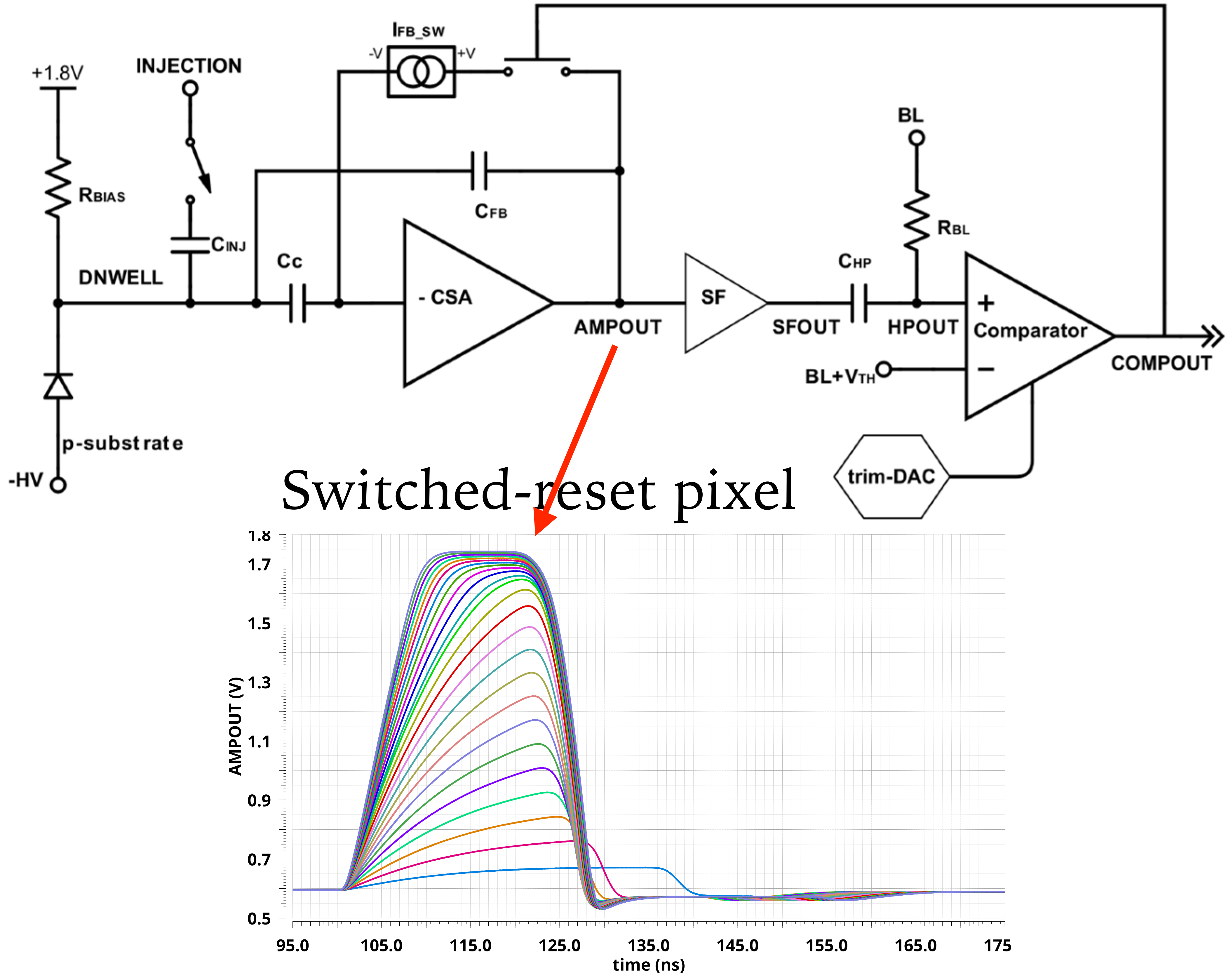
Pixel matrix

- Three pixel flavours (flavours 1. and 3. have been implemented in UKRI-MPW0):
  1. Continuous-reset pixel with PMOS trim-DAC
  2. Continuous-reset pixel with NMOS trim-DAC
  3. Switched-reset pixel with PMOS trim-DAC
- NMOS trim-DAC needs less PSUB -> less parasitic capacitance (75 fF less).





Continuous-reset pixel



Switched-reset pixel

Pixel matrix

- Three pixel flavours (flavours 1. and 3. have been implemented in UKRI-MPW0):
  1. Continuous-reset pixel with PMOS trim-DAC
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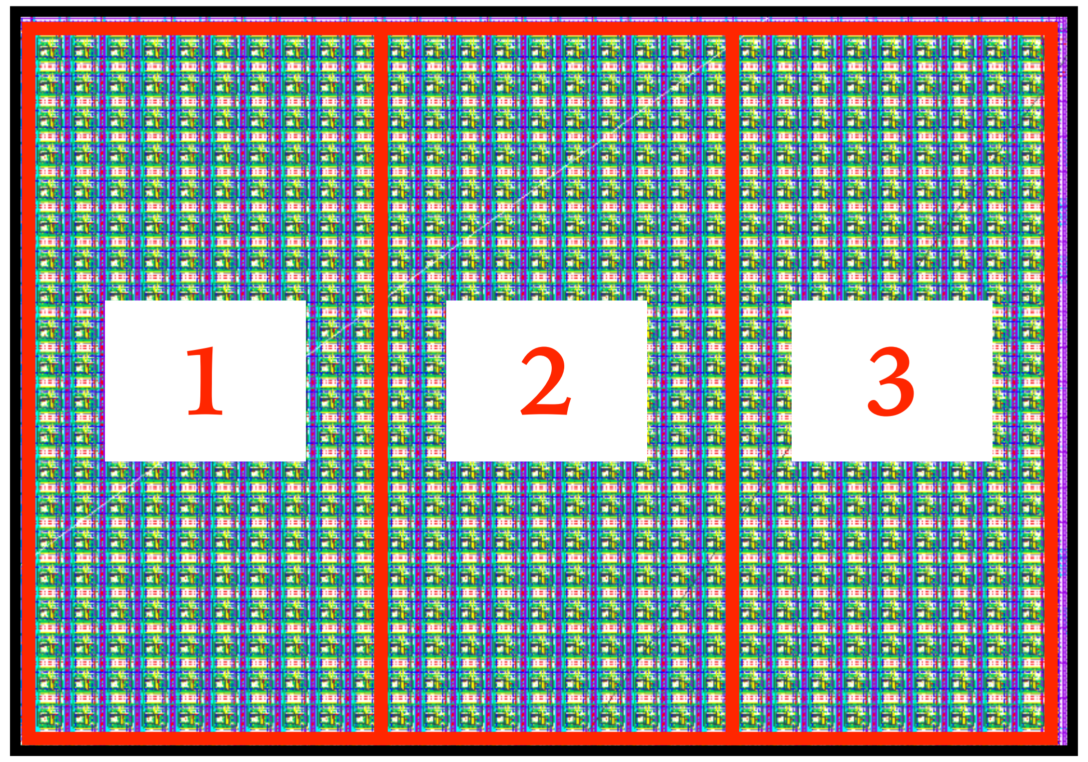
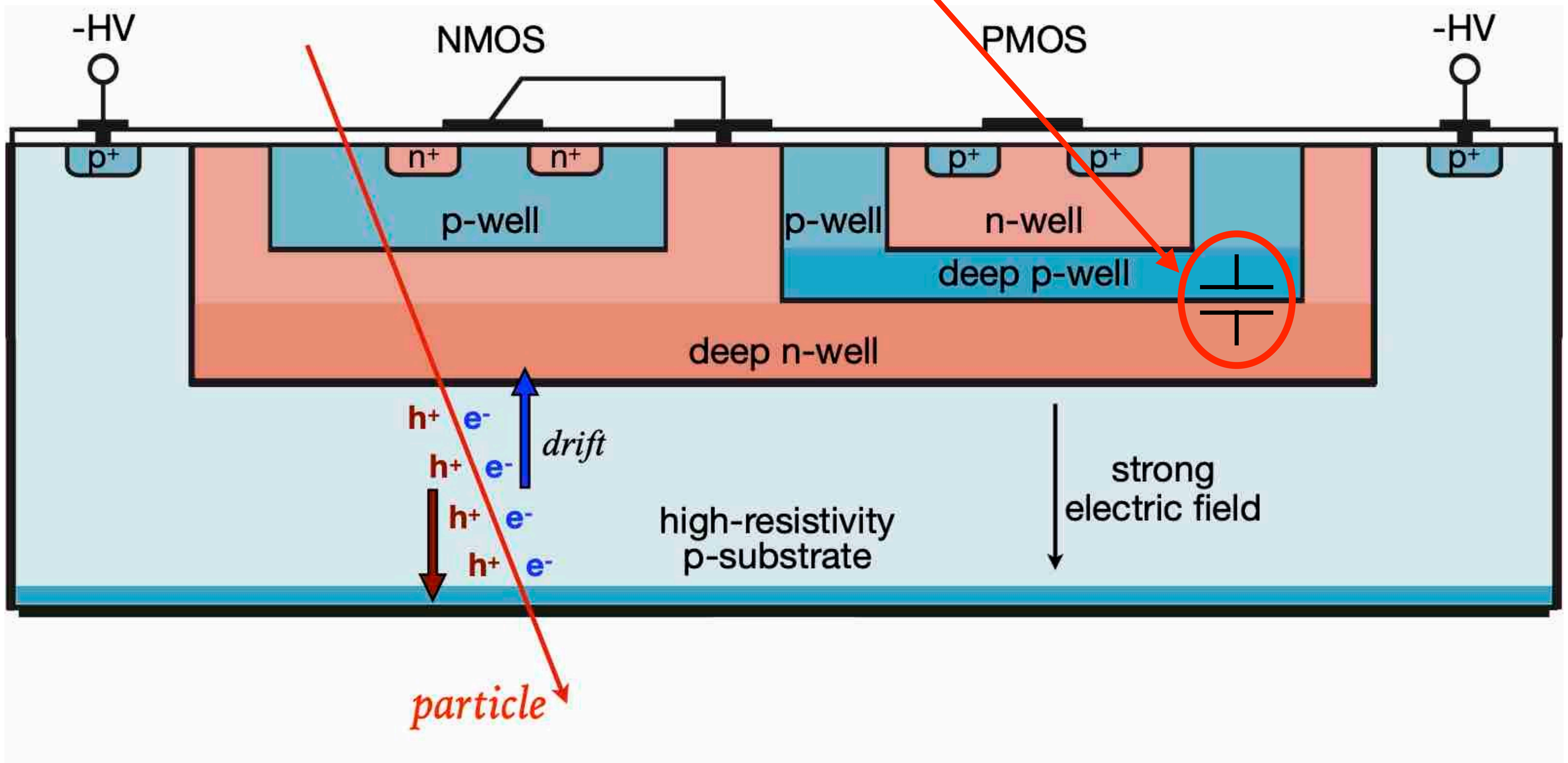
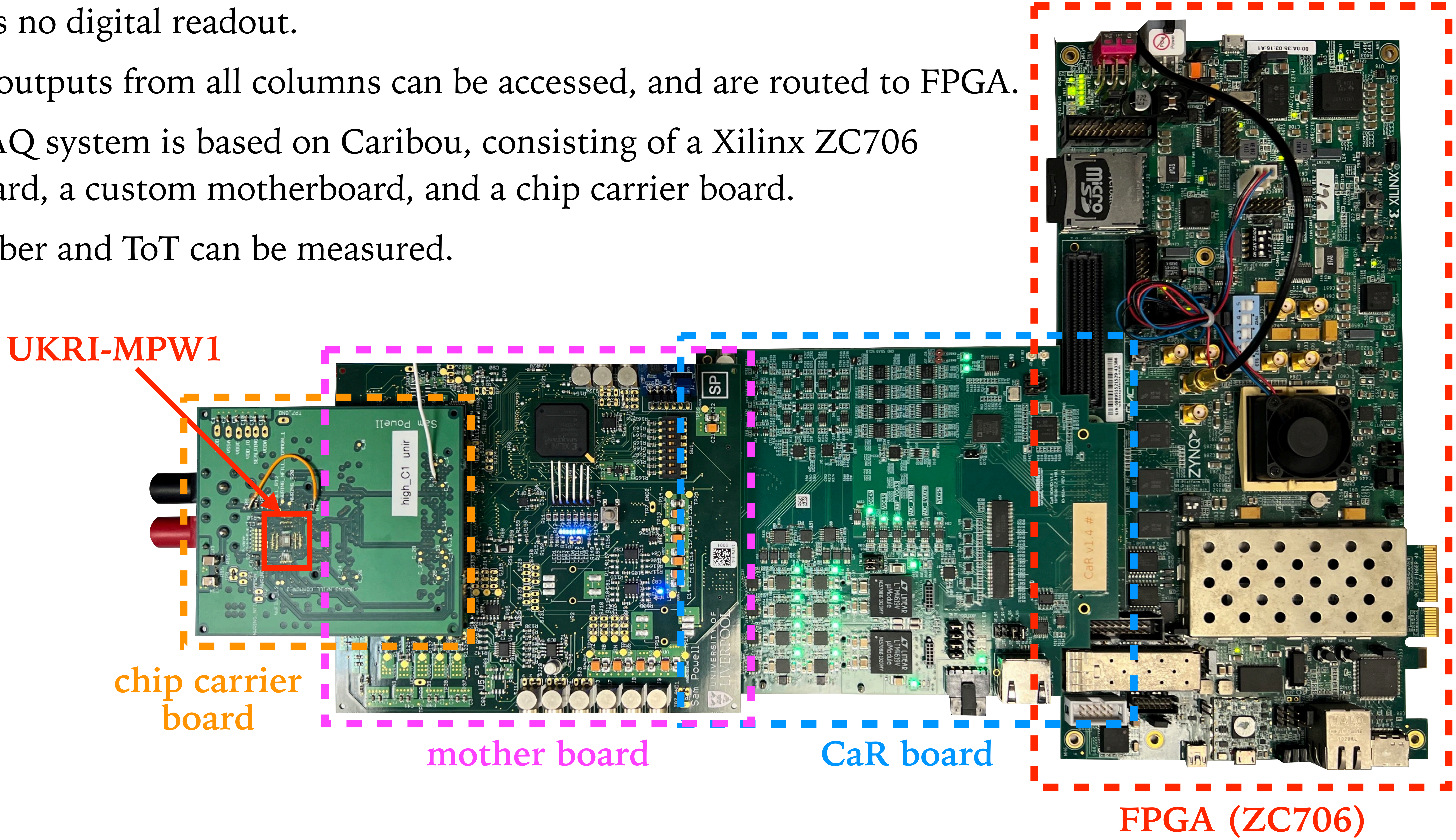




Readout and DAQ

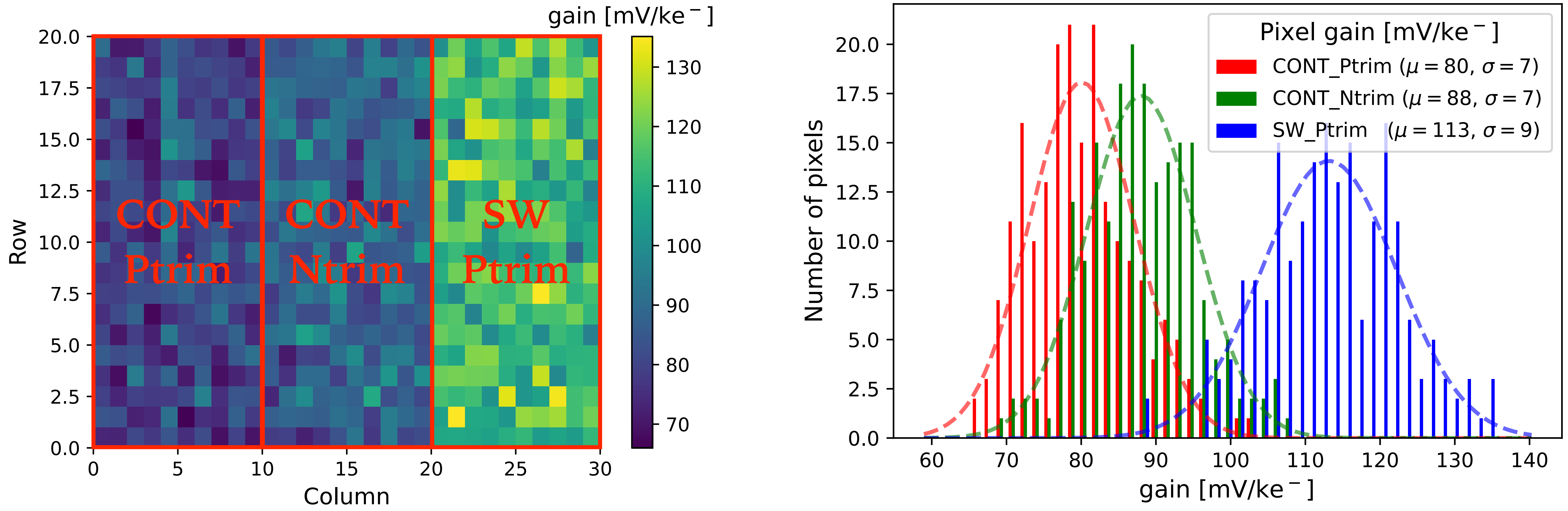
- UKRI-MPW1 has no digital readout.
- The comparator outputs from all columns can be accessed, and are routed to FPGA.
- UKRI-MPW1 DAQ system is based on Caribou, consisting of a Xilinx ZC706 FPGA, a CaR board, a custom motherboard, and a chip carrier board.
- S-curve, hit number and ToT can be measured.



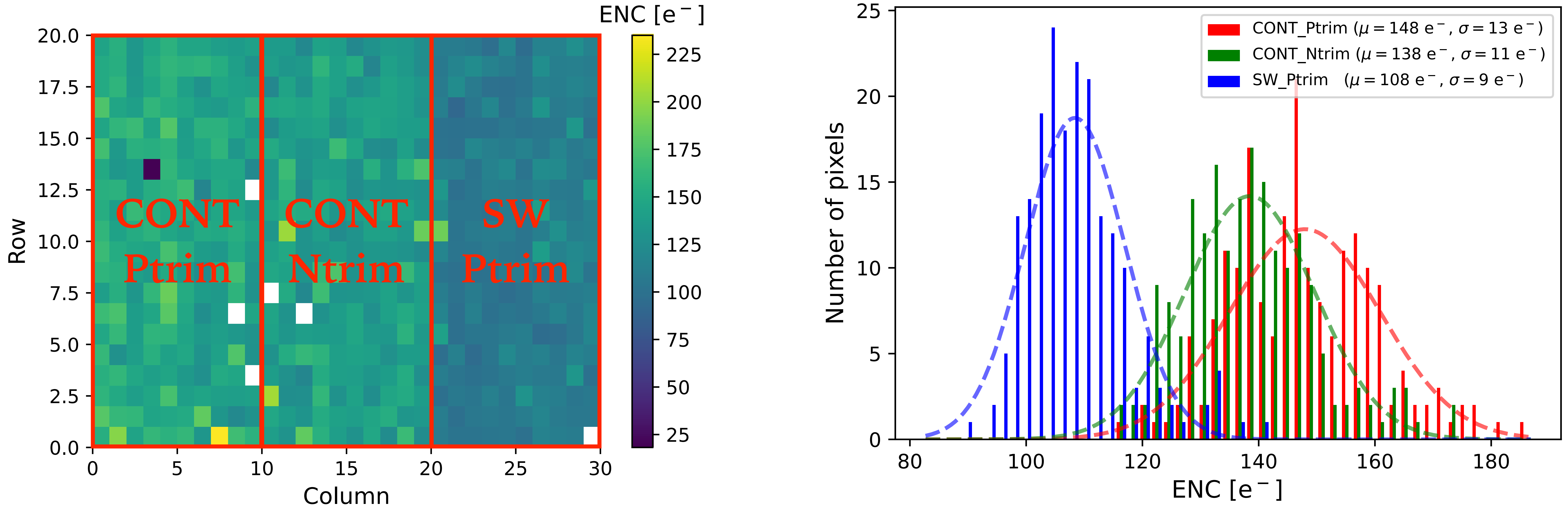
Pixel characterisation

- Pixel performance is measured using S-curve scans.
- Switched-reset pixels have higher gain and lower noise, due to lower feedback current.
- Pixels with NMOS trimDAC have higher gain, thus lower ENC.

pixel gain

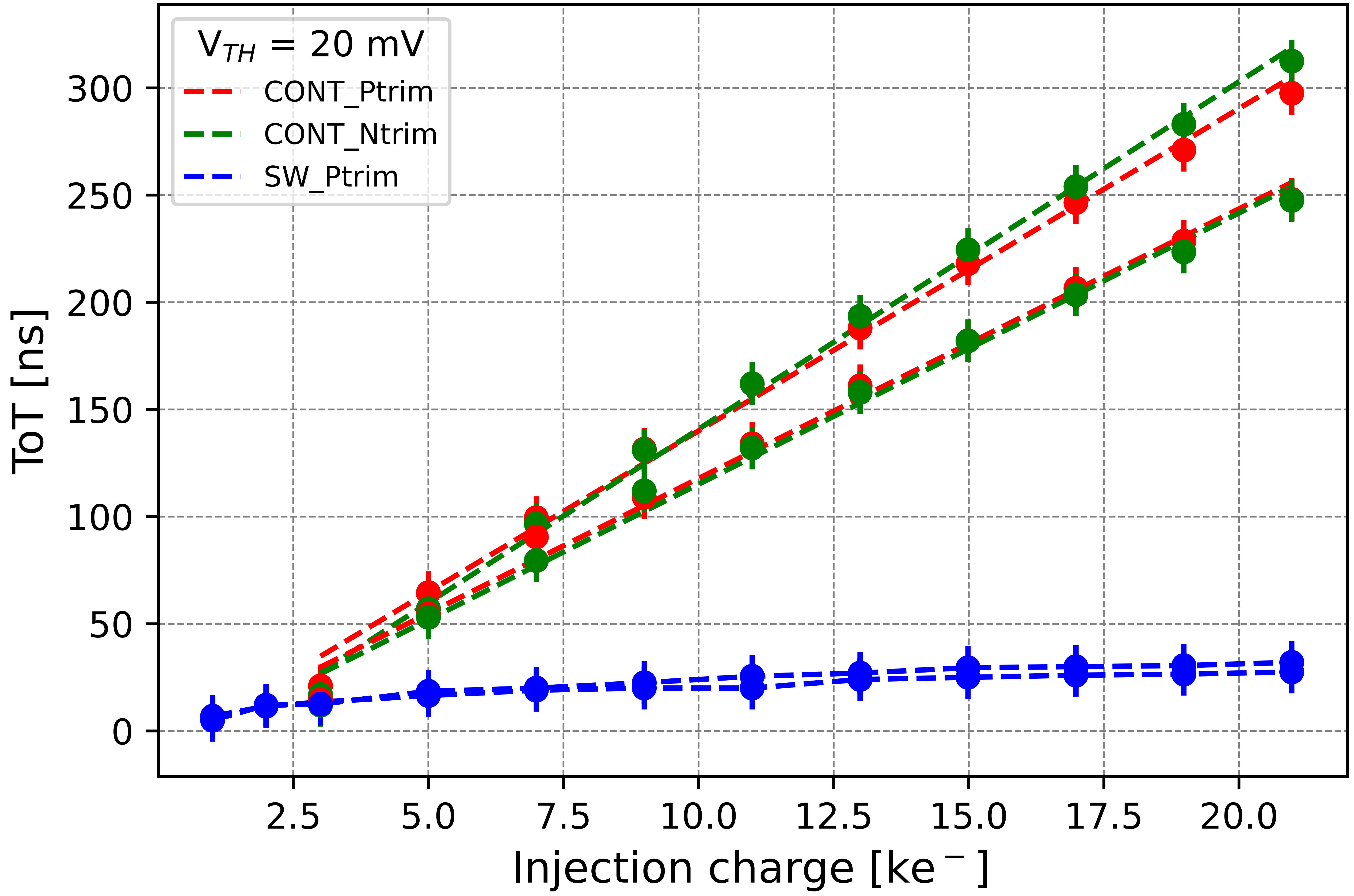


pixel noise



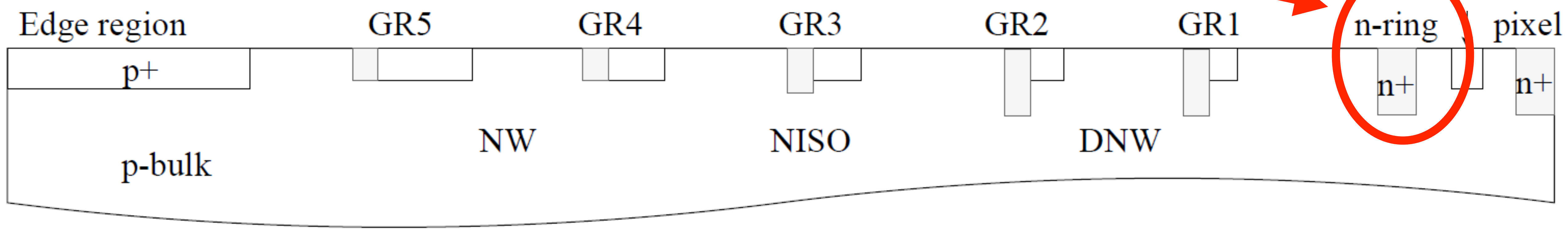
Pixel characterisation

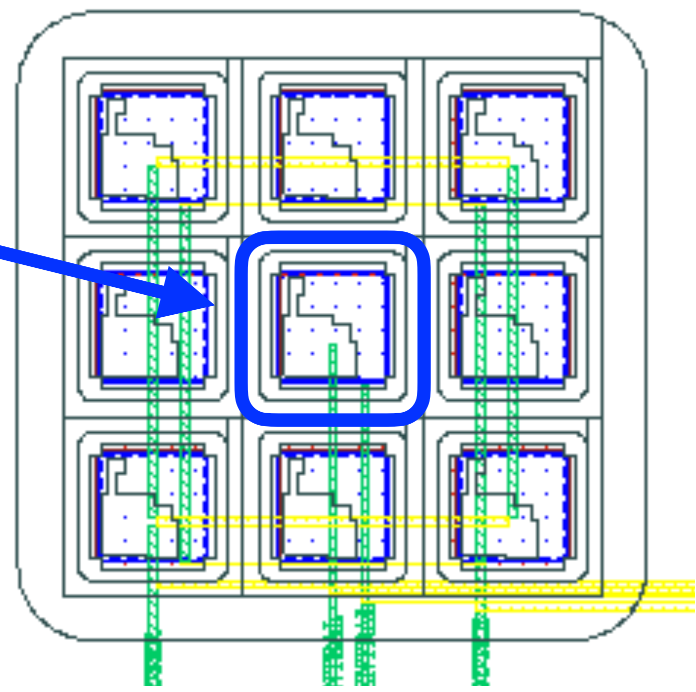
- ToT for different injection charges.
- Continuous-reset pixels have linear ToT with respect to charge.
- Switched-reset pixels have ToT always below 50 ns.

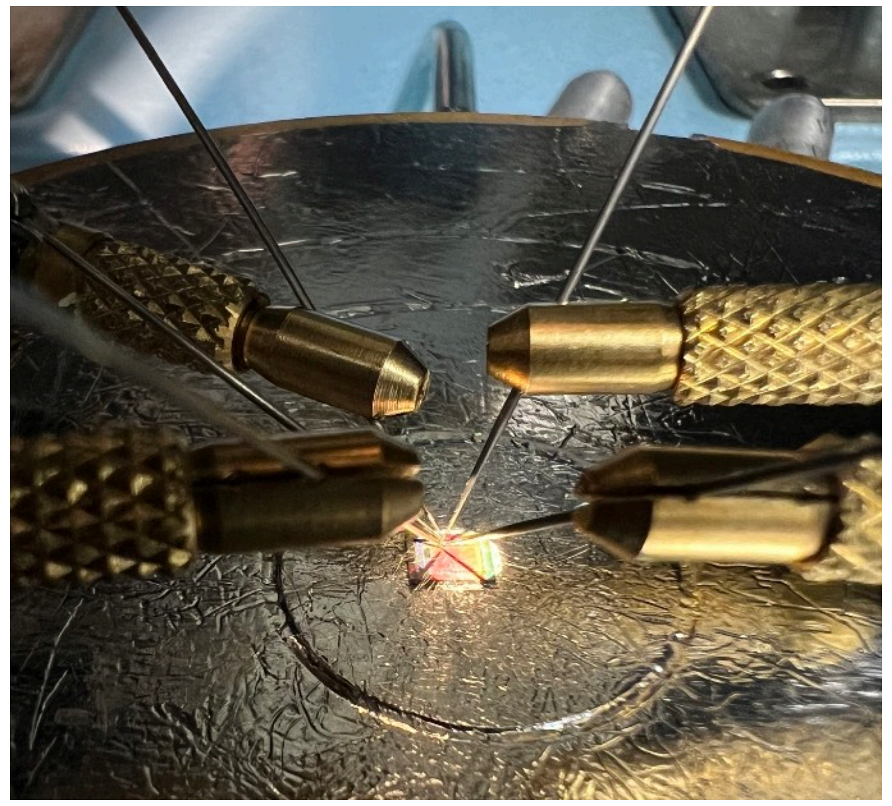


I-V of test structure

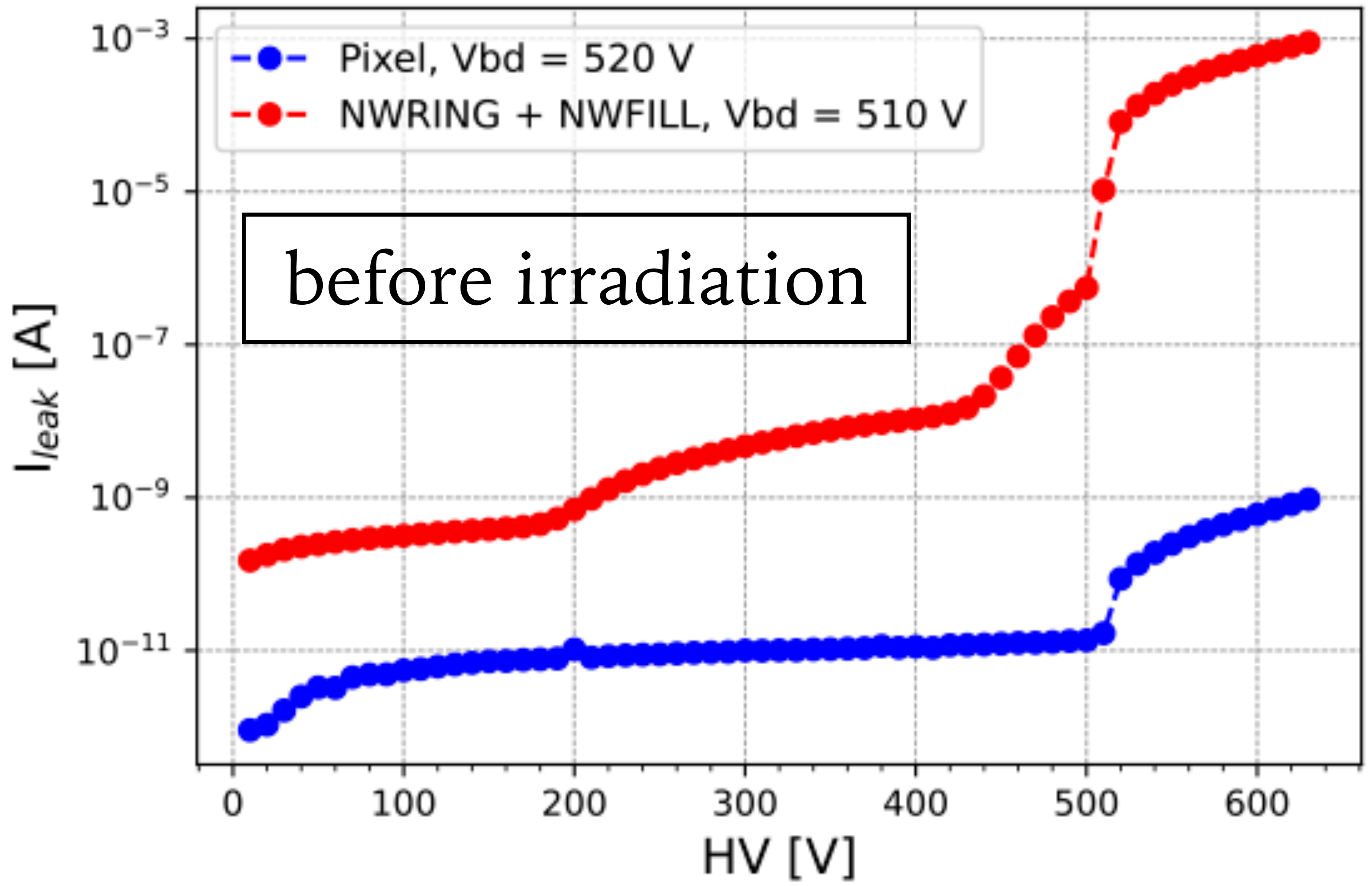
- Measure the leakage currents from N-type ring and inner pixel from the test structure on probe station with no cooling.

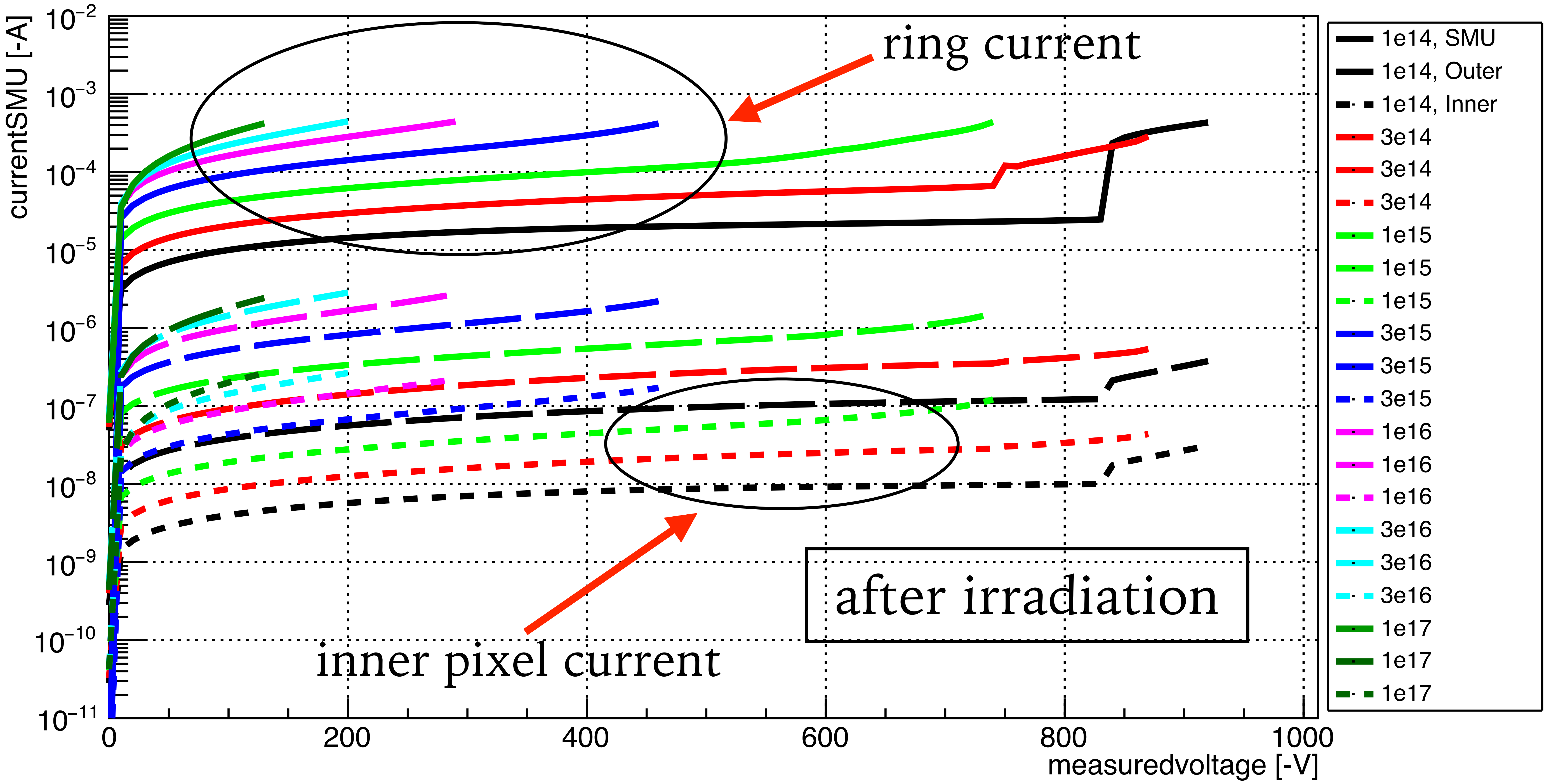






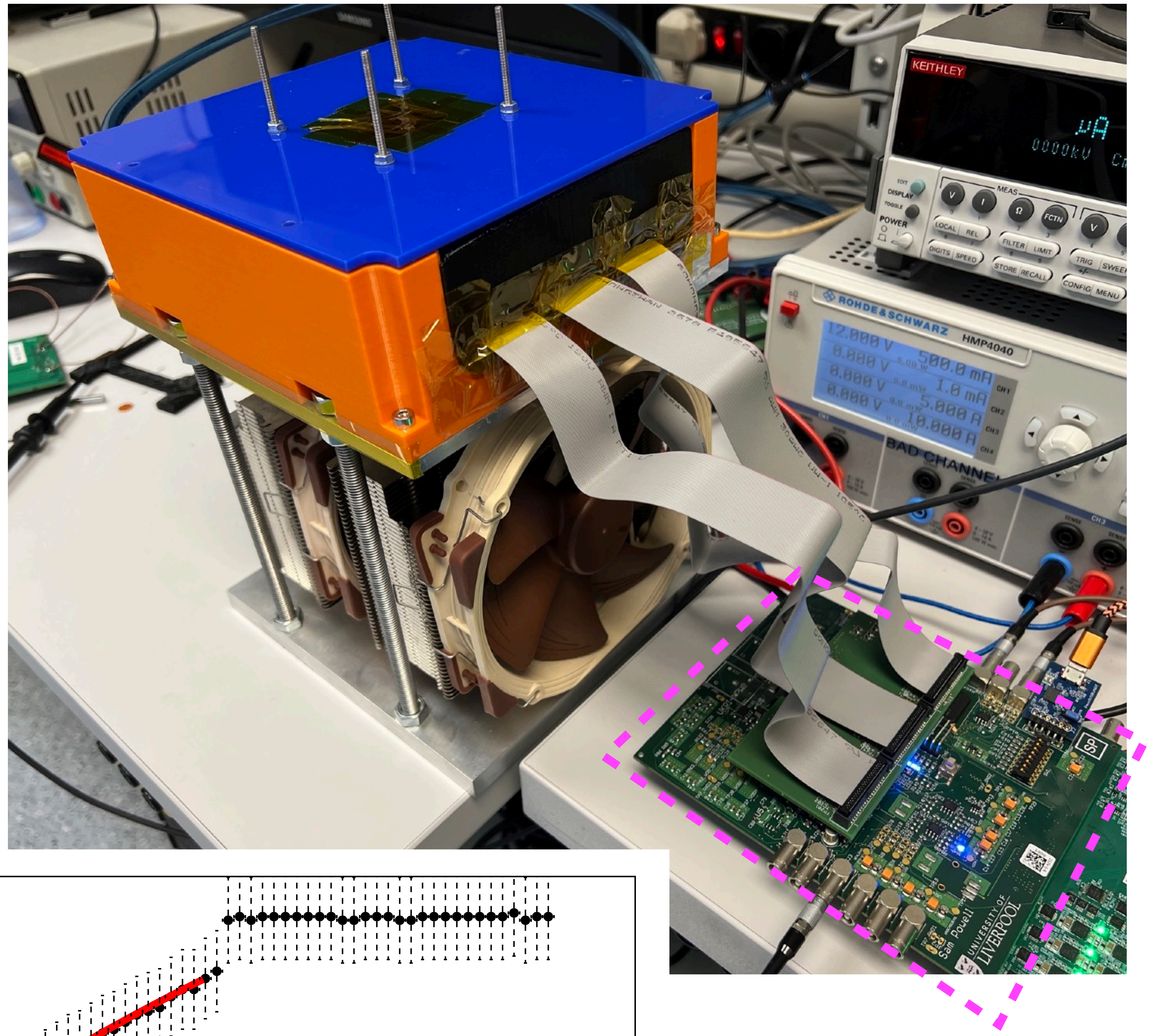
- Samples have been irradiated with neutron to different fluences.
- Higher leakage current. Reach compliance at larger bias voltages for low fluences.



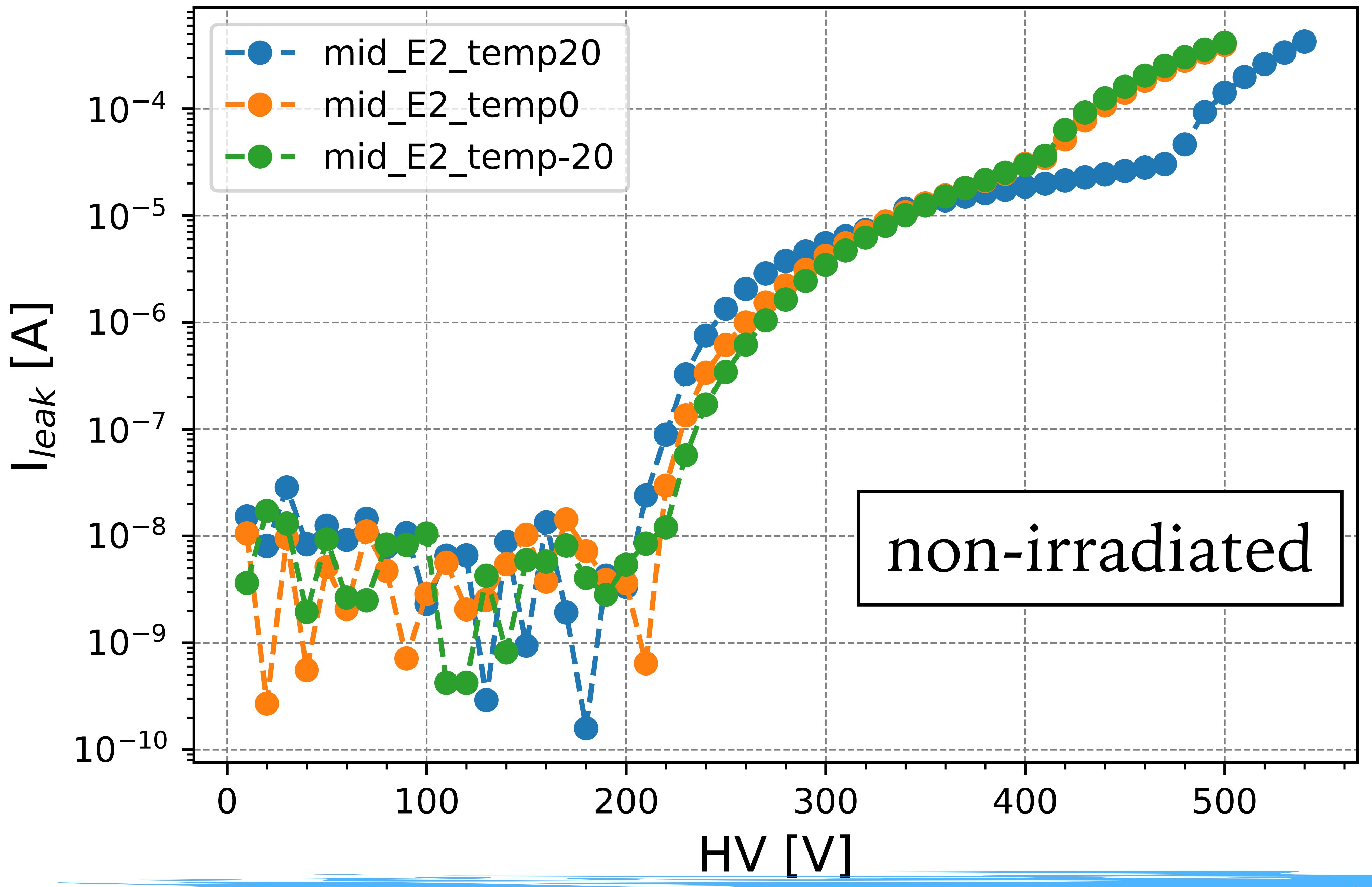


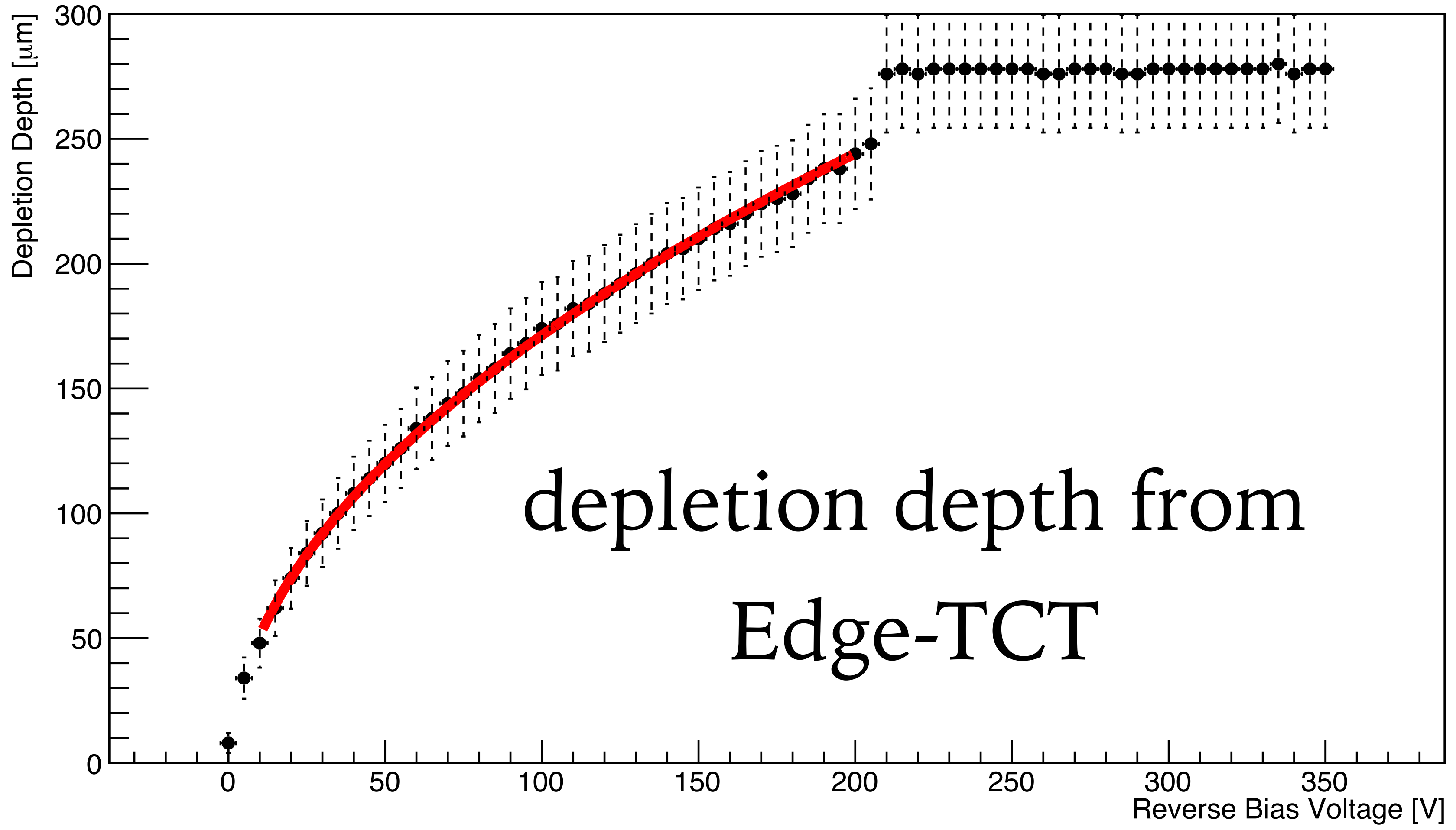
IV with cooling

- Peltier cooler based cooling setup.
- 3D printed cooling box filled with nitrogen.
- Ribbon cable to connect mother board and chip carrier board.
- Measure leakage current of the whole chip when configured.
- Leakage current jumps around 200 V, where chip fully depletes.
- Still trying to understand the mechanism behind the jump. (edge defects? related with backside processing?)



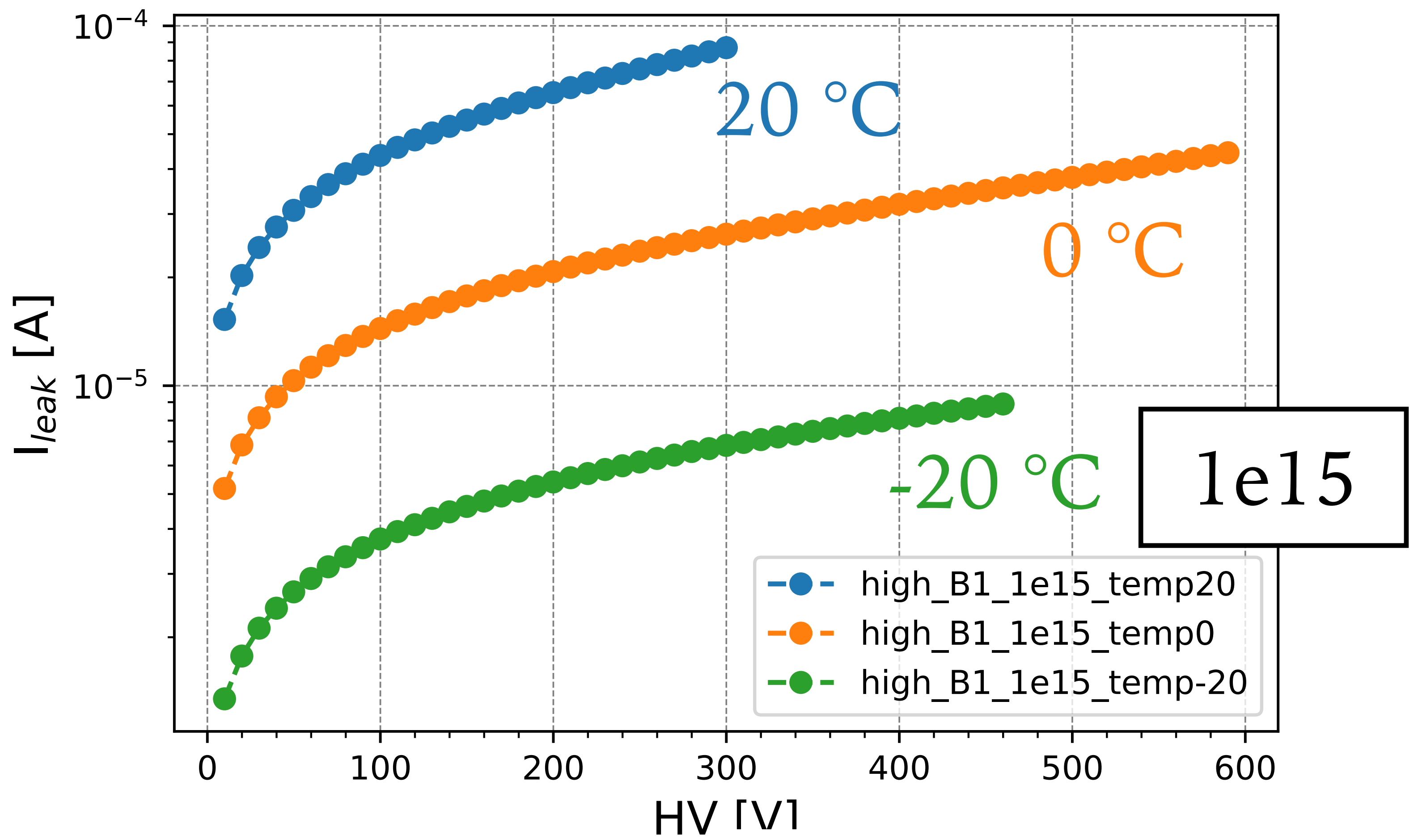
mother board

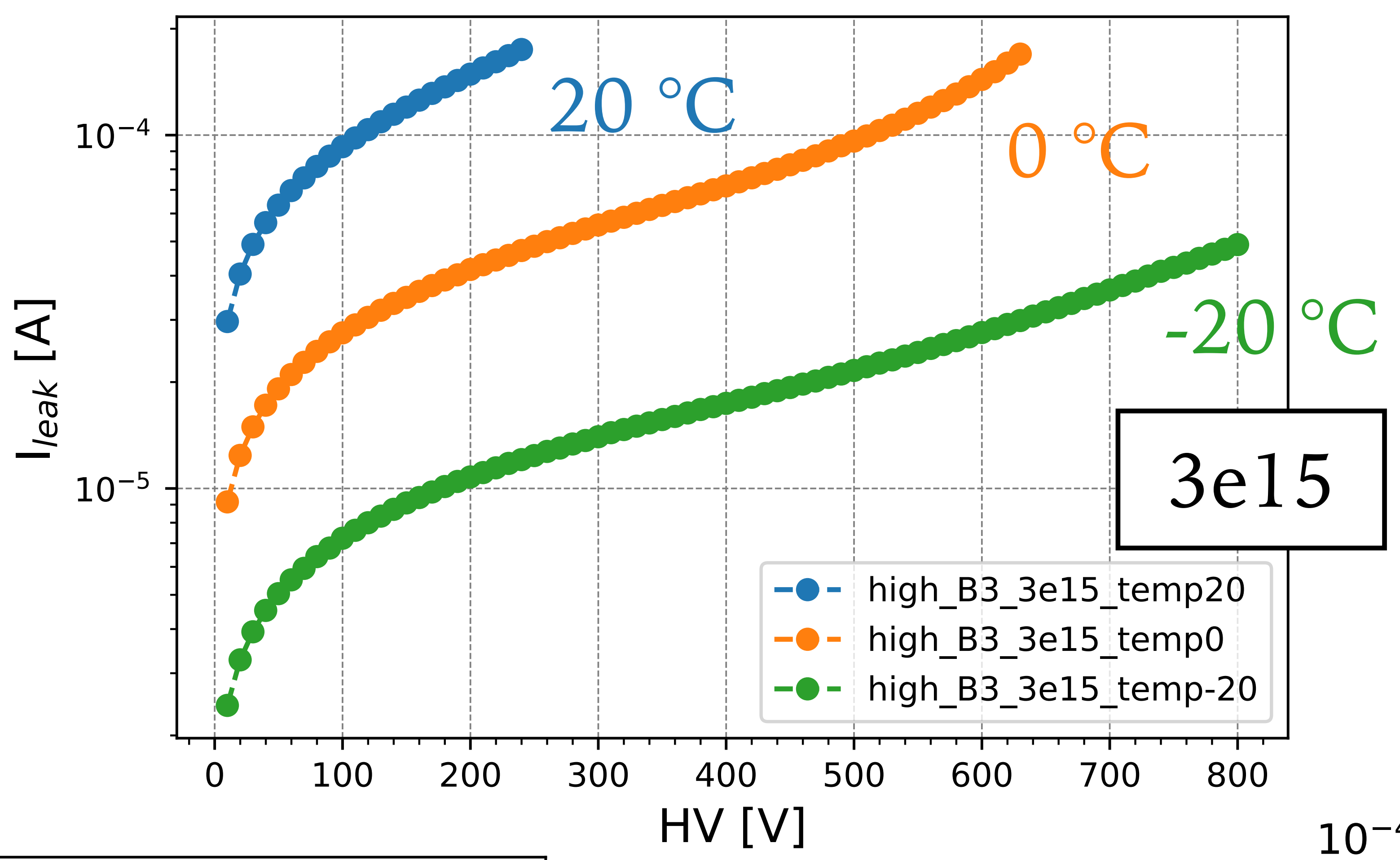


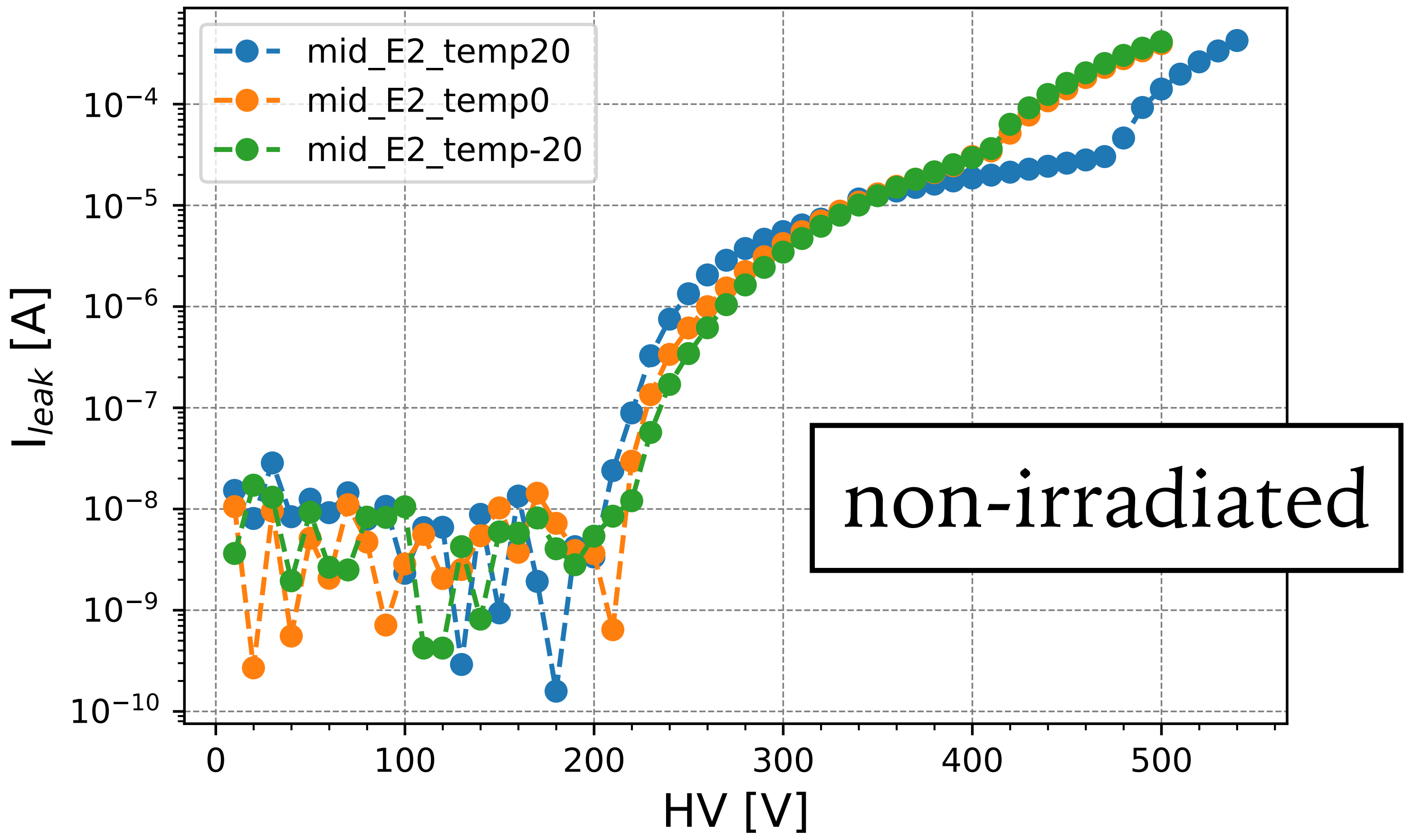


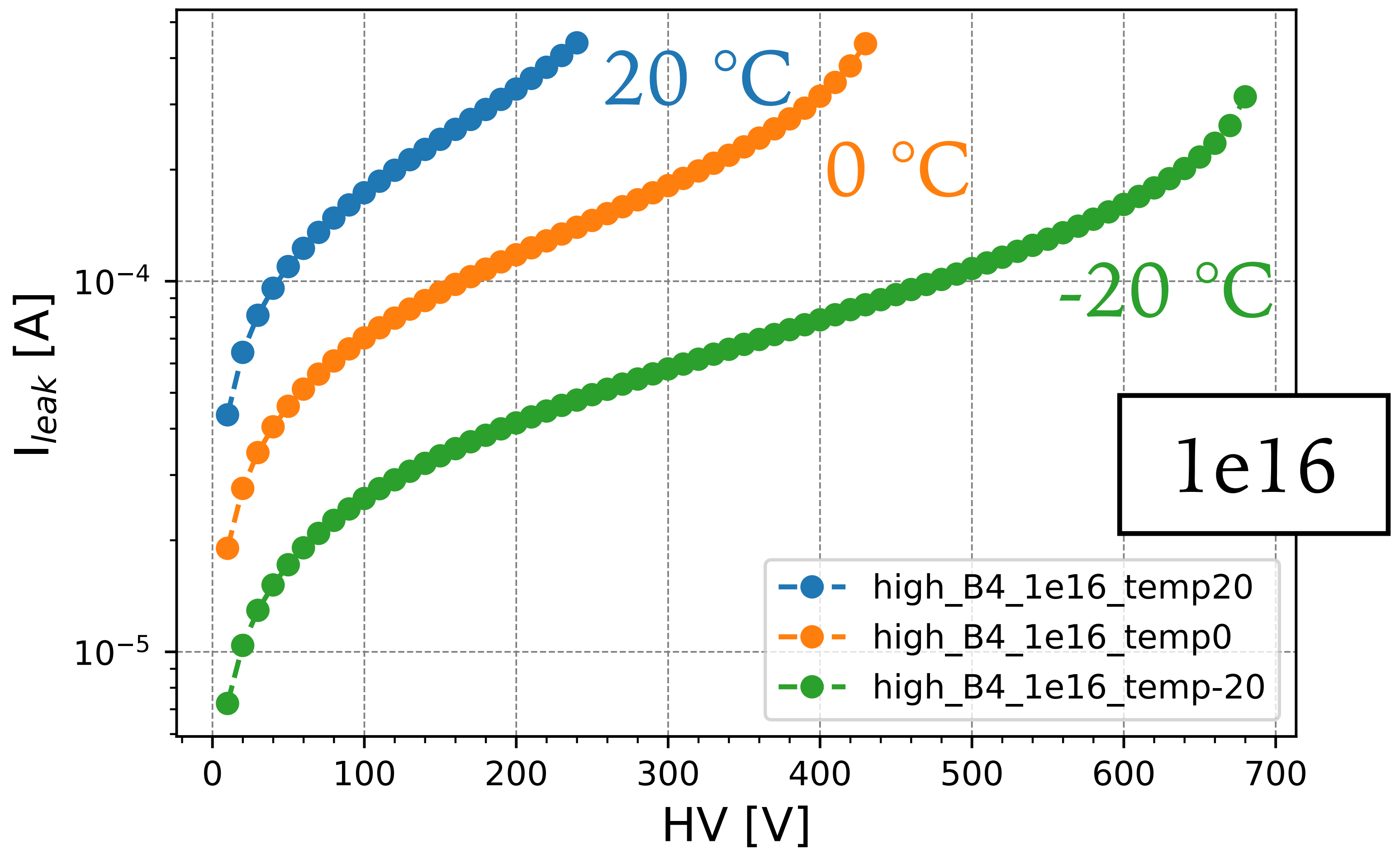
IV with cooling

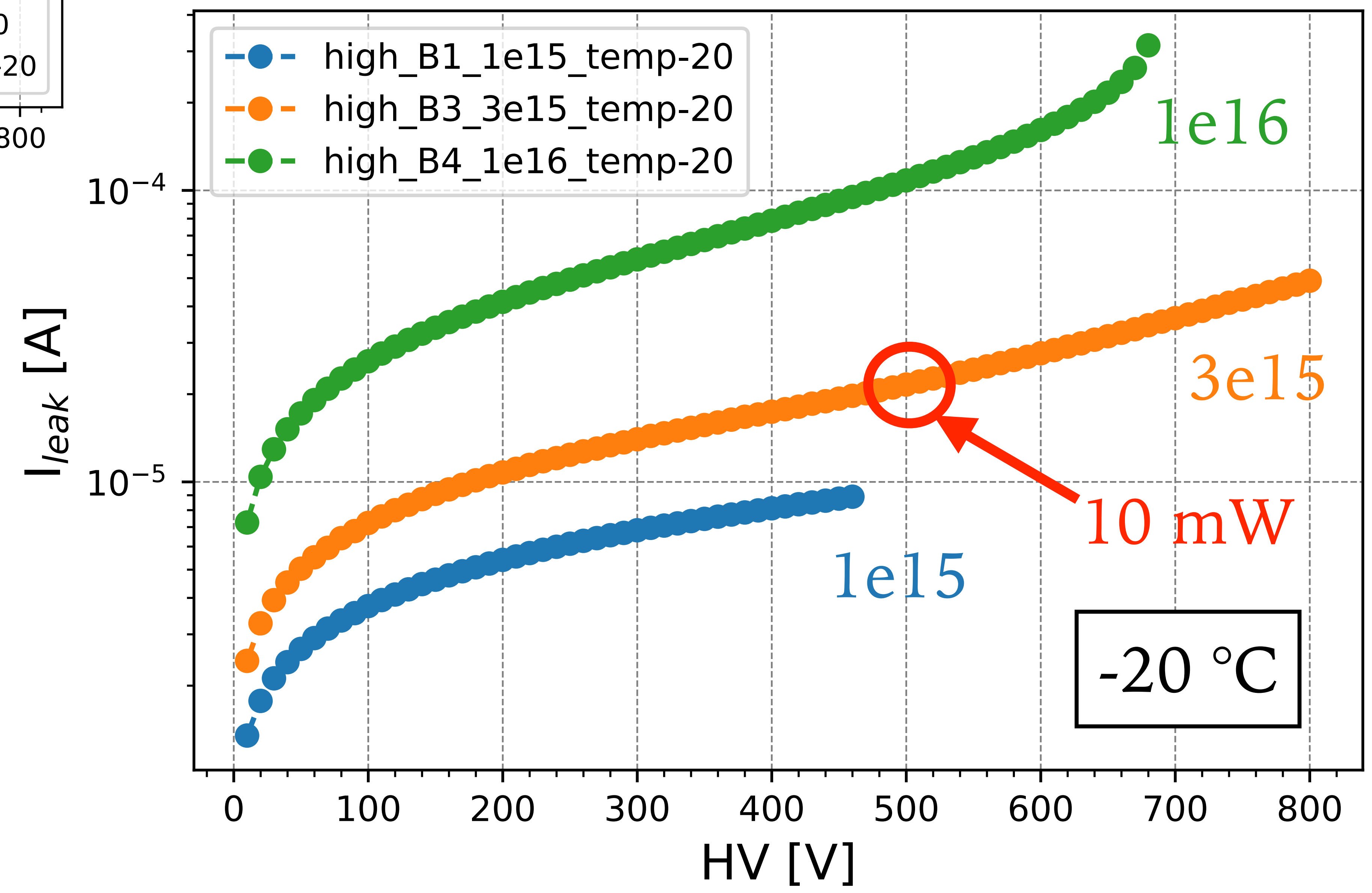
- Leakage currents of irradiated samples.
- No current jump at 200 V -> reach compliance at larger voltages.
- Had to use lower compliance to avoid destroying chips with HV > 800 V.





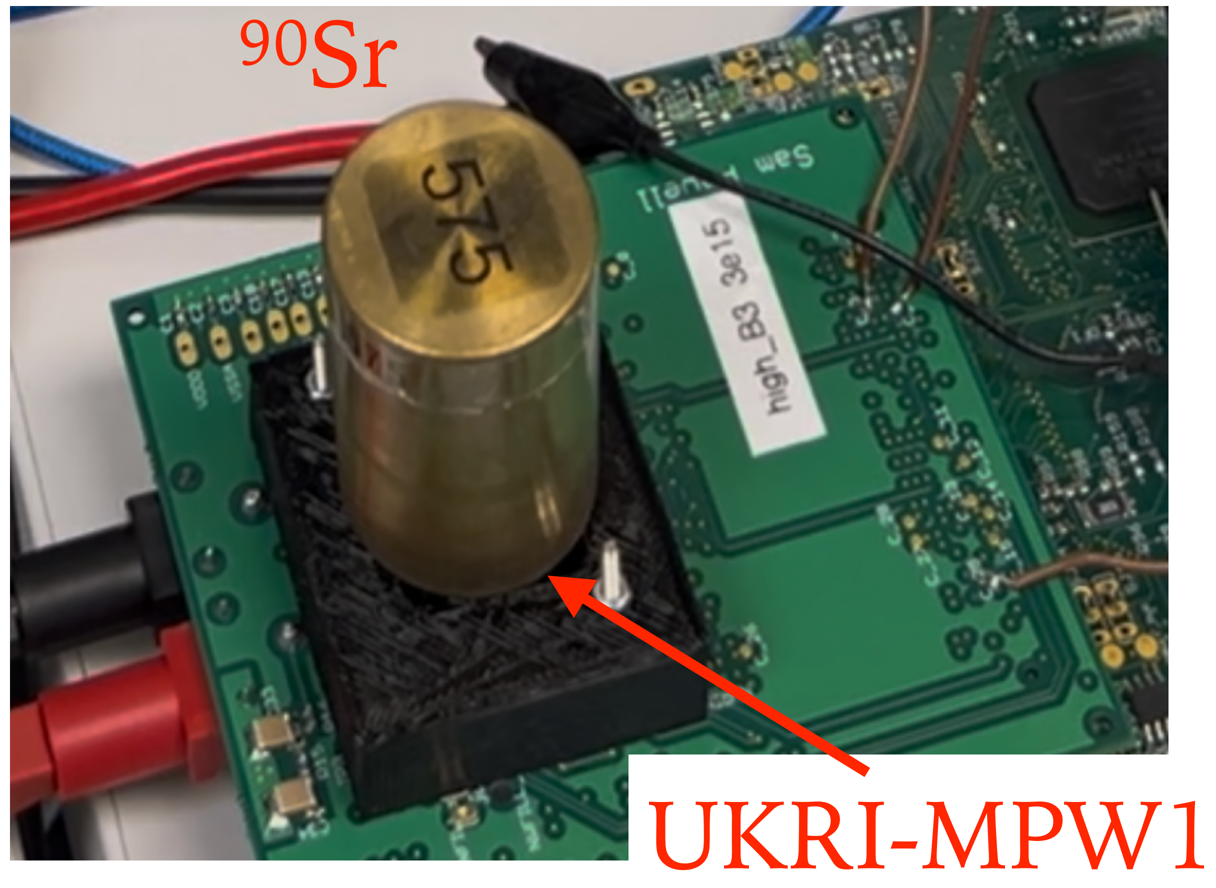


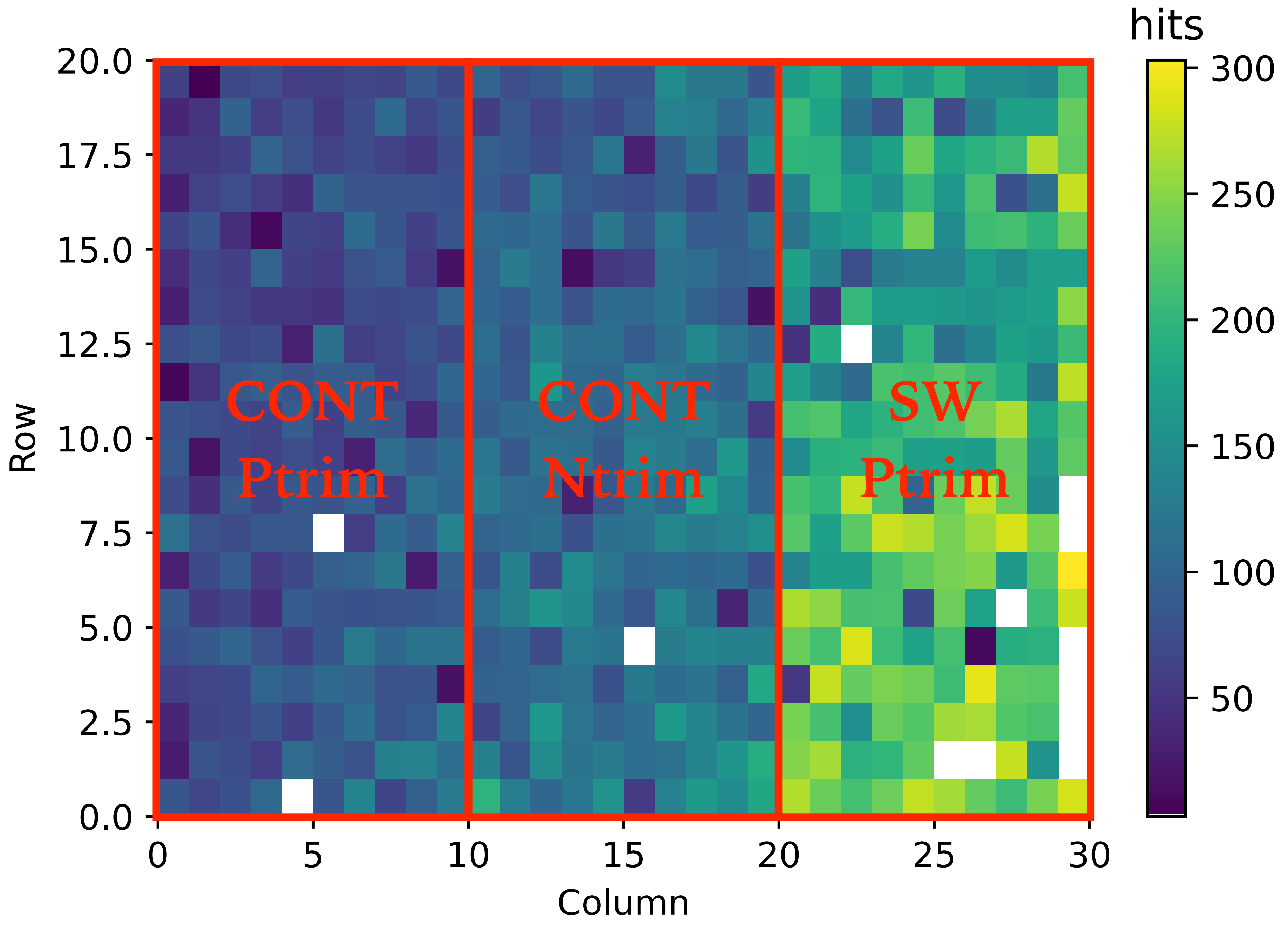




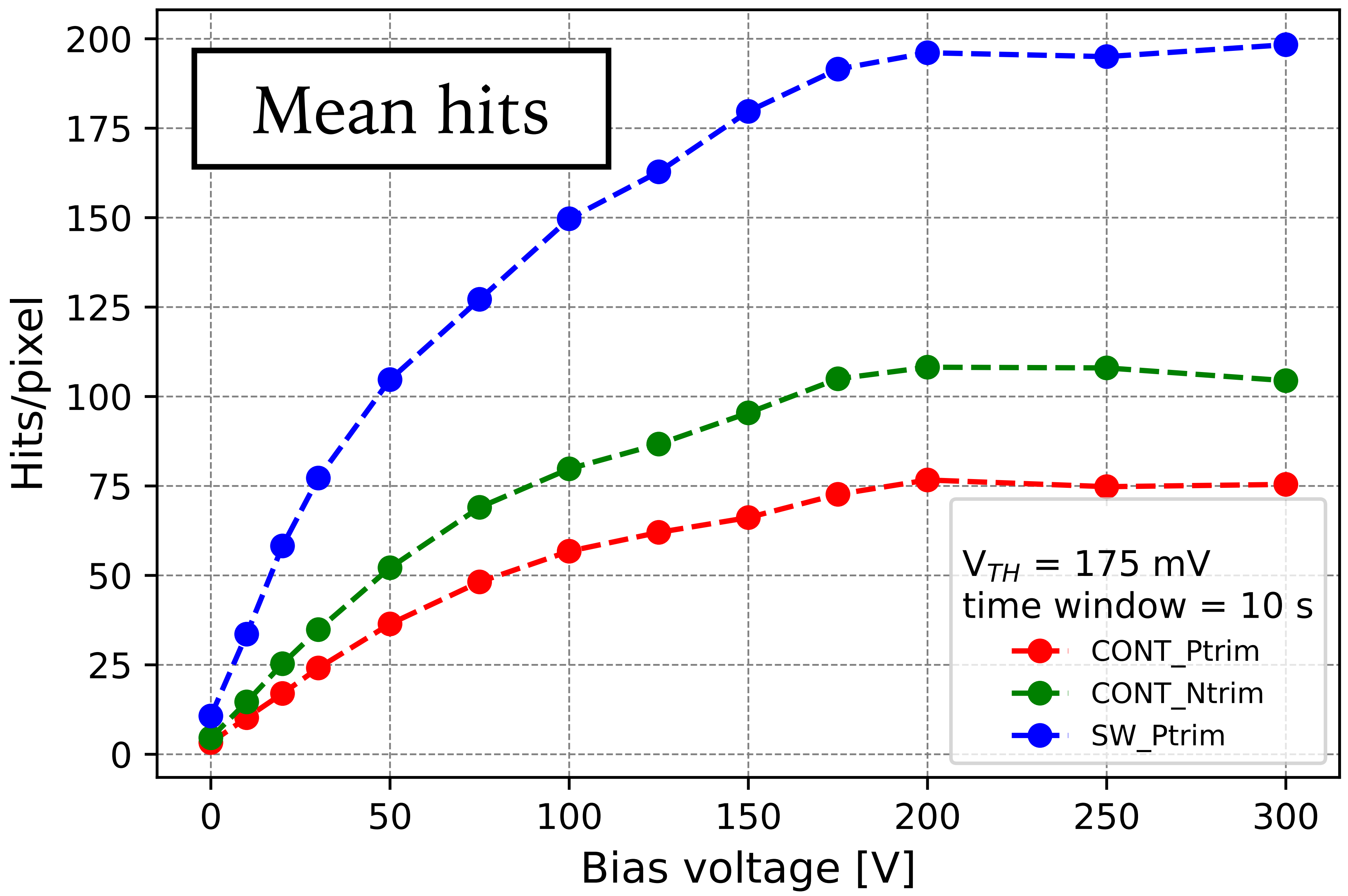
Radiation source measurement – non irradiated

- Used a Sr90 source to briefly characterise the sensing diode.
- Count the number of hits received by each pixels within a time window of 10 s.
- Pixel flavour with higher gain (Switched-reset) detect more hits.
- Hits number increases with Bias voltage, saturates around 200 V, where the chip fully depletes.

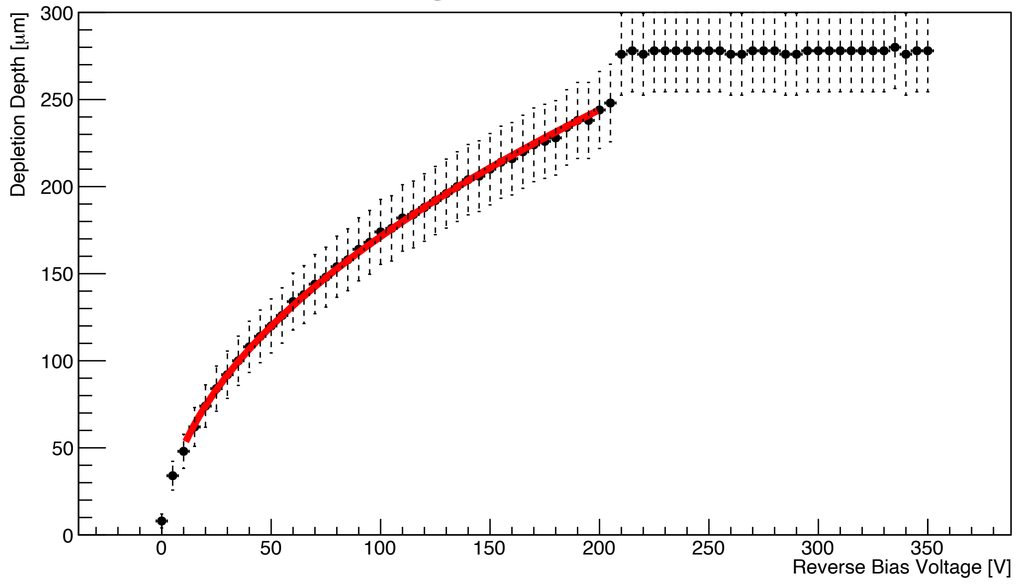




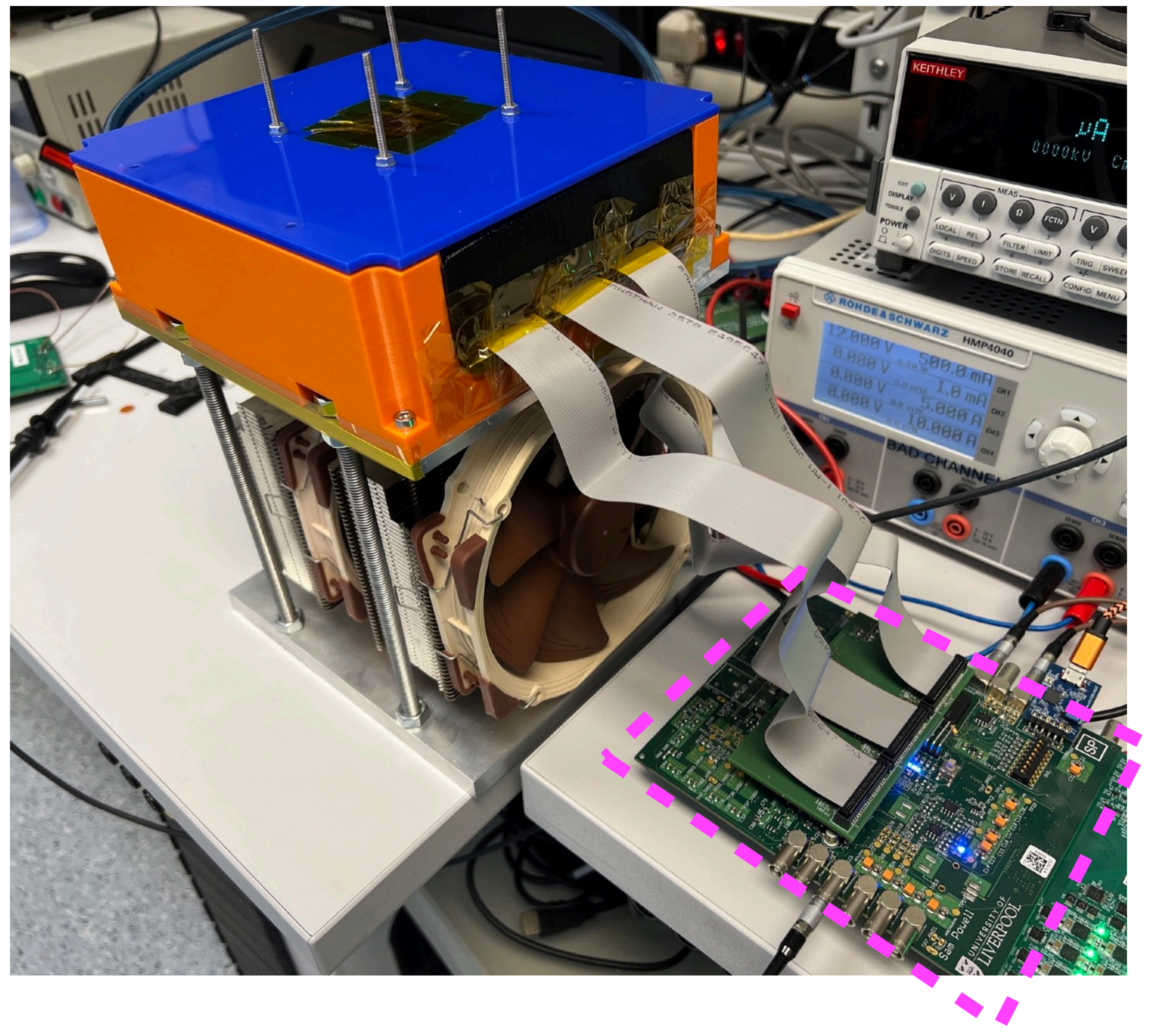
HV = 250 V



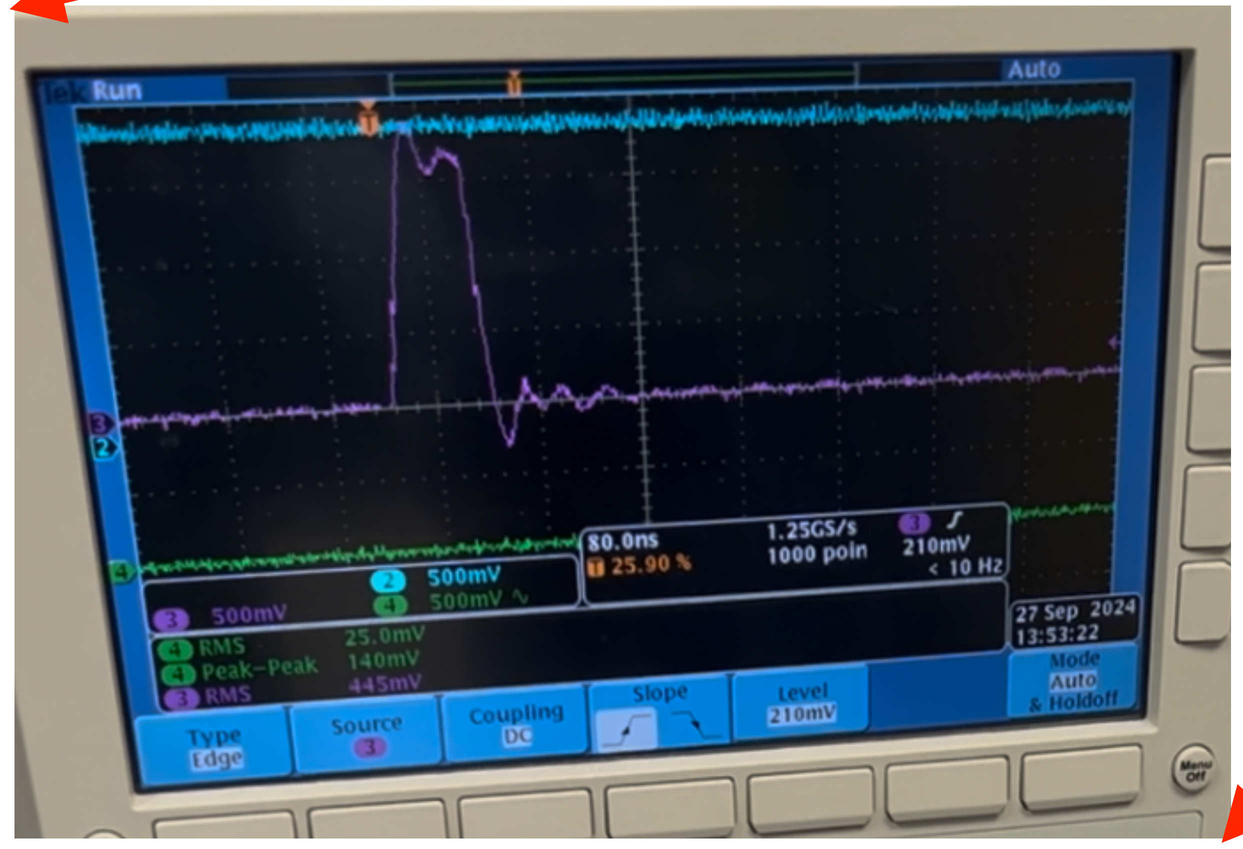
Edge-TCT

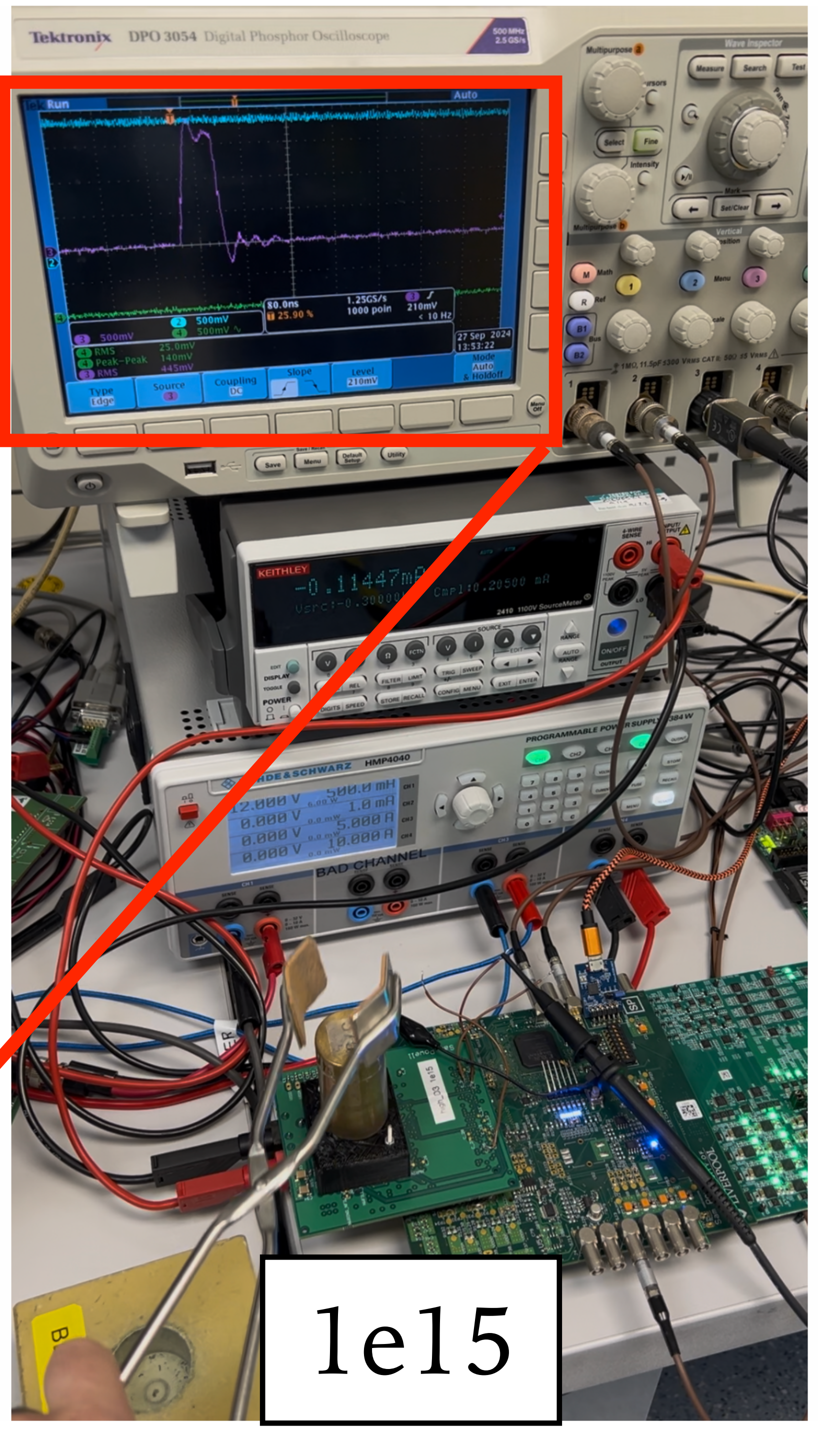


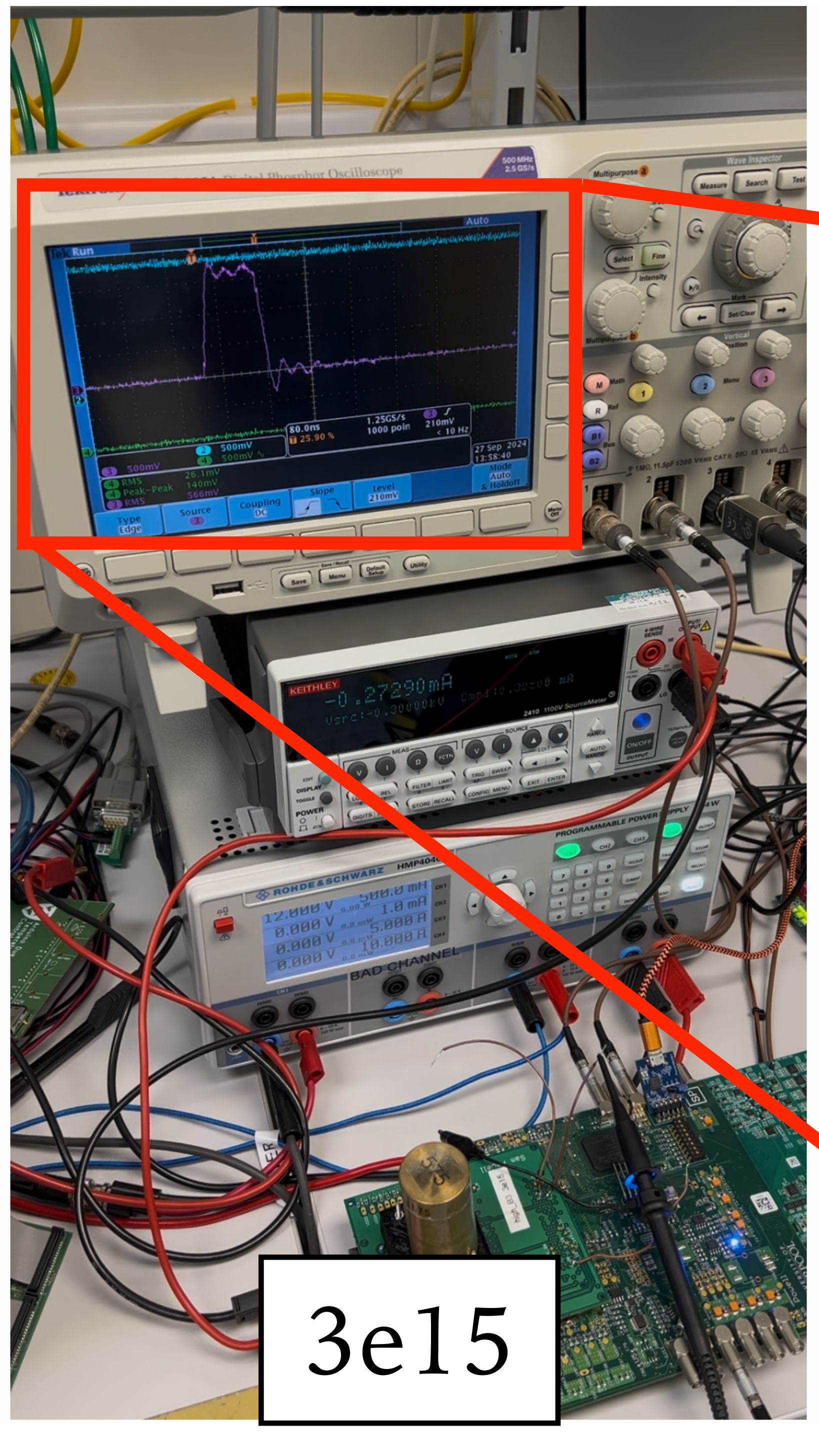
Radiation source measurement – irradiated

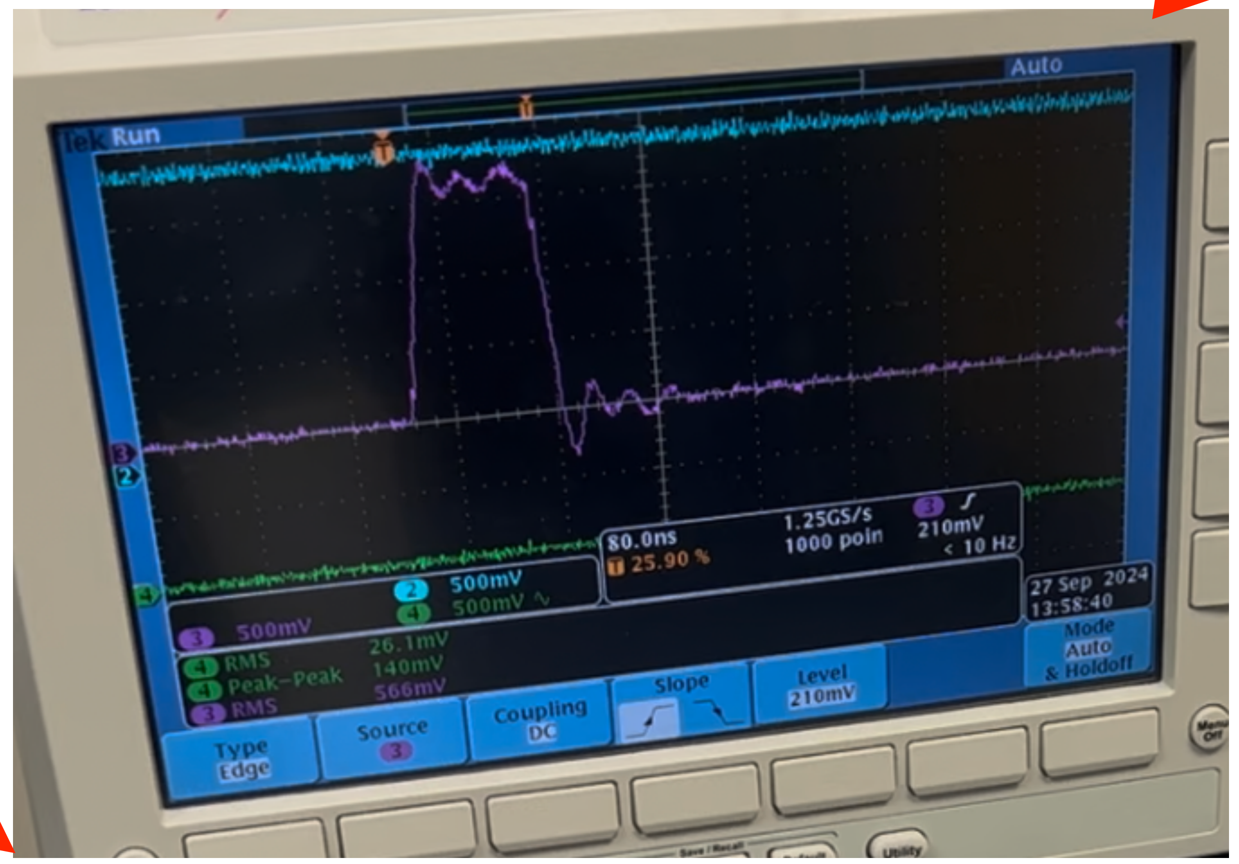


- Ribbon cable for cooling setup adds high noise to power lines.
- Measured irradiated samples without cooling just before the workshop.
- 1e15 and 3e15 irradiated samples could still detected hits with no cooling.
- 1e16 irradiated samples could barely detect without cooling.
- Will use a climate chamber to re-measure irradiated samples.
- Comparator output from one pixel:



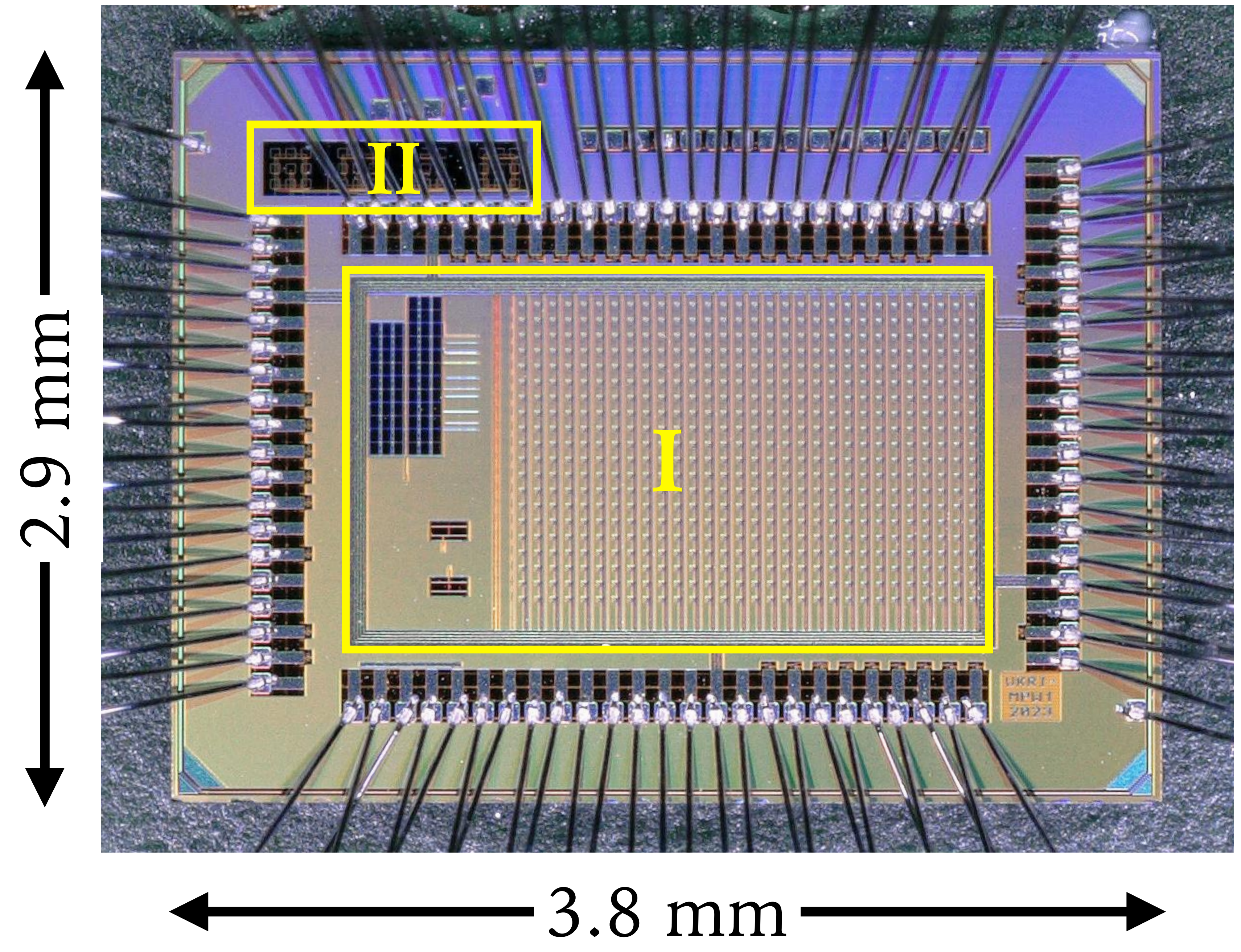






Summary and outlook

- **Summary:**
  - Monolithic HV-CMOS sensor UKRI-MPW1 has high breakdown voltage (> 500 V) and low leakage current (~ 10 nA).
  - Customised P-Shield used.
  - High NIEL radiation tolerance: after 3e15 n_{eq}/cm^2 neutron irradiation, could still detect hits without cooling.
- **Outlook:**
  - Evaluate irradiated samples with cooling.
  - Measure TID tolerance.



Backup: Motivation: radiation tolerance

- Much higher luminosity (> 5×10^{34} $cm^{-2}s^{-1}$) in future experiments.
- To survive radiation damage after long operation, pixel trackers must have higher radiation tolerance.
- The table below compares the best achieved HV-CMOS performance with the tracking detector requirements for future experiments.

	HV-CMOS performance	HL-LHC	FCC-hh
Radiation tolerance	2×10^{15} n_{eq}/cm^2	10^{16} $n_{eq}/cm^2/y$	10^{16} - 10^{17} $n_{eq}/cm^2/y$
Pixel size	50×50 μm^2	50×50 μm^2	25×50 μm^2
Time resolution	3.7 ns	0.2* - 1000 ns**	~ 100 ps
Thickness (material budget)	50 μm	0.1%** - 2% X_0/layer	1% X_0/layer

*LHCb requirement; **ALICE requirement

Backup: trimDAC

- trimDAC tune strength.