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UKRI-MPW1: an HV-CMOS pixel sensor for high radiation tolerance

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A High-Voltage CMOS (HV-CMOS) pixel sensor for particle detection in high energy physics experiments, named UKRI-MPW1, has been developed. It has a high breakdown voltage of ˜700 V, while keeping the leakage current below 100 $\mathrm{nA/cm^2}$. This is achieved by improving the sensor cross-section with a customised P-Shield layer and using an advanced chip guard ring scheme. With high biasing voltages, the sensor of UKRI-MPW1 is expected to have high radiation tolerance. The design and measurements of UKRI-MPW1 after irradiation are presented in this contribution.

Summary (500 words)

The High-Voltage CMOS (HV-CMOS) technology is a promising candidate for future particle physics experiments that have extreme requirements, such as the Mu3e experiment, future upgrades of the Large Hadron Collider (LHC) and the Circular Electron Positron Collider (CEPC). As opposed to hybrid silicon sensors that requires bump-bonding assembly, HV-CMOS pixel sensors integrate the sensing element and readout electronics into the same piece of silicon. Its single-layer structure makes this technology efficient in material budget, production cost and time. The sensor substrate is biased to high voltages, which brings the benefits of fast charge collection by drift and high radiation tolerance up to 10ˆ15 neq/cmˆ2.

To meet the radiation tolerance requirements of future experiments, for example in HL-LHC 5 × 10ˆ15 neq/cmˆ2, the HV-CMOS pixel sensor performance needs to be further improved. The Liverpool HV-CMOS group has developed the UKRI-MPW series HV-CMOS prototypes using the LFoundry 150 nm HV-CMOS process. The latest prototype UKRI-MPW1 improves the sensor cross-section by adding a customised P-Shield layer and uses an advanced chip guard ring scheme, which are optimised for increasing the breakdown voltage with back-side biasing. With large bias voltage, UKRI-MPW1 is expected to achieve a large improvement in the radiation tolerance. To avoid the formation of a parasitic channel between pixels, which was found in its predecessor UKRI-MPW0 [1], UKRI-MPW1 adds the p-type layer P-Shield between its pixels. A pixel matrix of 20 rows and 30 columns (pixel size of 60 × 60 µmˆ2) and test structures are included in the chip. UKRI-MPW1 samples were fabricated on high-resistivity (3 kΩ·cm) wafers which were thinned to 280 µm and backside processed using Beam-Line Ion Implantation (BLII) and Rapid Thermal Annealing (RTA). Samples have been irradiated to different neutron fluences up to 3 × 10ˆ16 neq/cmˆ2.

This contribution covers the evaluation of UKRI-MPW1 before and after irradiation, including IV, edge-TCT measurements and pixel performance. Preliminary I-V measurements show the chip has a high breakdown voltage of 700 V (600 V in UKRI-MPW0) and low leakage current of 100 nA/cmˆ2 (500 µA/cmˆ2 in UKRI-MPW0). After irradiation (1 × 10ˆ16 neq/cmˆ2), the chip can still be biased to 600 V and the leakage current increases from ˜10 nA to ˜10 µA. Pixels are expected to have lower Equivalent Noise Charge (ENC) and gain (< 100 e- and > 100 mV/ke- in UKRI-MPW0). The performance of the UKRI-MPW1 pixels before and after irradiation will be measured and presented at the workshop. Figures showing the listed performance are included in the attachment. The design improvement in UKRI-MPW1, for increasing breakdown voltage, decreasing leakage current and reducing pixel noise, will also be presented.

[1] C. Zhang et al., Measurement of UKRI-MPW0 after irradiation: an HV-CMOS prototype for high radiation tolerance, PoS TWEPP2023 (2024), https://dx.doi.org/10.1088/1748-0221/19/03/C03061

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