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First results on the Ignite-0 test ASIC in CMOS 28-nm technology

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The IGNITE project develops technical solutions for the next generation of trackers at colliders. It plans to implement an integrated module, comprising sensor, electronics, and fast readout, aimed at fast 4D-tracking. System pixels are required to have pitch around 50 μm and time resolution below 30 ps. In the present paper we present measurement results concerning the performance of the first-born prototype ASIC, which explores circuital solutions for Analog Front End and Time-to-Digital Converter circuits. Such prototype structures have been tested before being integrated in a subsequent design, containing a 64x64 pixel matrix for the readout of pixelated sensors.

Summary (500 words)

The INFN IGNITE project is developing technical solutions for the next generation of trackers at colliders, which may require high time resolution measurements at the pixel level (<30 ps on the electronic side), while keeping the pixel size (˜50 μm) and system power consumption substantially unaltered with respect to the present generation of inner tracking systems (1 to 1.5 W/cmˆ2, considering the example of CMS/ATLAS-phase2 and LHCb Upgrade-1).

In this paper we present test results on a prototype ASIC (named Ignite-0), designed in CMOS 28-nm technology, which aims to explore different circuital solutions on the front-end side. The Ignite-0 ASIC is implemented as a mini-ASIC and contains new versions of the former TimeSPOT pixel, consisting of an Analog Front End (AFE) and a high-resolution Time-to-Digital-Converter (TDC). It has been implemented for the detailed characterization of the front-end stages and has been tested on a dedicated test-bench, without physical connection to sensors, but using a built-in charge injection system.

The AFE solutions are evolutions of the TimeSPOT one, which is a Charge Sensitive Amplifier with Krummenacher feedback and discrete-time Offset Compensation. Alternative solutions for threshold settings have been implemented and tested. They are illustrated and critically compared in this paper. Different solutions on the AFE input stage and feedback circuit, aimed at optimizing the system performance in terms of time resolution and low power consumption (around 20 μW per pixel), are here explored as well. The AFE solutions all aim at a time resolution of 30 ps at 1 fC deposited charge.

The TimeSPOT TDC, based on a Vernier-type architecture, have several improvements in terms of operational and SEU robustness. The TDC has a nominal binary resolution of 30-40 ps, corresponding to a r.m.s. resolution of about 10 ps. Furthermore, the front-end pixel size is also reduced from 55 μm (TimeSPOT) to the level of 40 μm, to make it possible the read-out of smaller pixel sensors.

The Ignite-0 ASIC also integrates additional important service circuits, and in particular DACs and PLLS, to test them on silicon before their integration on the 64x64 pixel matrix, which is presently in an advanced implementation stage.

In this paper we illustrate and discuss the results obtained on the AFE, TDC and the other test structures. We also indicate their use in the 64x64 ASIC, which is presently in an advanced stage of development. Such ASIC is itself of remarkable interest both in the short term, for the characterization of high-performance timing silicon sensors (such us 3D, TI-LGAD, i-LGAD etc.), and in the longer term, as a test ASIC of the final IGNITE ASIC, featuring a 256x256 pixel matrix.

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