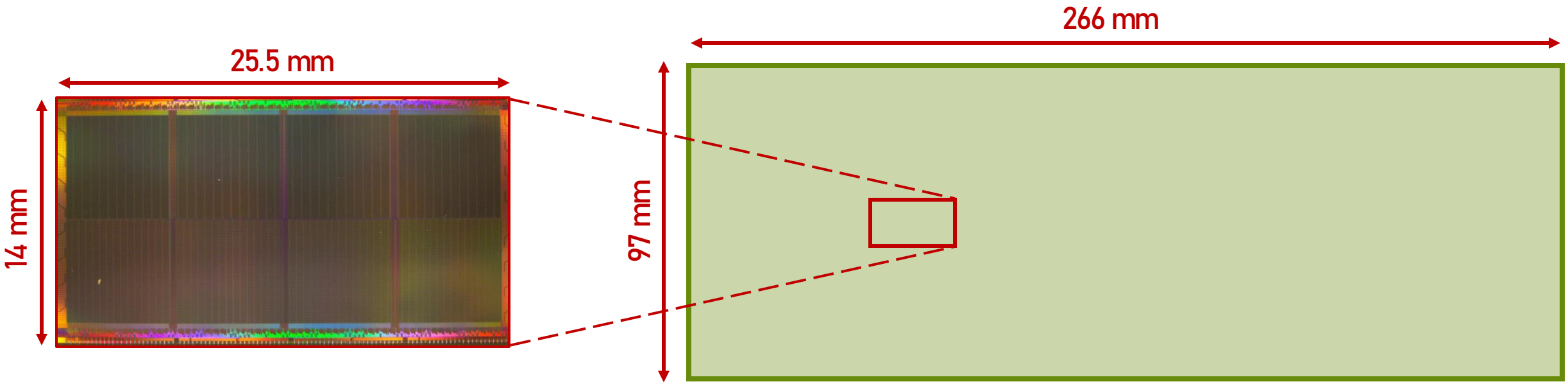
Yield Characterisation and Failure Analysis of the Monolithic Stitched Sensor MOSS for ALICE ITS3

Gregor Eberwein (Oxford & CERN), on behalf of ALICE

TWEPP 2024

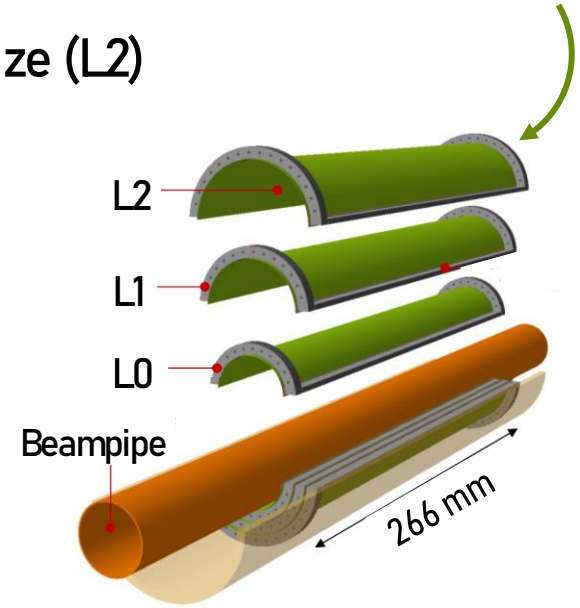
02.10.2024

Stitching for ALICE Inner Tracking System (ITS3)

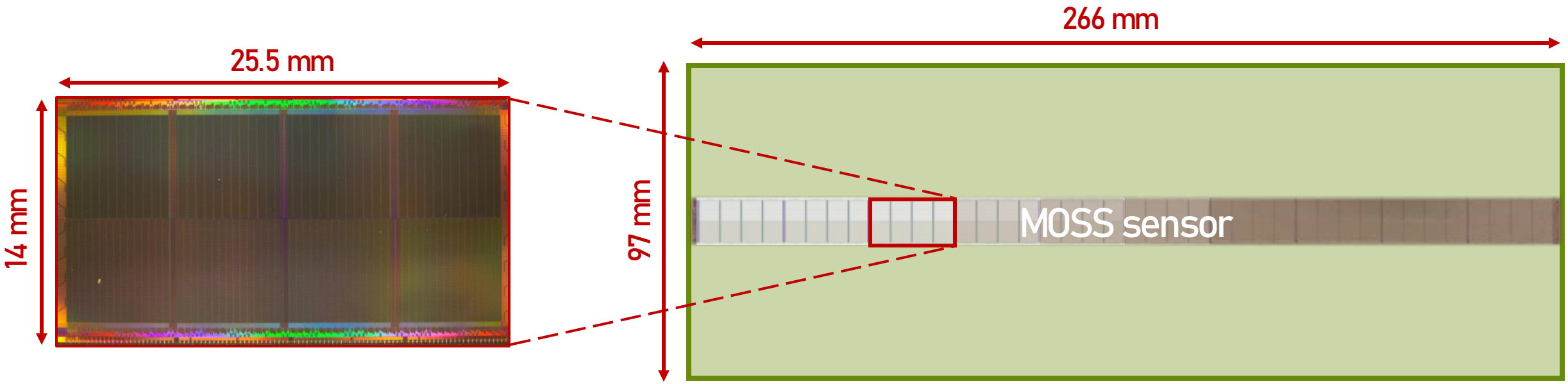


~ maximum design reticle size

ITS3 outermost layer size (L2)

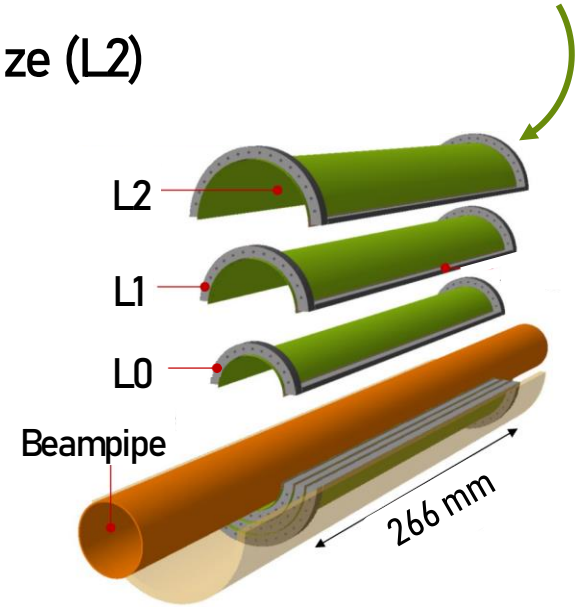


Stitching for ALICE Inner Tracking System (ITS3)



~ maximum design reticle size

ITS3 outermost layer size (L2)



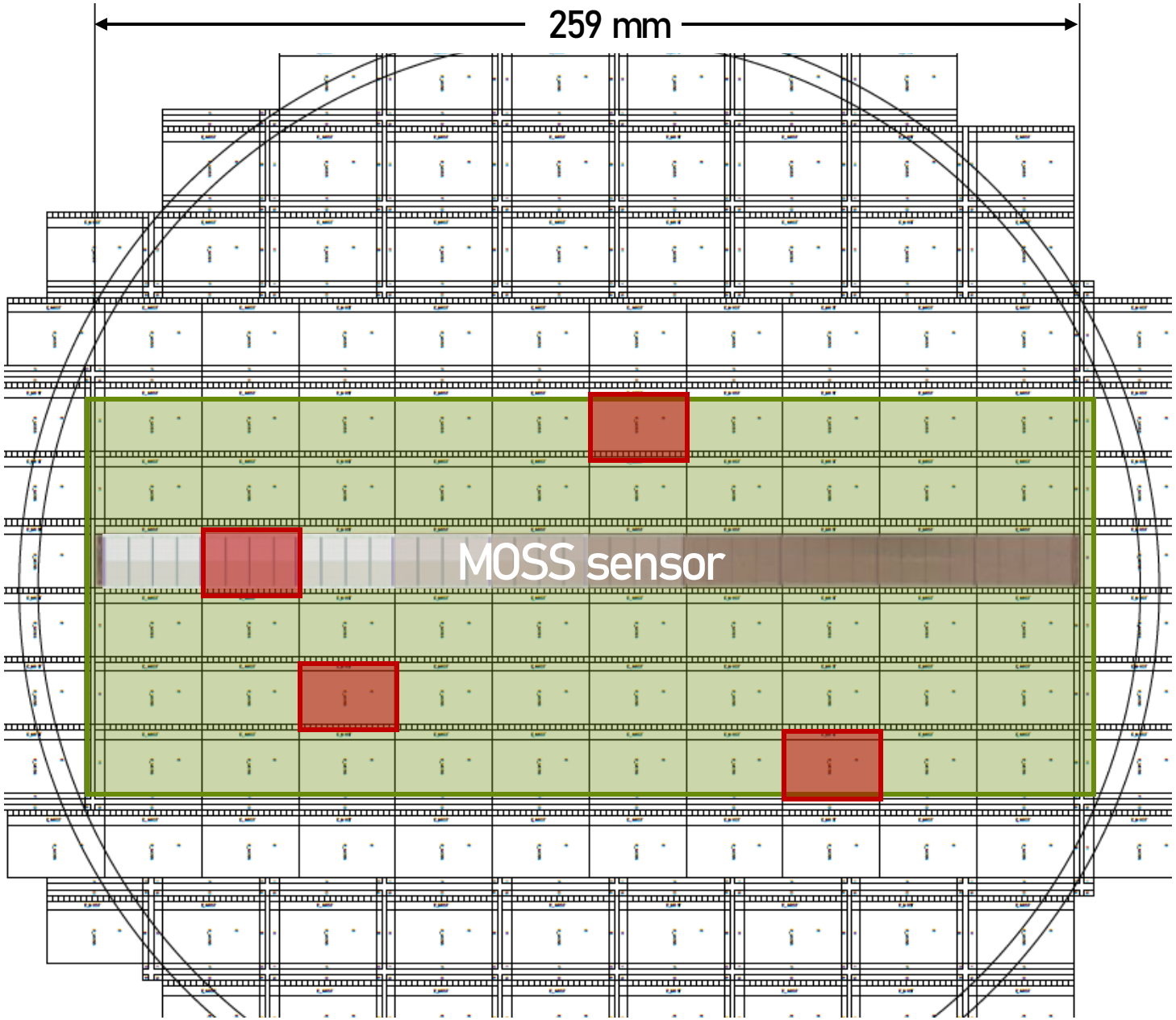
Stitched prototypes in Engineering Run 1 (ER1, 65nm):

- MOSS – MOnolithic Stitched Sensor (14 x 259 mm^2)
- MOST – Timing (2.5 x 259 mm^2)

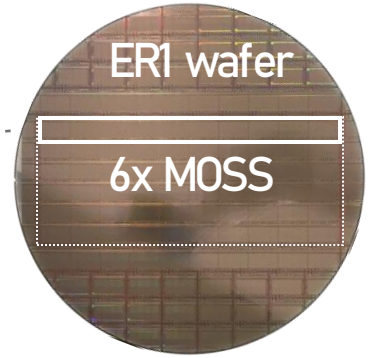
Wafer scale MAPS sensor

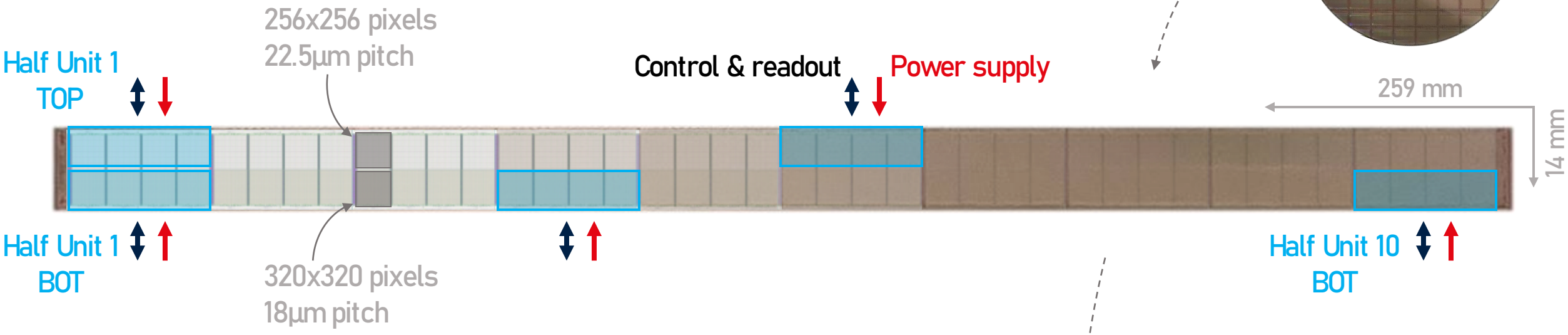
- Cannot pick single reticle-size structures: High yield crucial
- MOSS: Yield characterisation
- Full ITS3 layer: Segmentation in individual power domains to switch off faulty areas

See talks by P. Leitao, S. Bugiel



MOSS prototype sensor





MOSS on testing PCB (82 available)

20 Half Units per MOSS, individually interfaced

Highly **granular design for detailed characterisation**:

- 107 supply nets (64 power domains + substrate)
- 2192 bonding pads
- 390 digital I/Os, 480 Analog I/Os

MAPS and metal interconnections

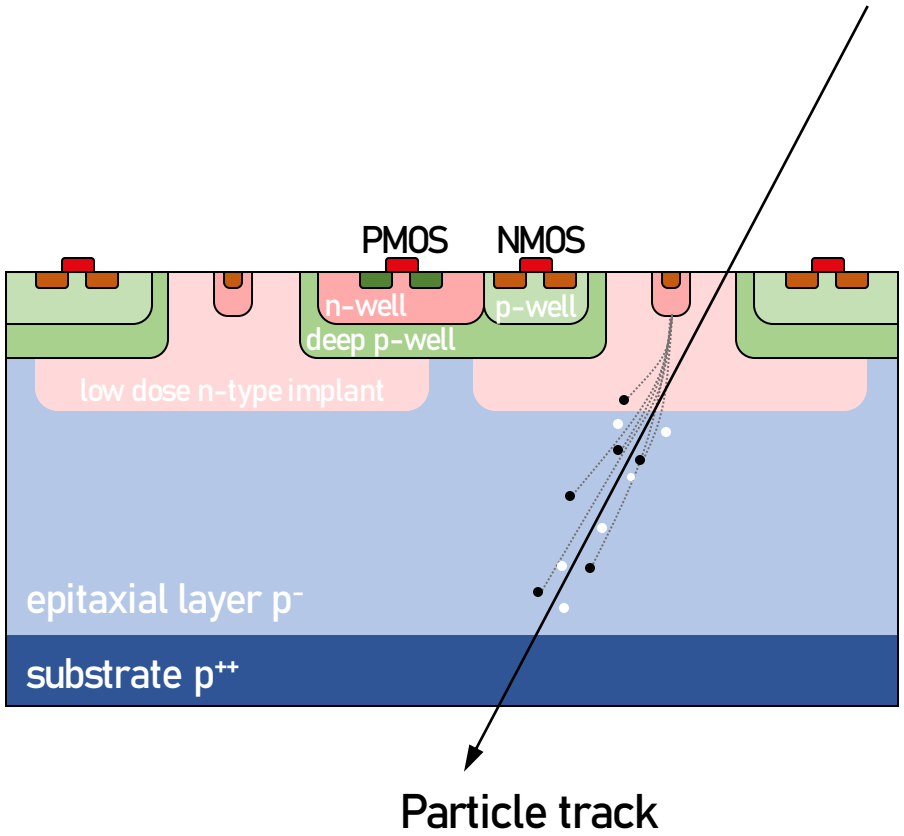


*Illustration not to scale

MAPS and metal interconnections

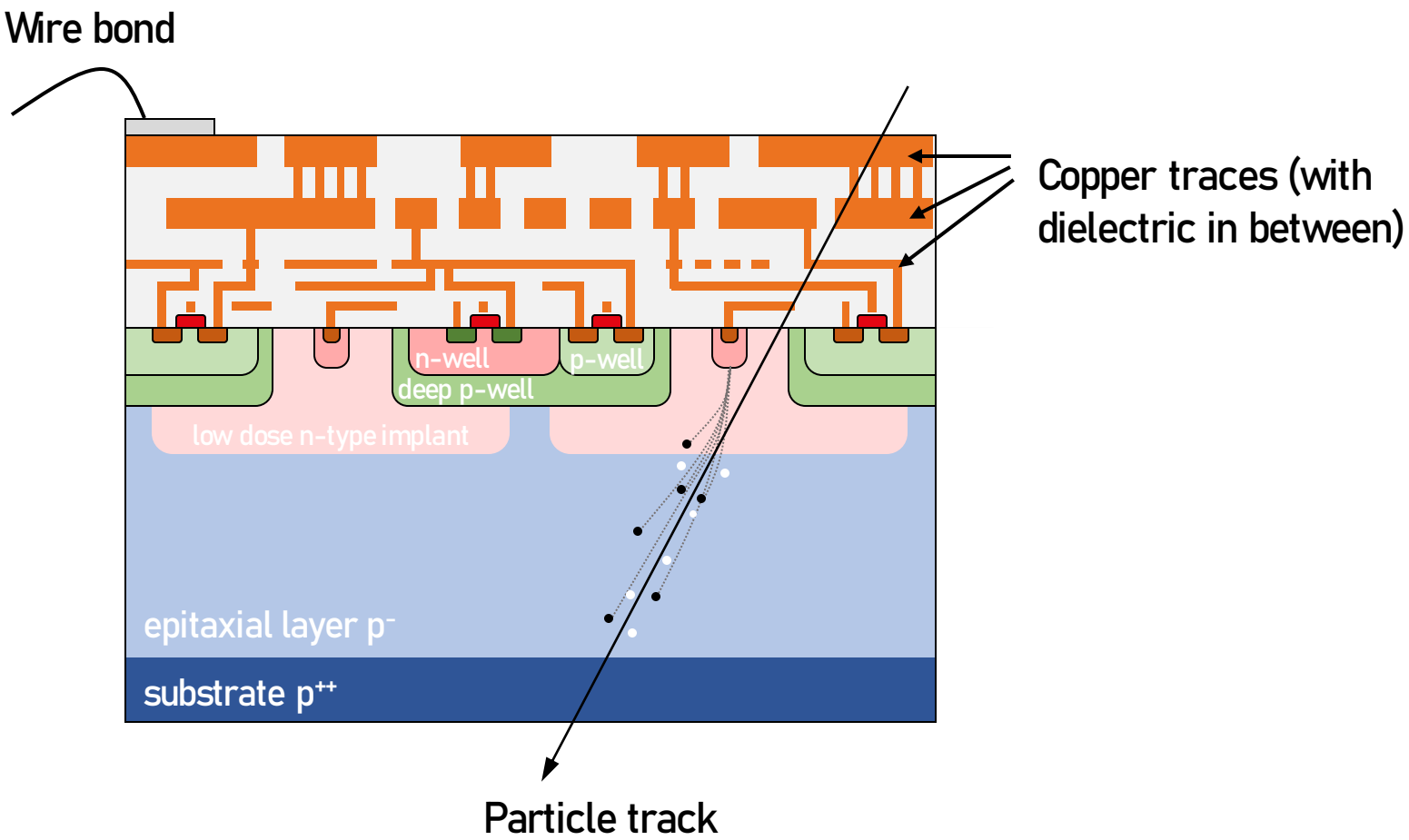


*Illustration not to scale

MAPS and metal interconnections

MOSS:
Top 2 copper layers (M7/M8): Power grid

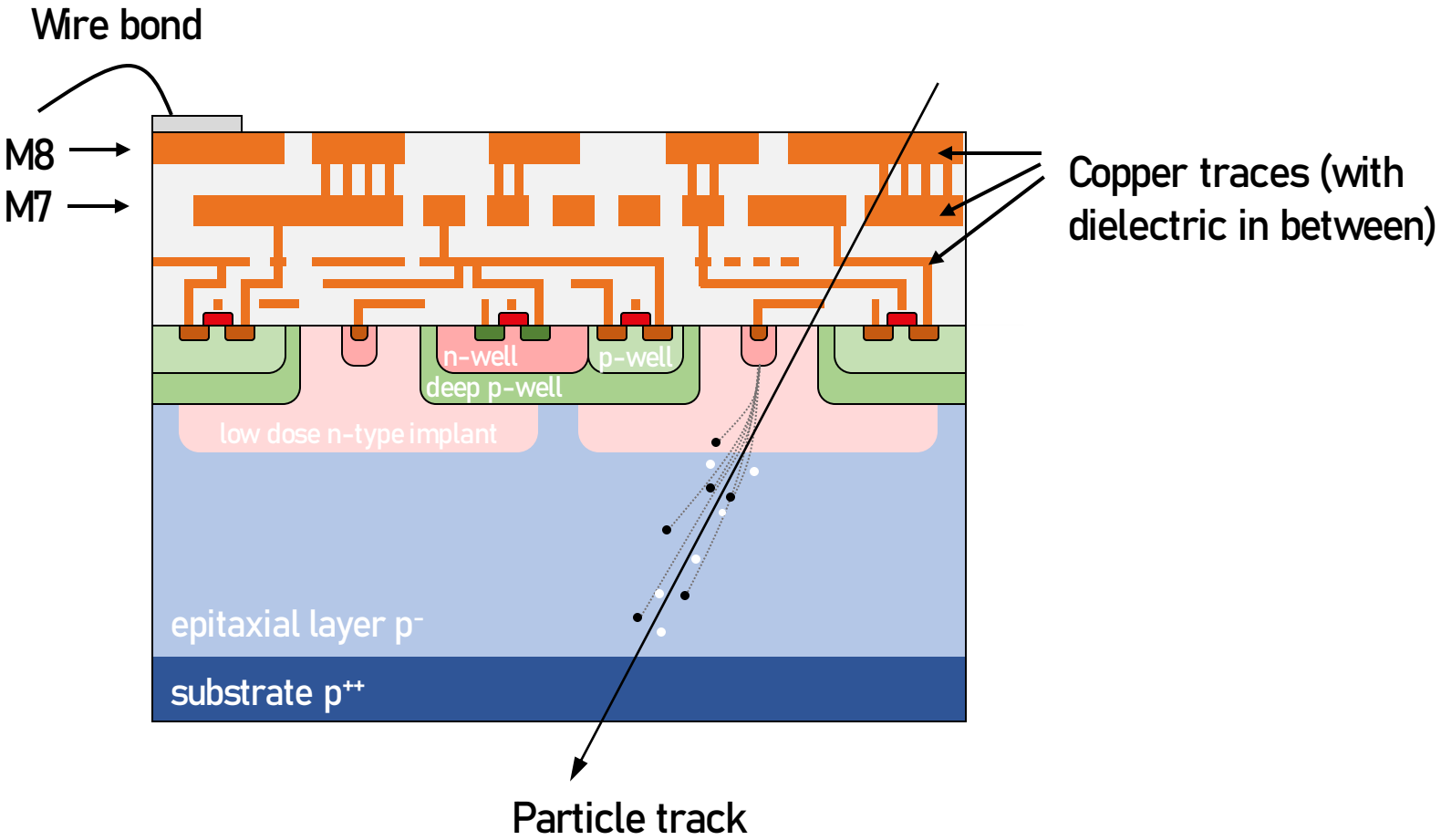
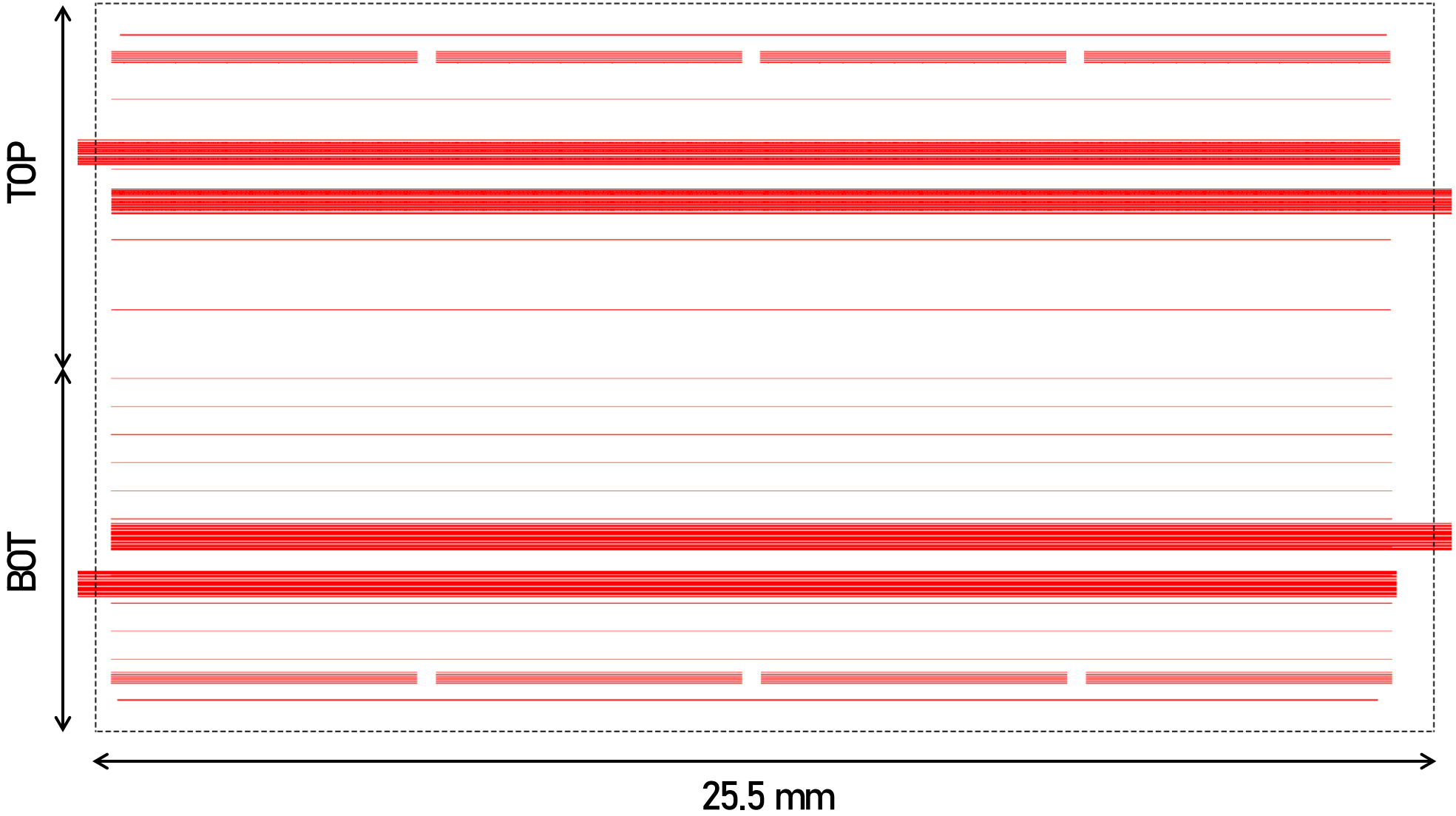


*Illustration not to scale

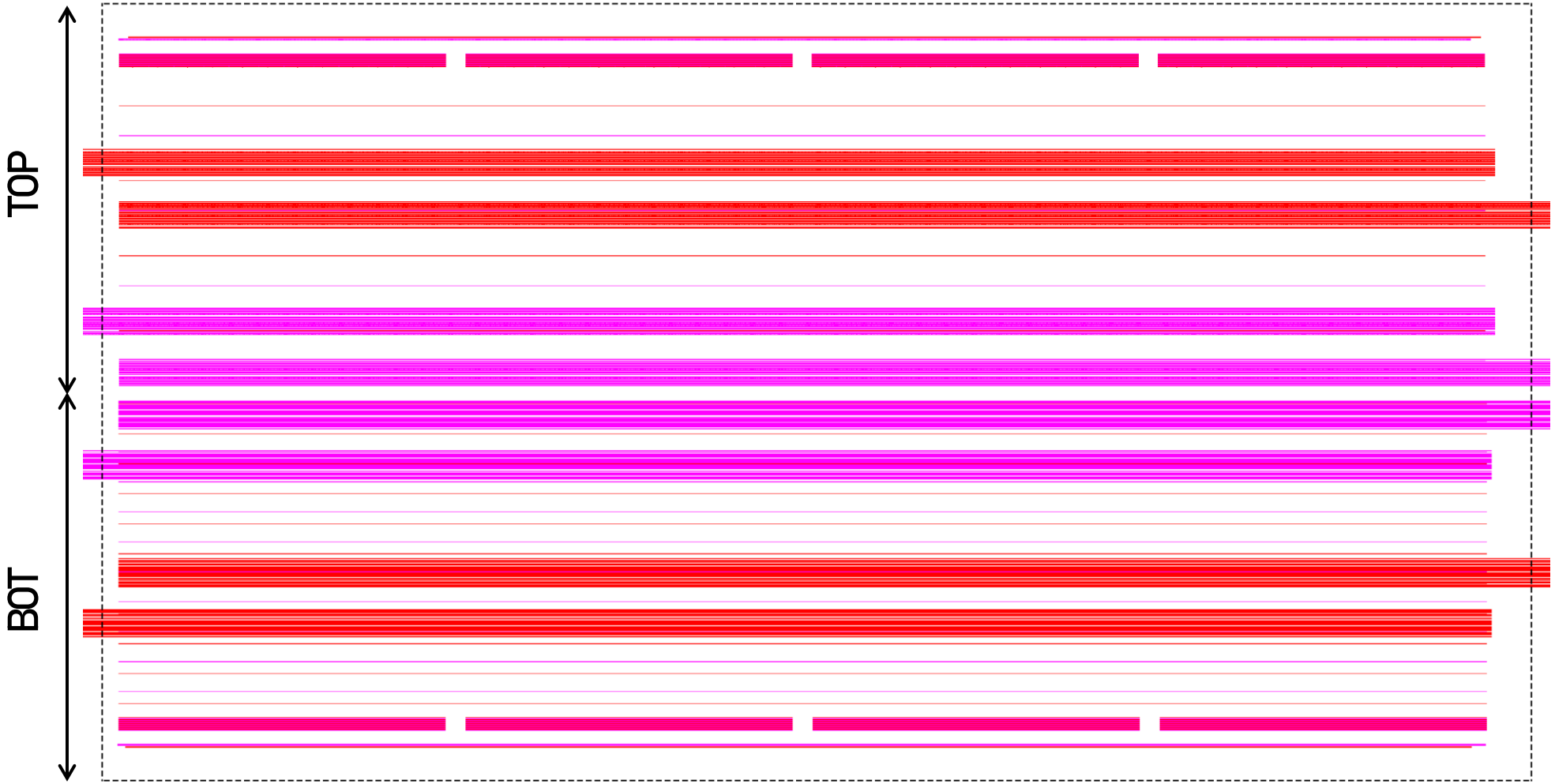
MOSS power grid



AVDD

M7: horizontal

MOSS power grid

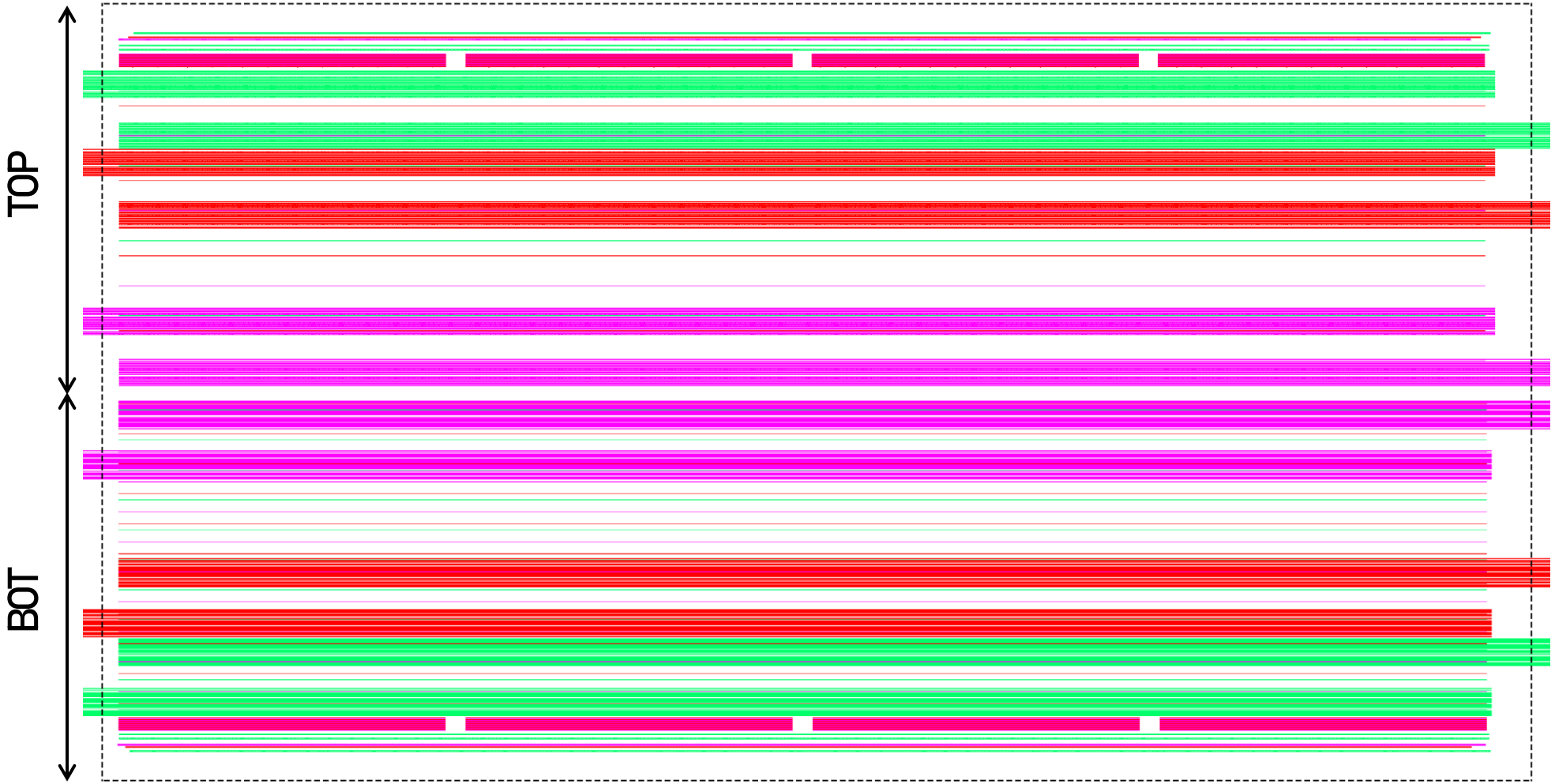


AVDD

AVSS

M7: horizontal

MOSS power grid



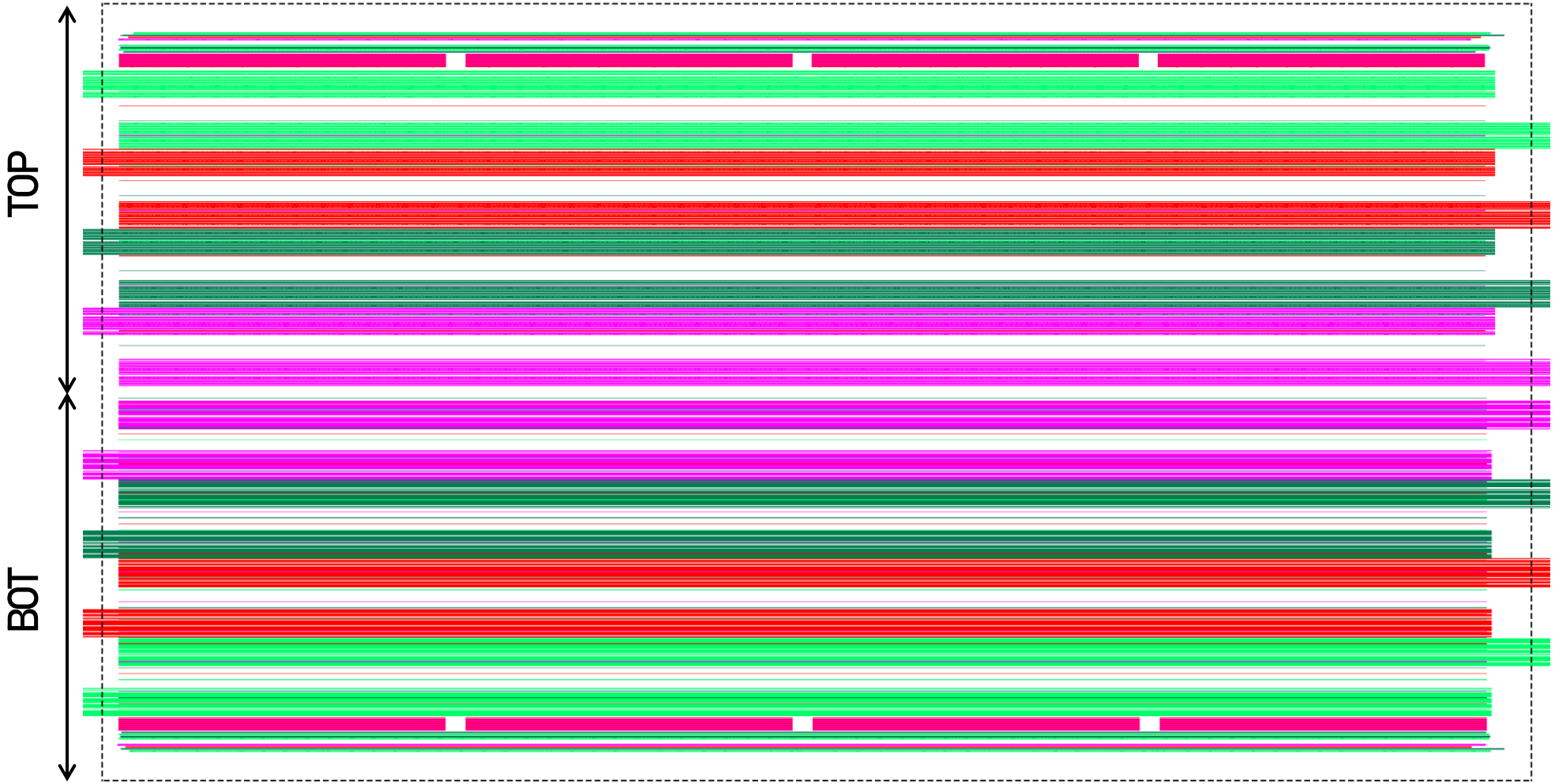
AVDD

AVSS

DVDD

M7: horizontal

MOSS power grid



AVDD

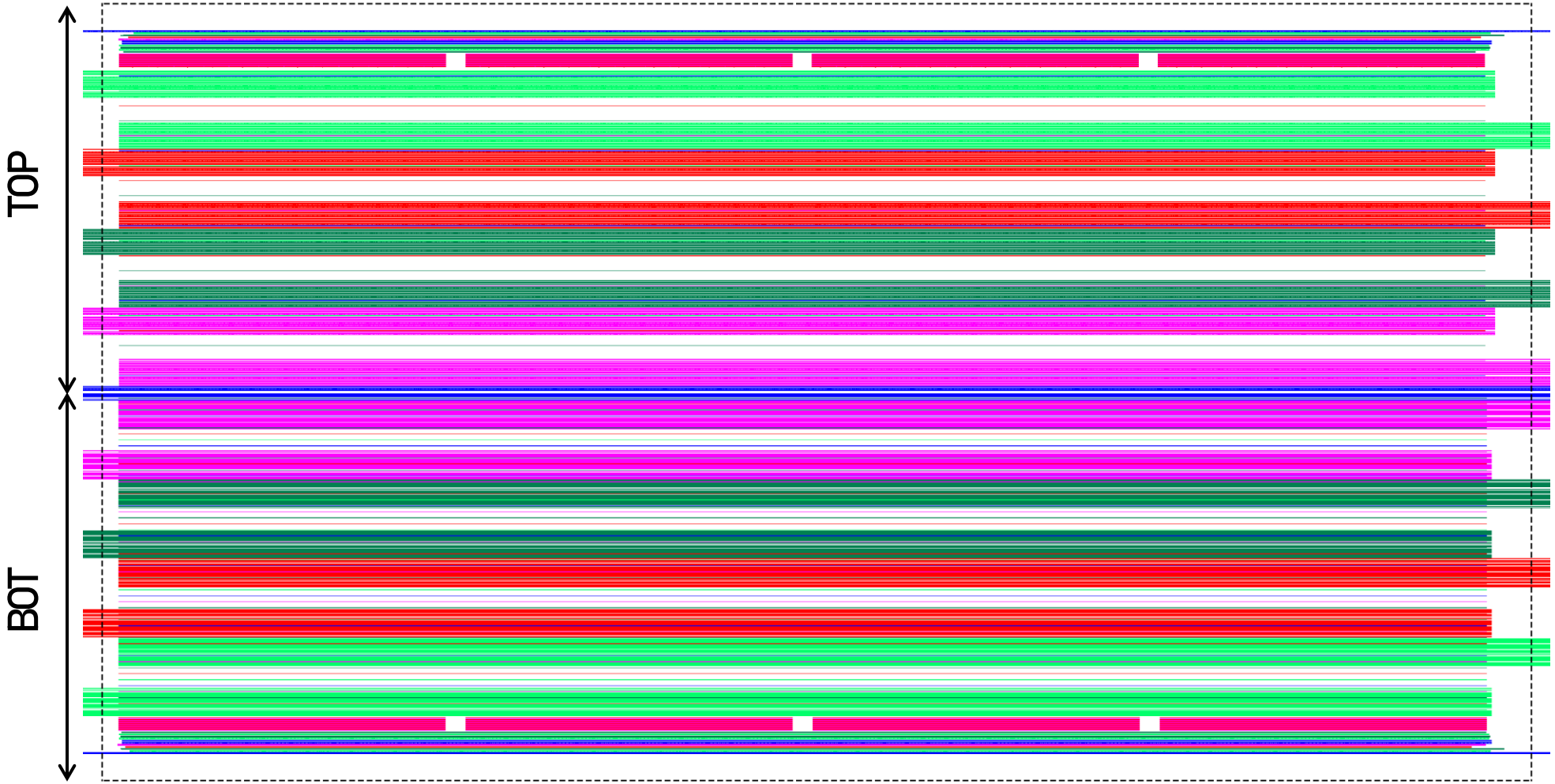
AVSS

DVDD

DVSS

M7: horizontal

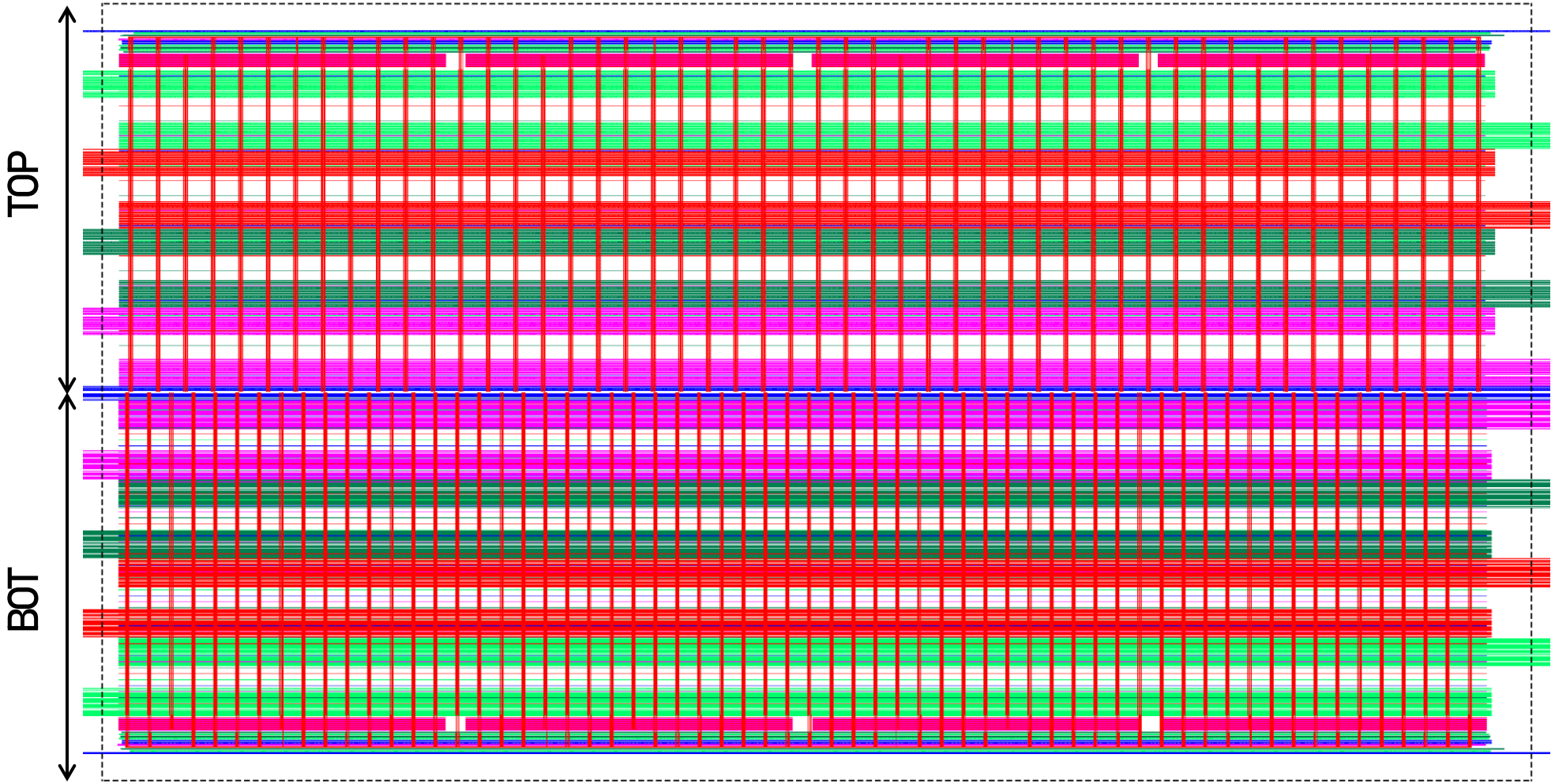
MOSS power grid



AVDD
AVSS
DVDD
DVSS
PSUB

M7: horizontal

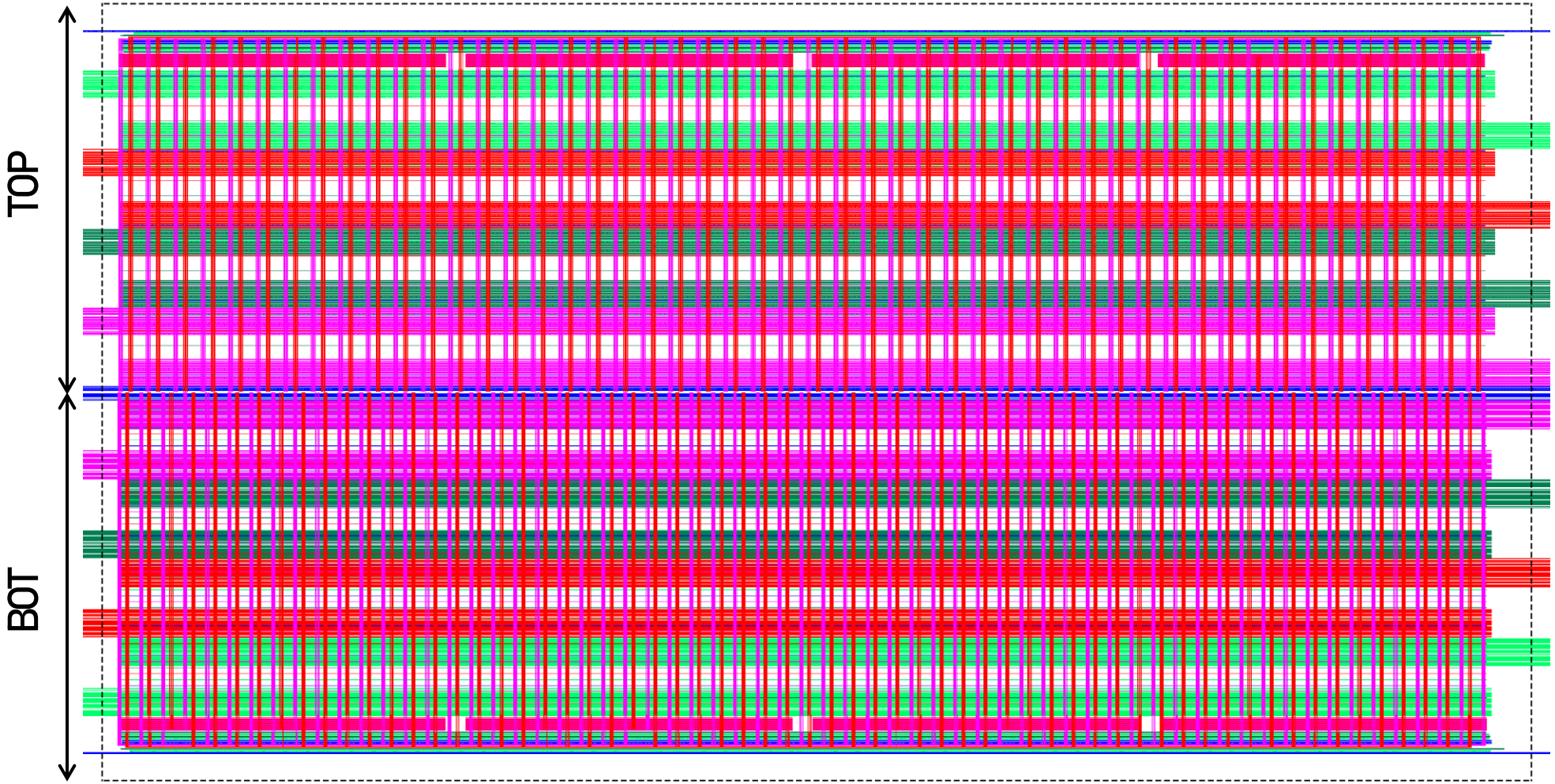
MOSS power grid



AVDD
AVSS
DVDD
DVSS
PSUB

M7: horizontal
M8: vertical

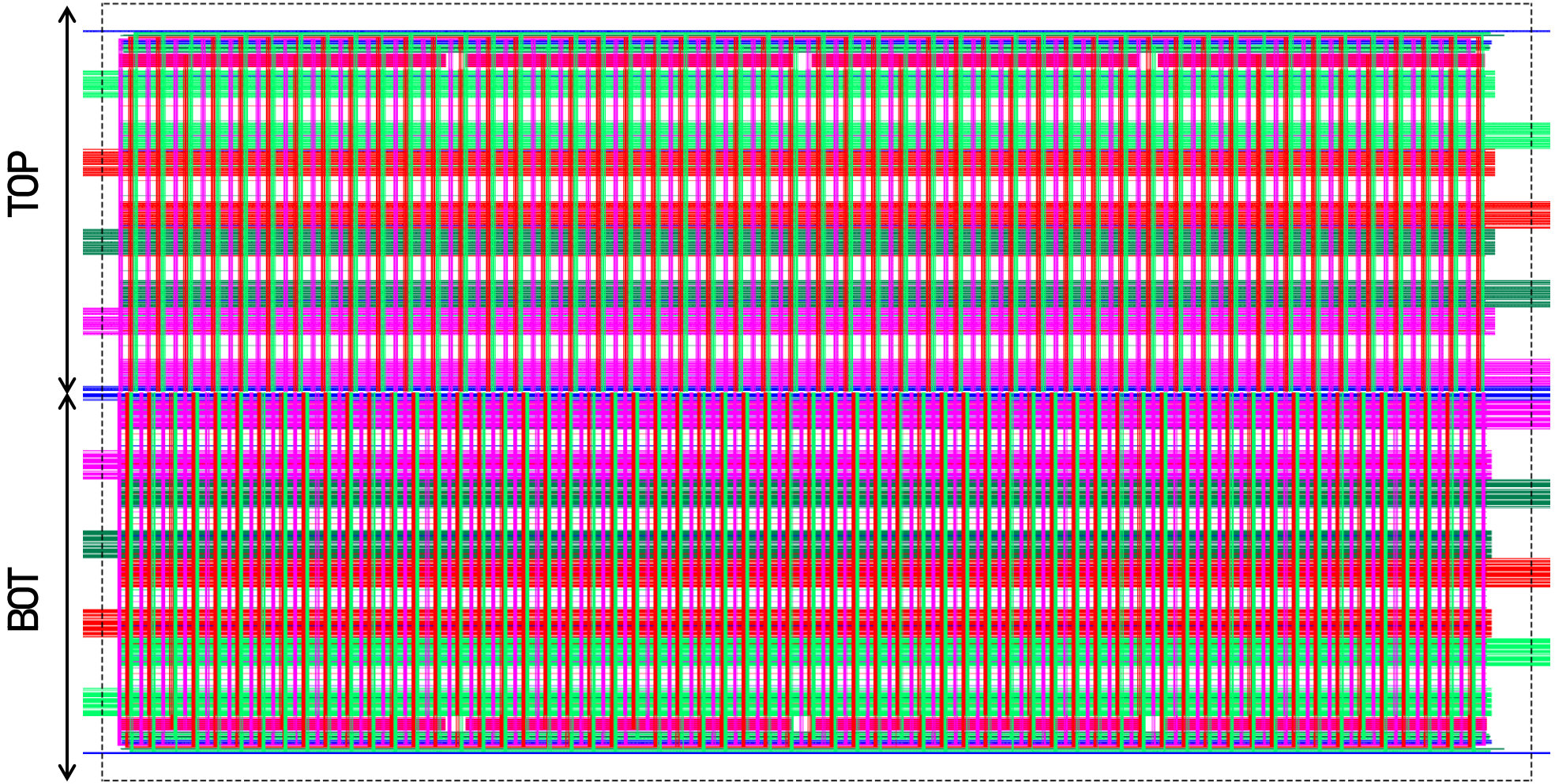
MOSS power grid



AVDD
AVSS
DVDD
DVSS
PSUB

M7: horizontal
M8: vertical

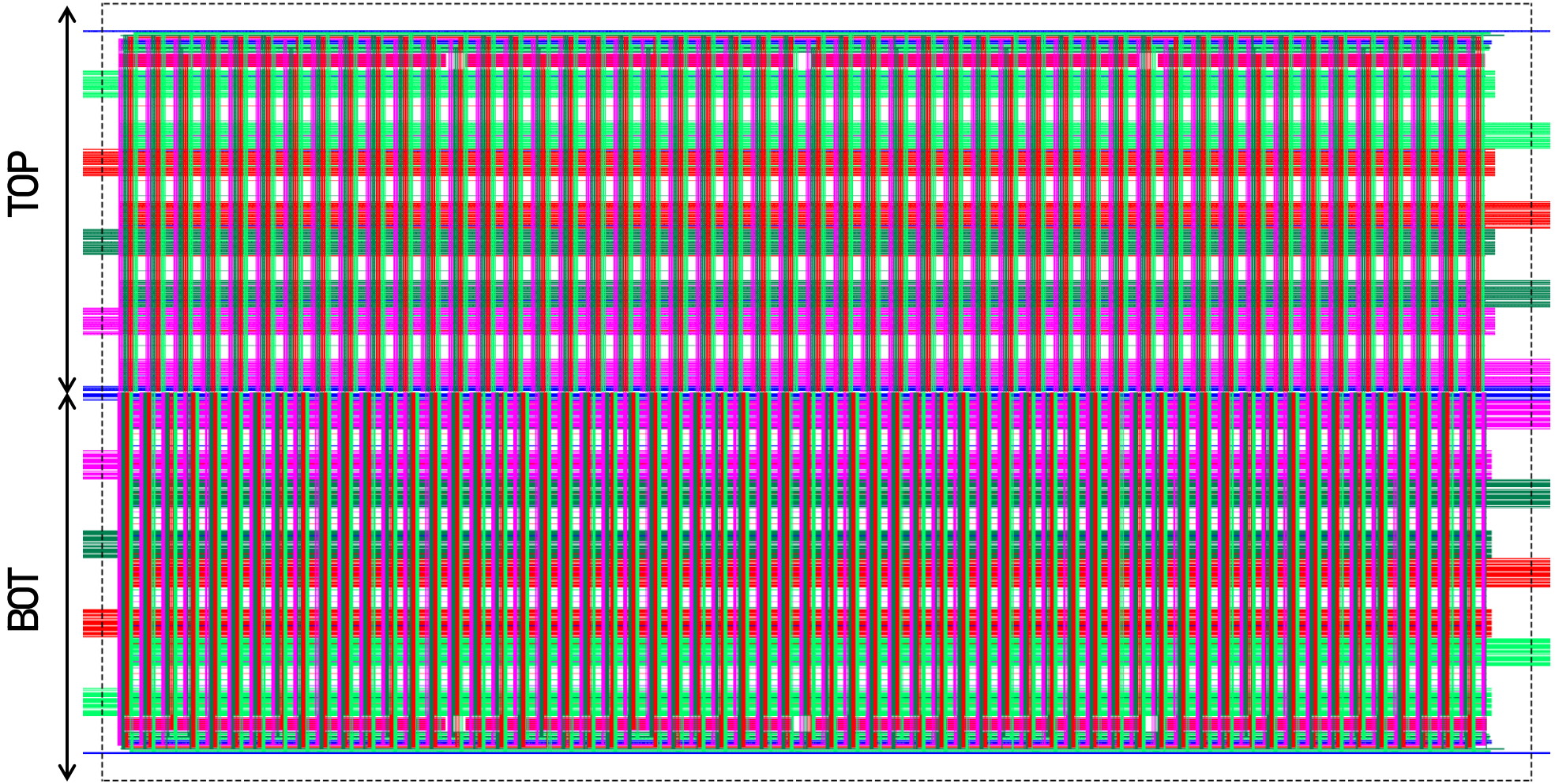
MOSS power grid



AVDD
AVSS
DVDD
DVSS
PSUB

M7: horizontal
M8: vertical

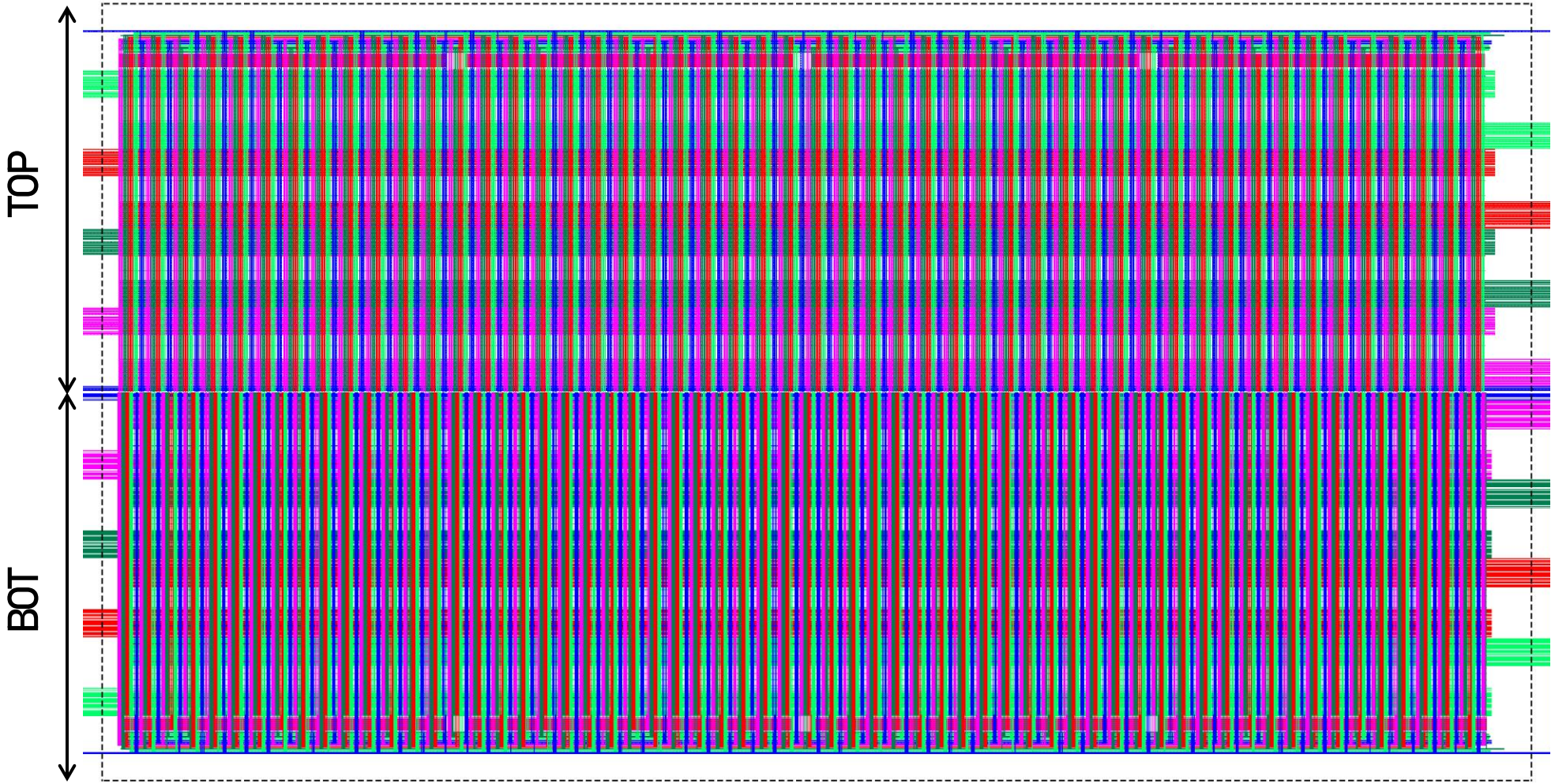
MOSS power grid



AVDD
AVSS
DVDD
DVSS
PSUB

M7: horizontal
M8: vertical

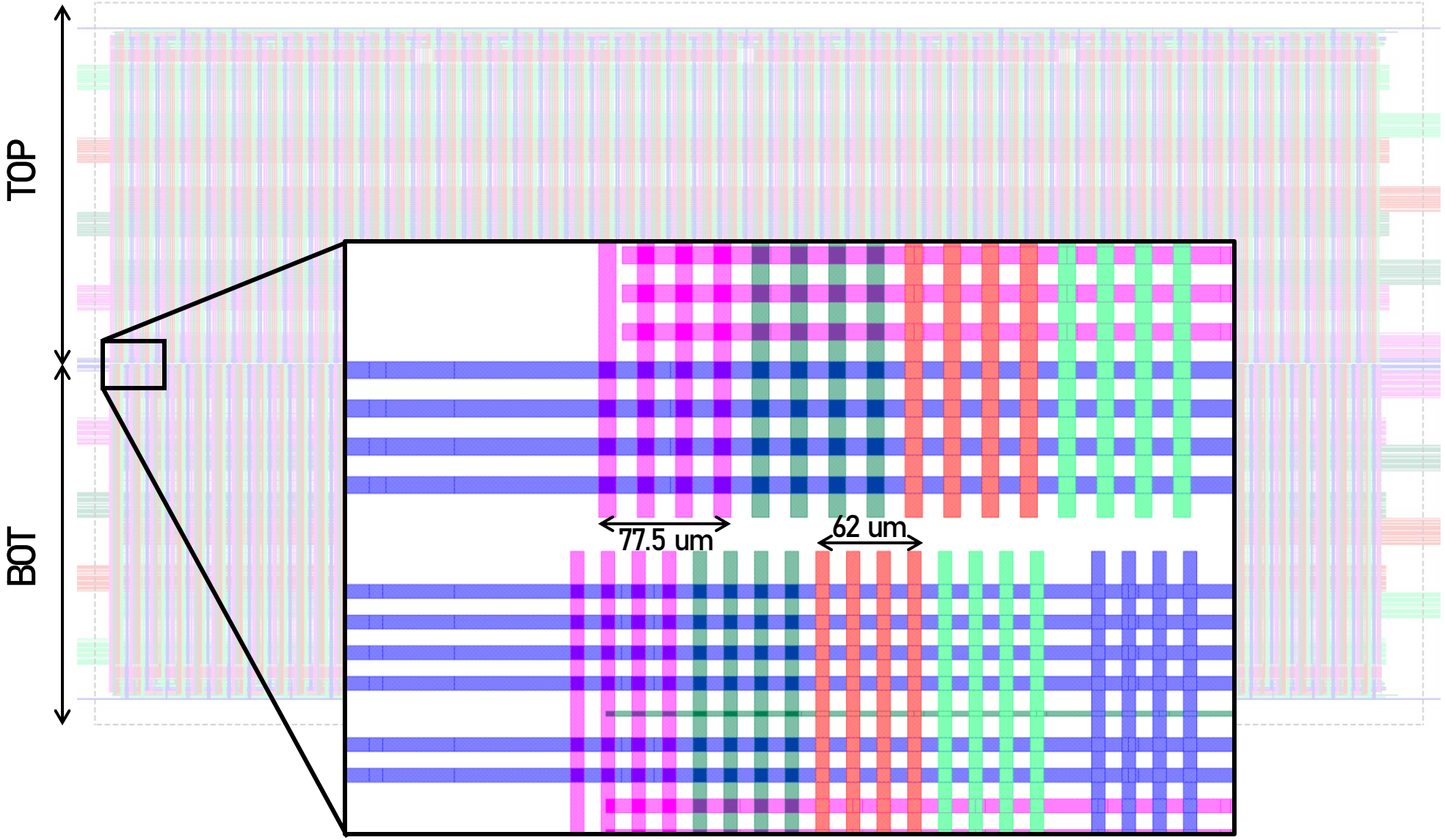
MOSS power grid



AVDD
AVSS
DVDD
DVSS
PSUB

M7: horizontal
M8: vertical

MOSS power grid

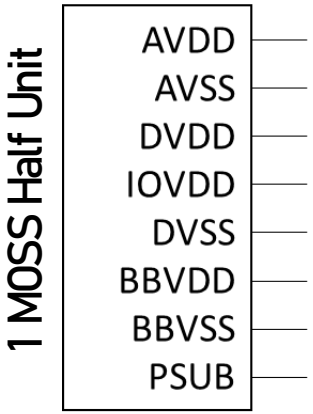


AVDD
AVSS
DVDD
DVSS
PSUB

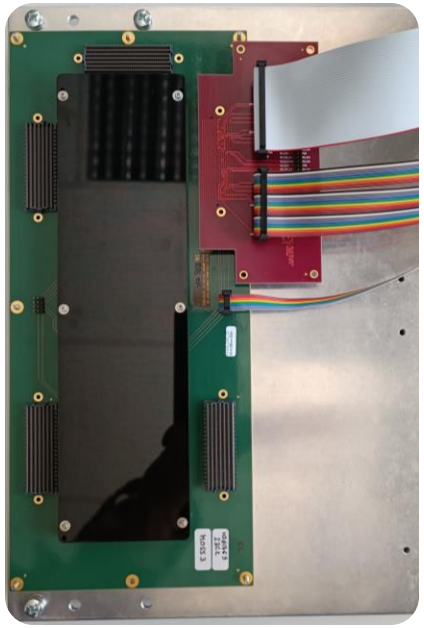
M7: horizontal
M8: vertical

Measurement sequence

Impedances

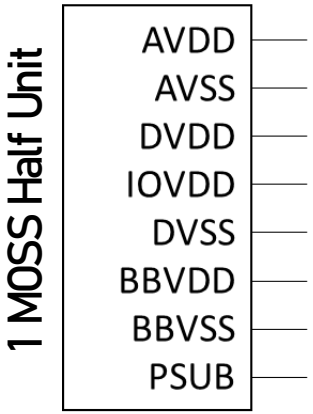


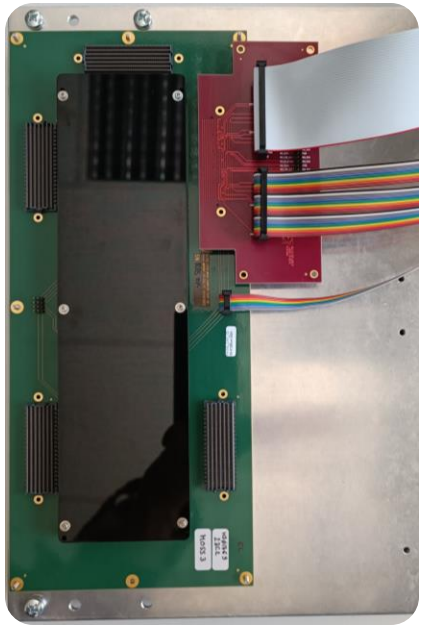
8 power nets -> $\binom{8}{2}$ = 28 net pair combinations



Measurement sequence

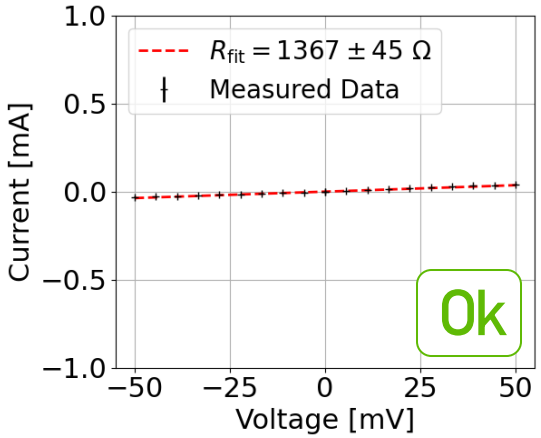
Impedances

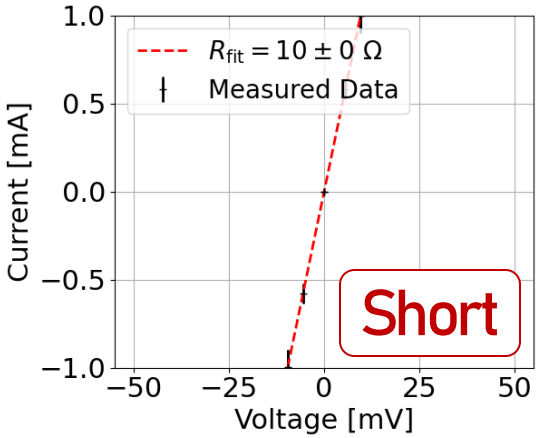




8 power nets -> $\binom{8}{2}$ = 28 net pair combinations

Impedance of each net combination measured: 'Short' if <30 Ohm





-> Detect potential faults prior to powering

Measurement sequence

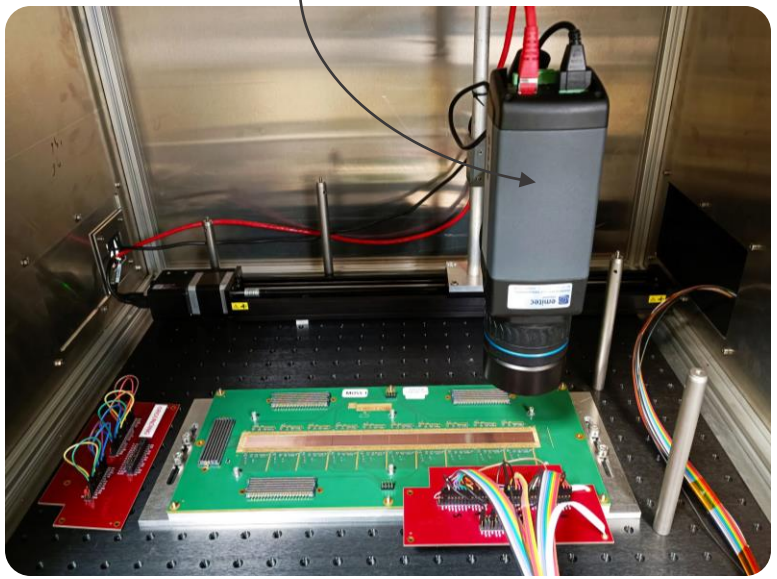
Impedances

Power ramping

Sequentially ramp up power nets to nominal voltage – observed (transient) high currents

Systematic measurement with thermal camera for every half unit to localise faults

Thermal camera on linear stage

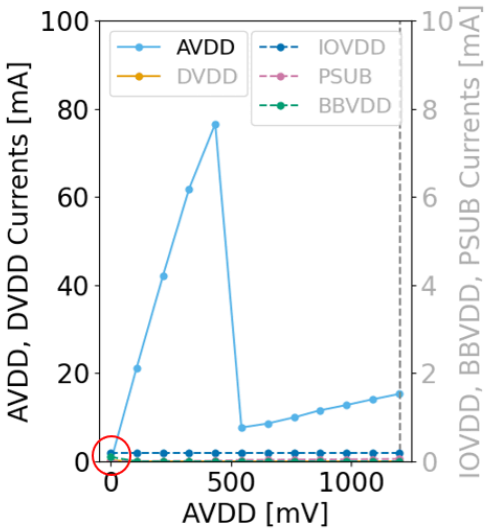


Measurement sequence

Impedances

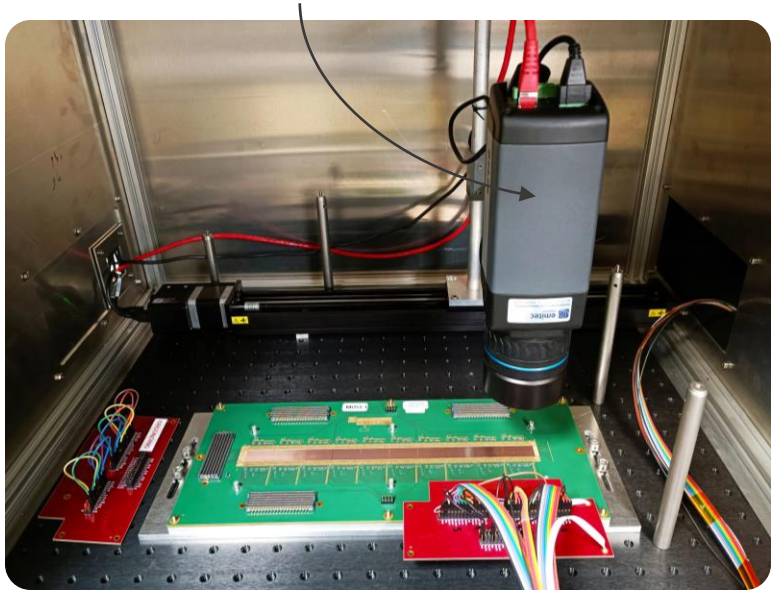
Power ramping

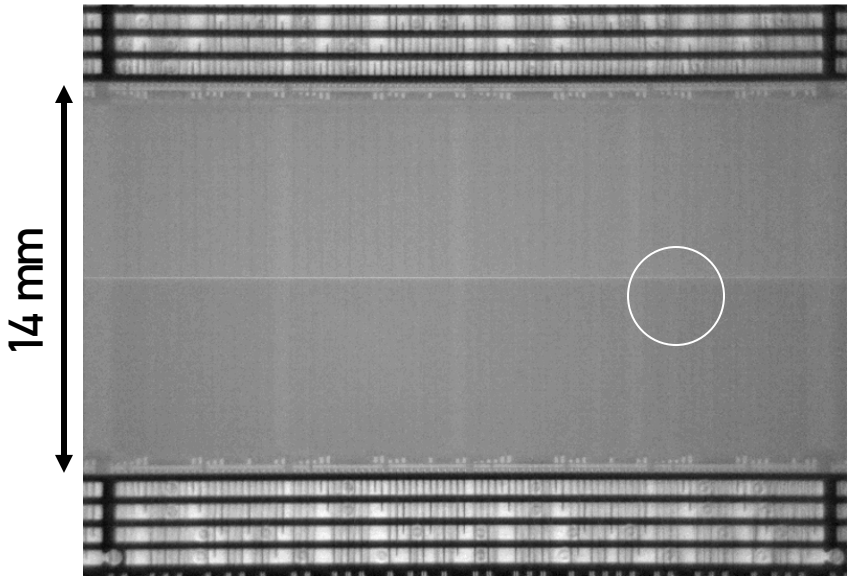
Sequentially ramp up power nets to nominal voltage – observed (transient) high currents →



Systematic measurement with thermal camera for every half unit to localise faults

Thermal camera on linear stage



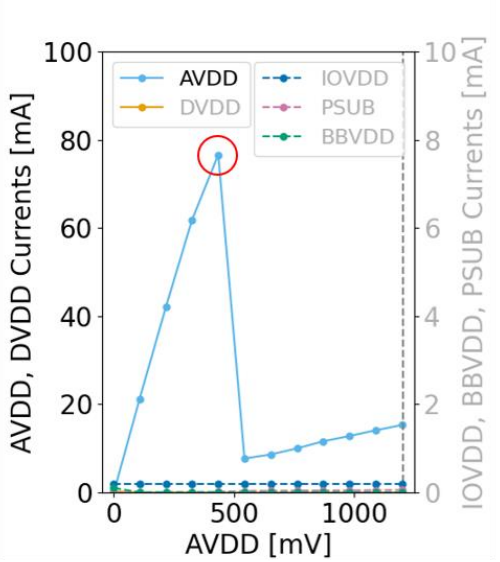


Measurement sequence

Impedances

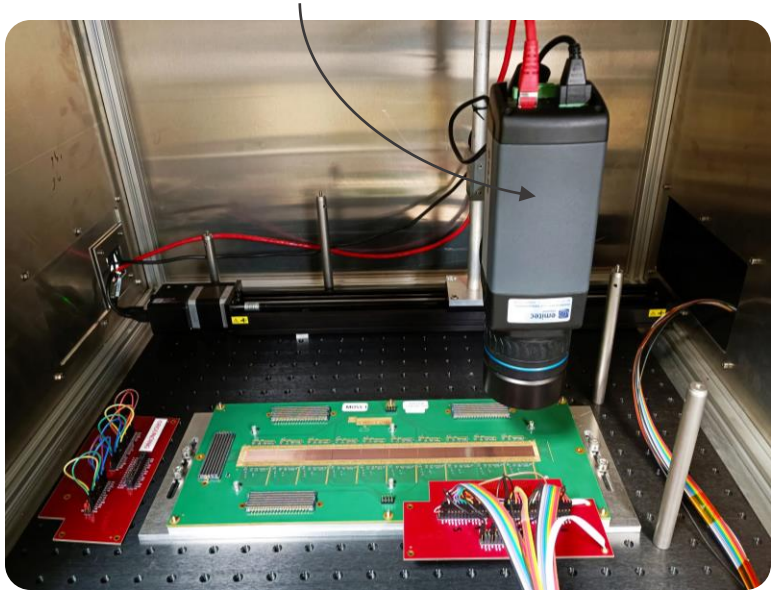
Power ramping

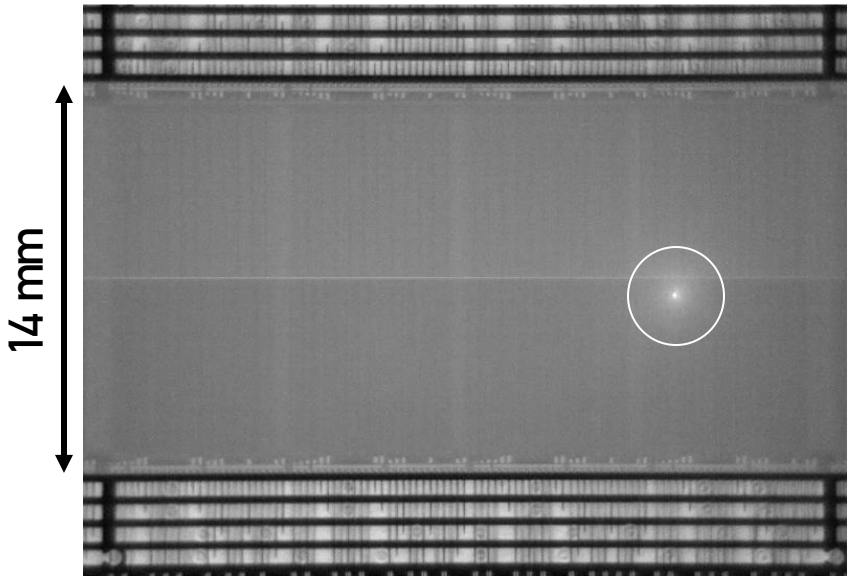
Sequentially ramp up power nets to nominal voltage – observed (transient) high currents →



Systematic measurement with thermal camera for every half unit to localise faults

Thermal camera on linear stage





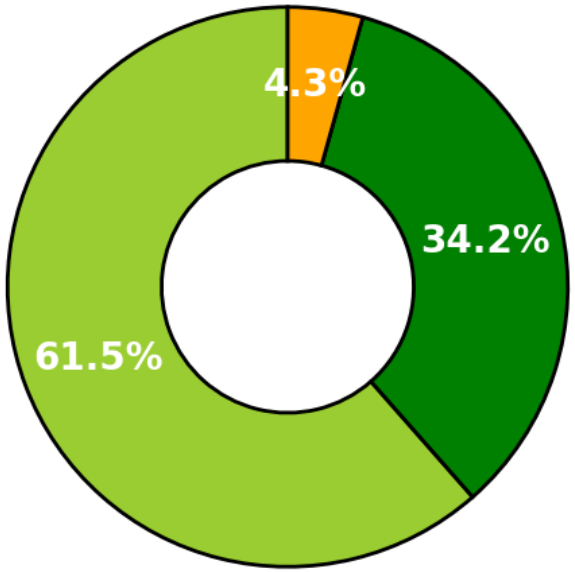
Measurement sequence

Impedances

Power ramping

Sequentially ramp up power nets to nominal voltage – observed (transient) high currents

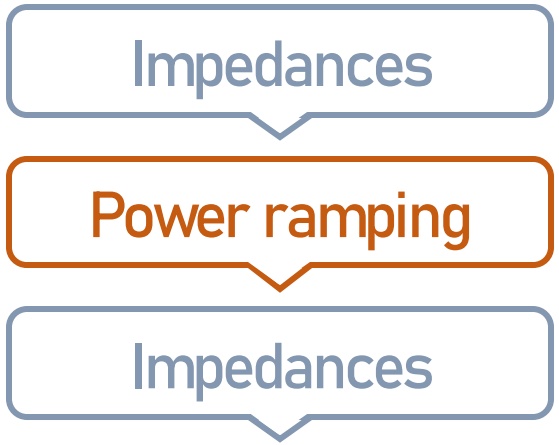
Systematic measurement with thermal camera for every half unit to localise faults



OK-I: Succeeding power on
OK-II: Succeeding power on with transient currents
LIMIT: Persistent high current

81 MOSS
1620 half units
psub: 0V

Measurement sequence



Repetition of Impedance measurement to confirm opening of shorts (change from low to high impedance)

Measurement sequence

Impedances

Power ramping

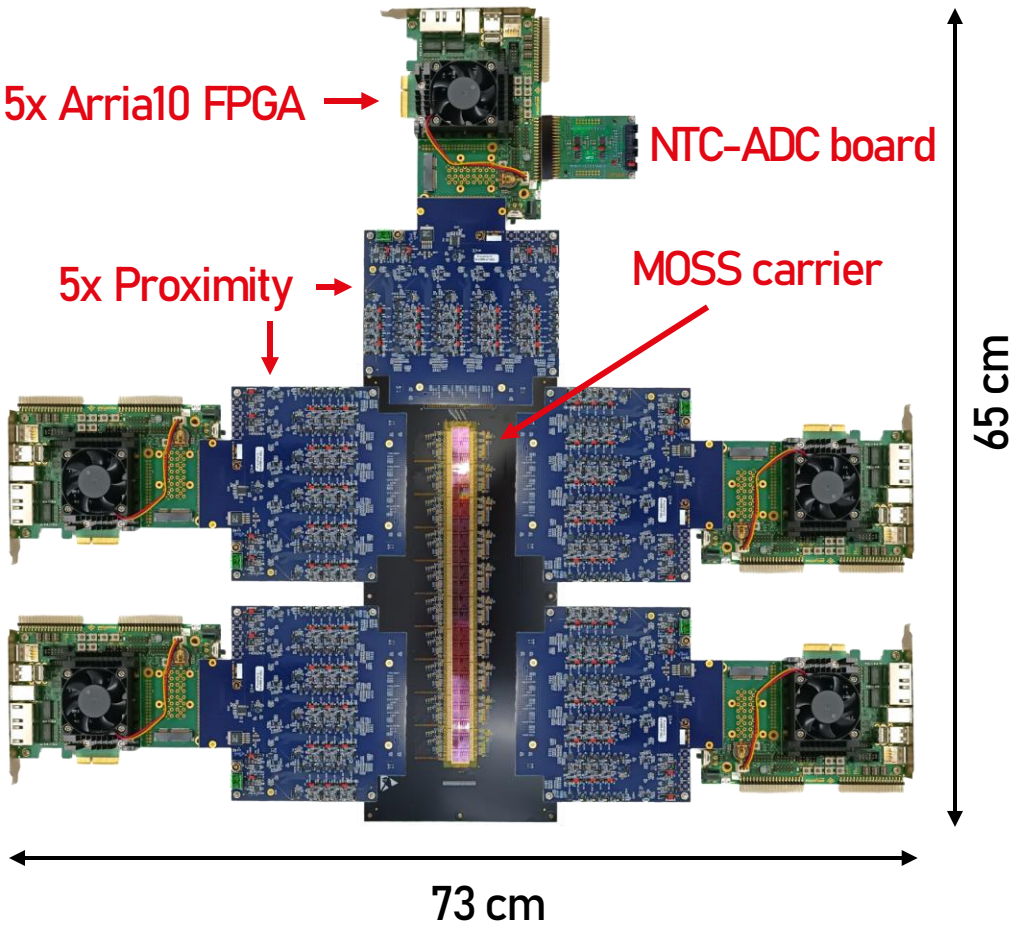
Impedances

Functional tests:

- Register scan
- Shift Register scan
- DAC scan
- Digital pulsing
- Analog pulsing
- Fake-hit rate scan
- Threshold scan

> 99% pass rate

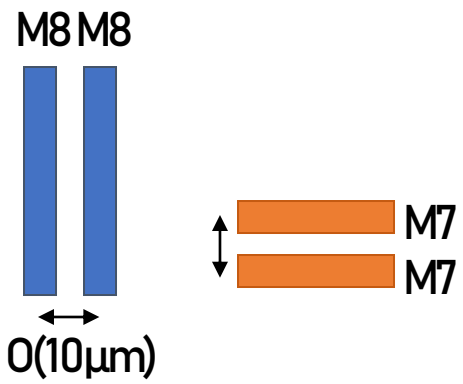
Half Units passing the power ramps (OK-I and OK-II) are functionally tested



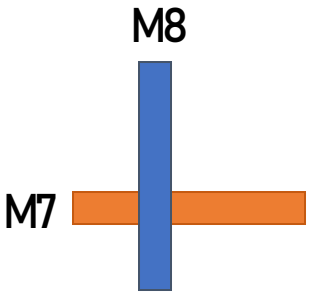
Shorts, and how to find them

Use data on impedances, powering, and hot spots to find the root cause of shorts

- Conservative spacing of metal lines, especially power grid O(10µm)

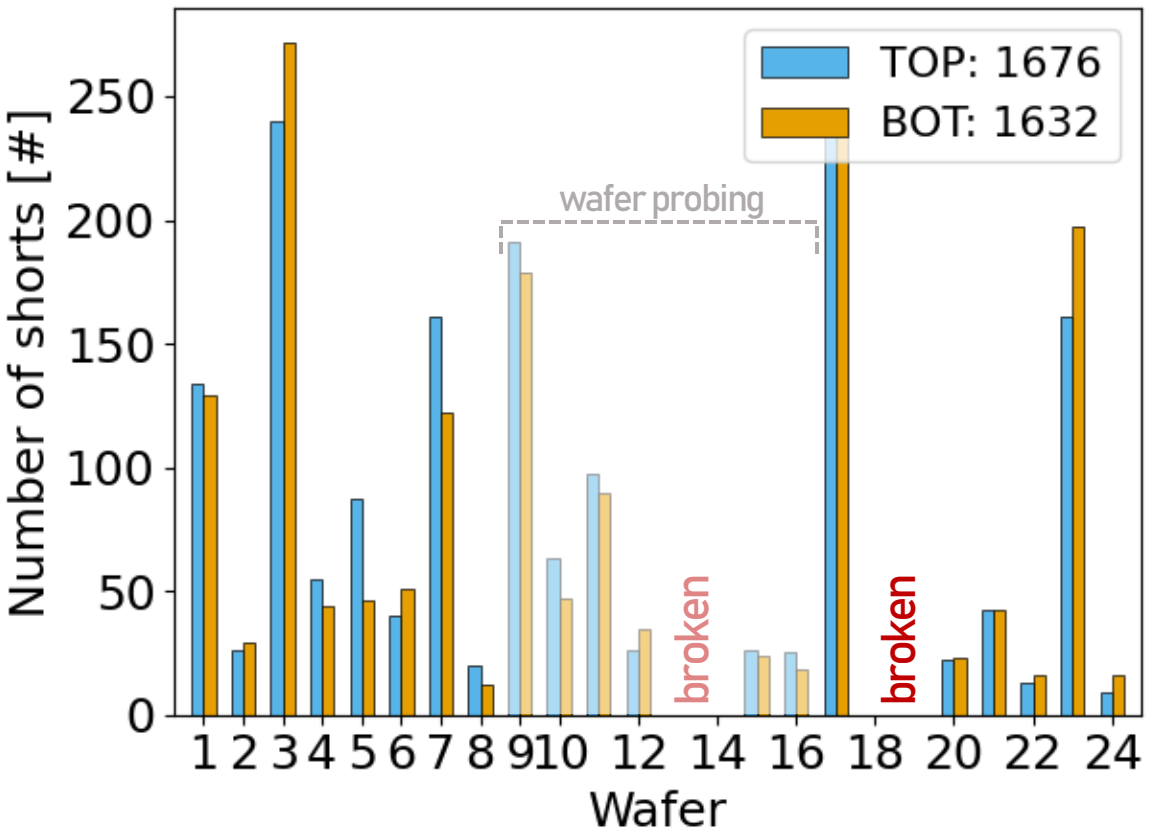


- Recommendation: Use different metal layers for critical paths



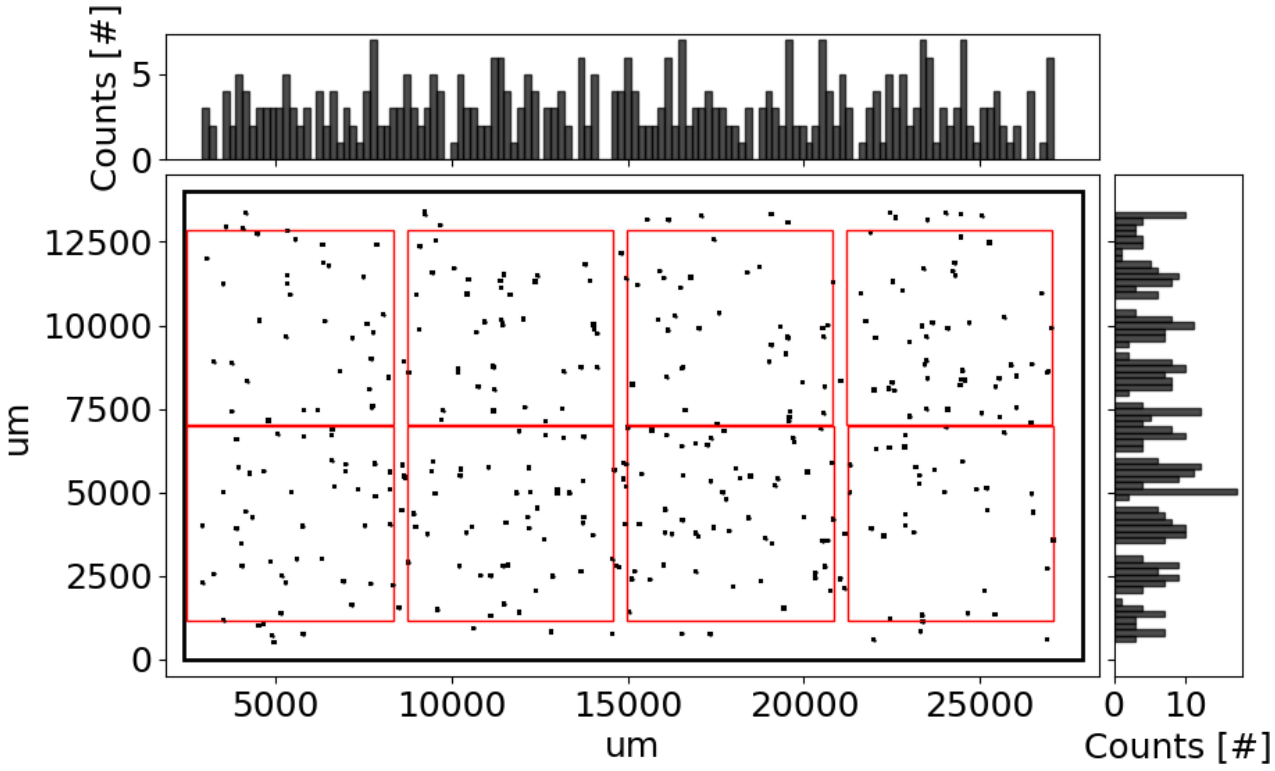
Hypothesis formation on shorts

- Wafer-wafer fluctuation
- Comparable number of shorts in TOP/BOT: metal line spacing independent



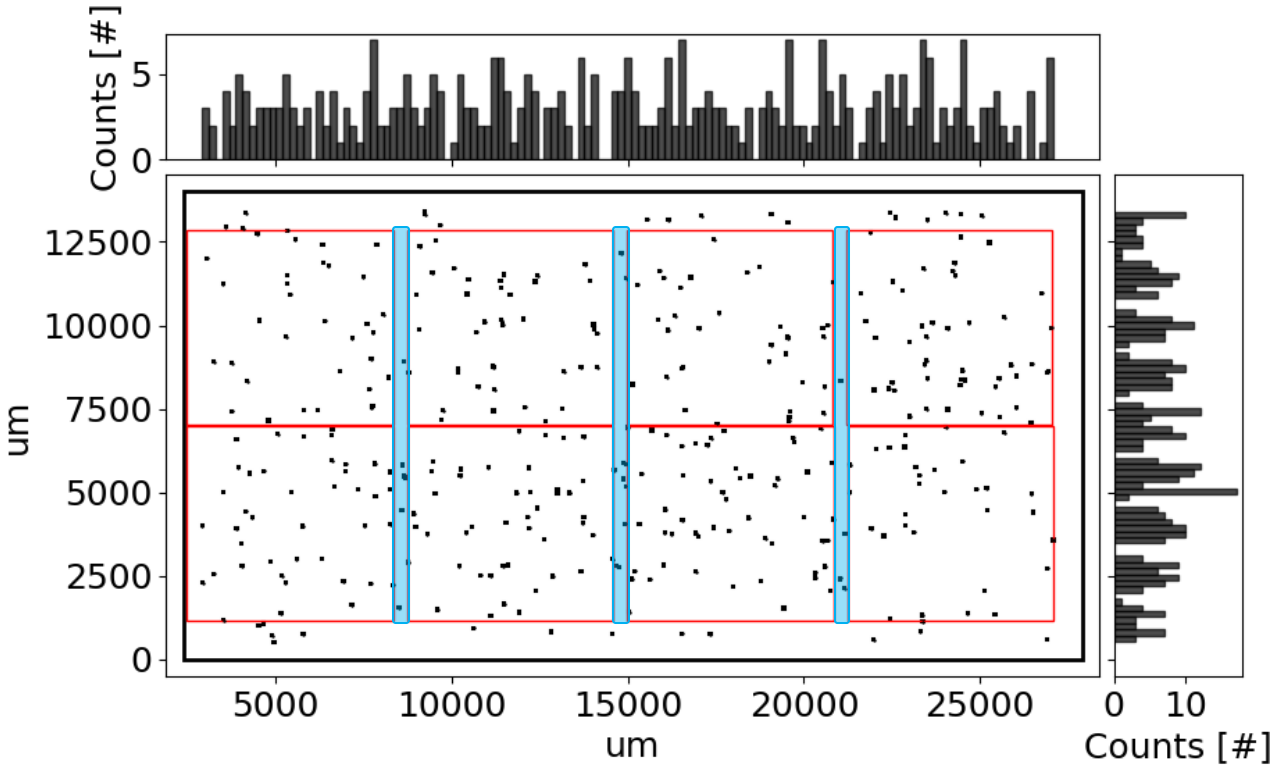
Hypothesis formation on shorts

- Wafer-wafer fluctuation
- Comparable number of shorts in TOP/BOT: metal line spacing independent
- Hotspots where only top two metals are routed (M7/M8)



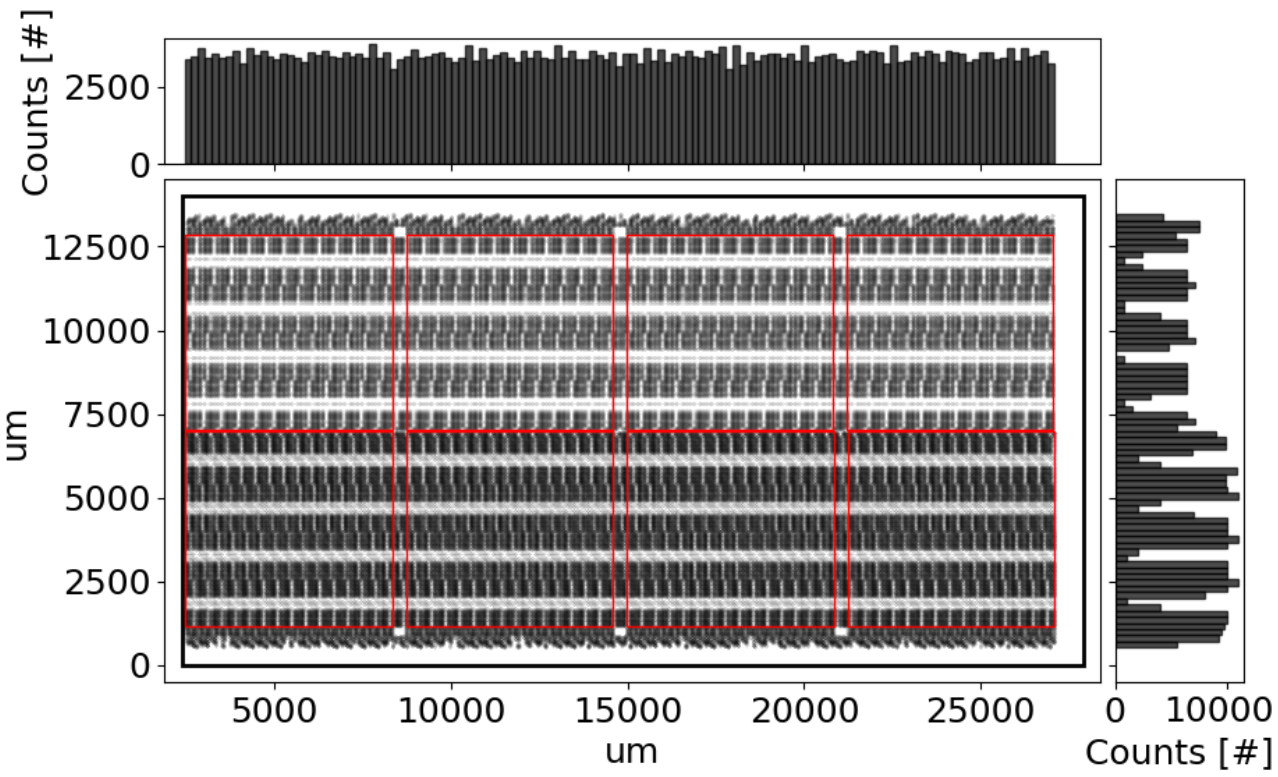
Hypothesis formation on shorts

- Wafer-wafer fluctuation
- Comparable number of shorts in TOP/BOT: metal line spacing independent
- Hotspots where only top two metals are routed (M7/M8)



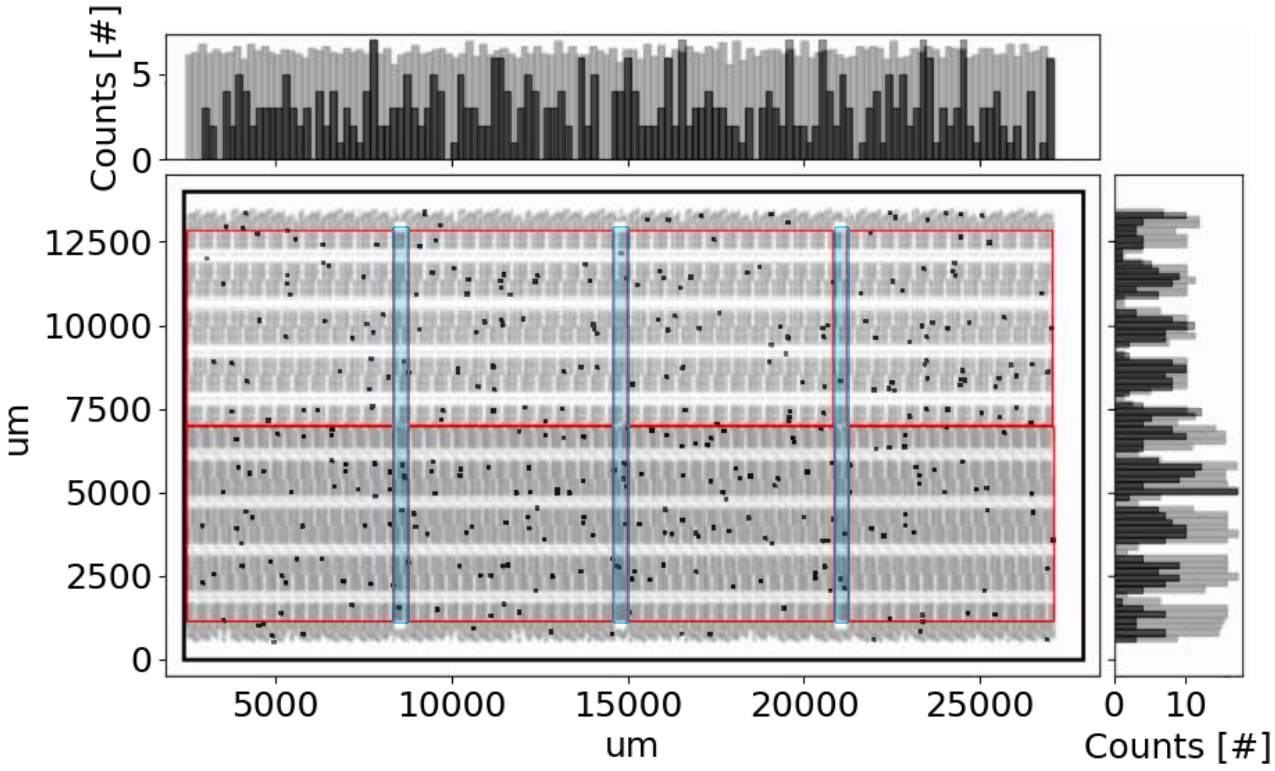
Hypothesis formation on shorts

- Wafer-wafer fluctuation
- Comparable number of shorts in TOP/BOT: metal line spacing independent
- Hotspots where only top two metals are routed (M7/M8)
- M7/M8 [specific] locations match hotspot locations



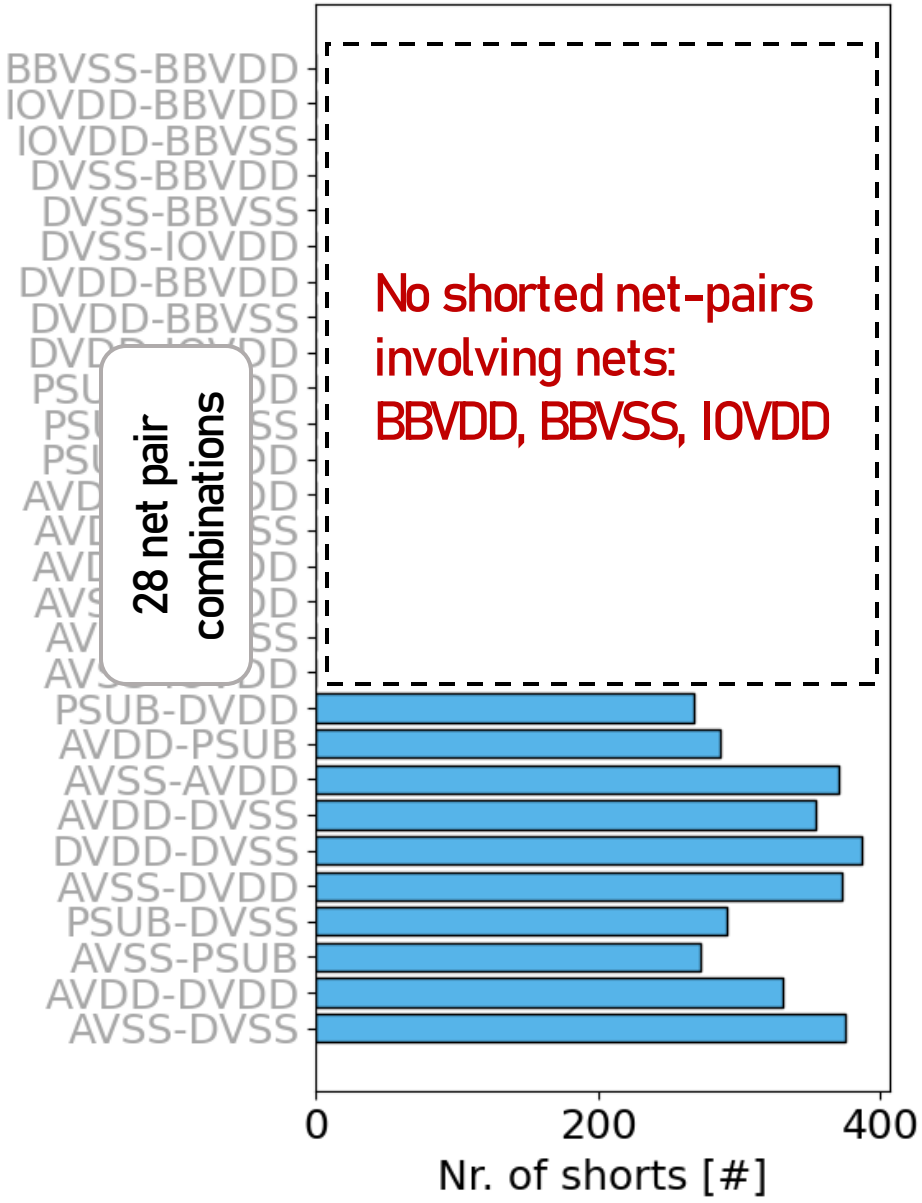
Hypothesis formation on shorts

- Wafer-wafer fluctuation
- Comparable number of shorts in TOP/BOT: metal line spacing independent
- Hotspots where only top two metals are routed (M7/M8)
- M7/M8 [specific] locations match hotspot locations



Hypothesis formation on shorts

- Wafer-wafer fluctuation
- Comparable number of shorts in TOP/BOT: metal line spacing independent
- Hotspots where only top two metals are routed (M7/M8)
- M7/M8 [specific] locations match hotspot locations
- No shorts on 3 (of 8) power nets, where M7/M8 metals do not [exhibit specific features]

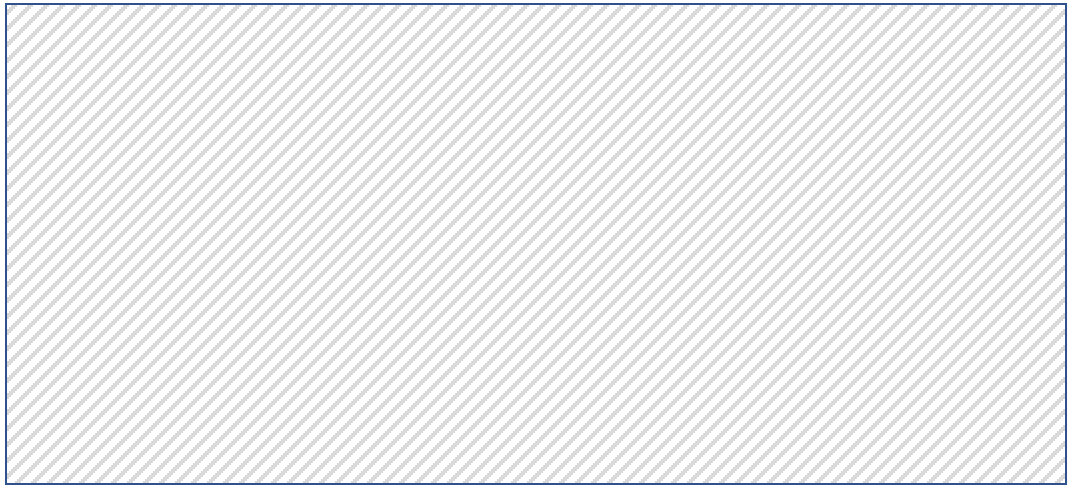


Hypothesis formation on shorts

- Wafer-wafer fluctuation
- Comparable number of shorts in TOP/BOT: metal line spacing independent
- Hotspots where only top two metals are routed (M7/M8)
- M7/M8 [specific] locations match hotspot locations
- No shorts on 3 (of 8) power nets, where M7/M8 metals do not [exhibit specific features]

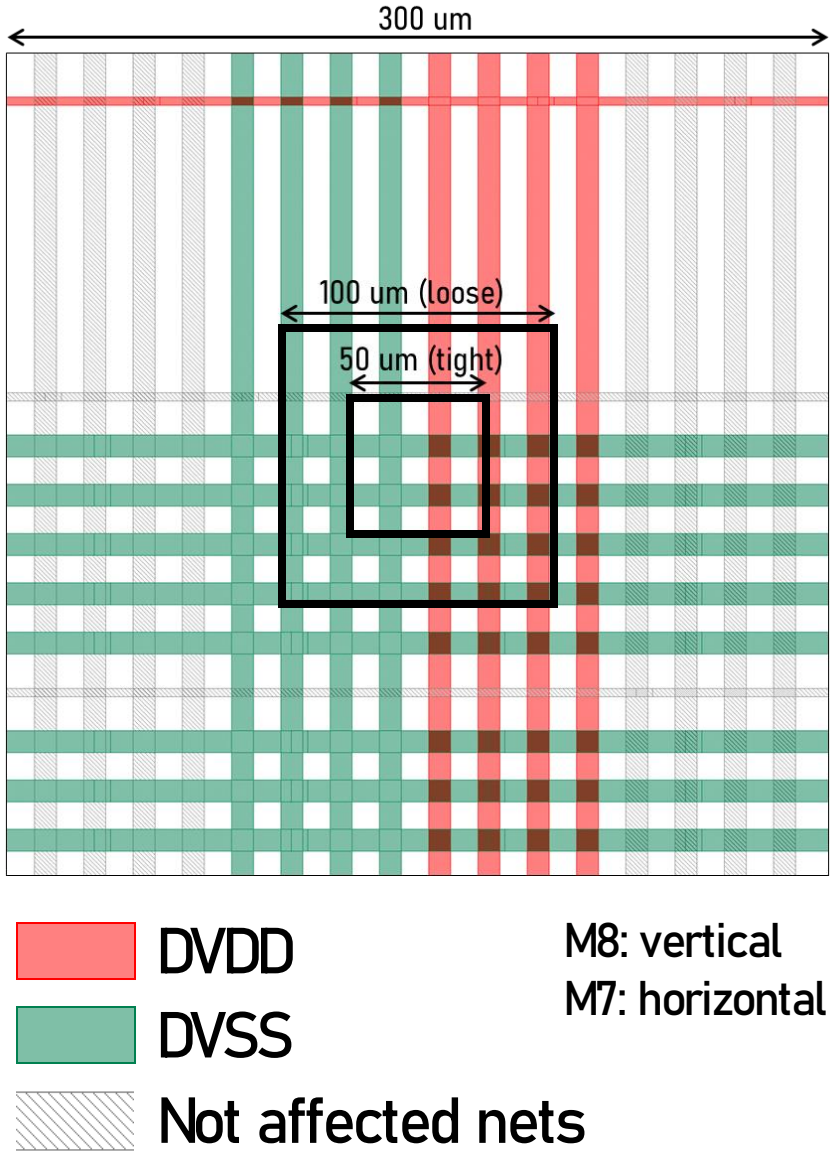
Hypothesis A:

[Specific] shorts [involving] M7-M8 metals, at [specific] locations



Correlation of power nets and hot spot locations

- Correlate single hotspot with single shorted net-pair
- Correlate hotspot location extracted with thermal camera with location in chip design
  Resolution window: 50µm (best) / 100µm (average)



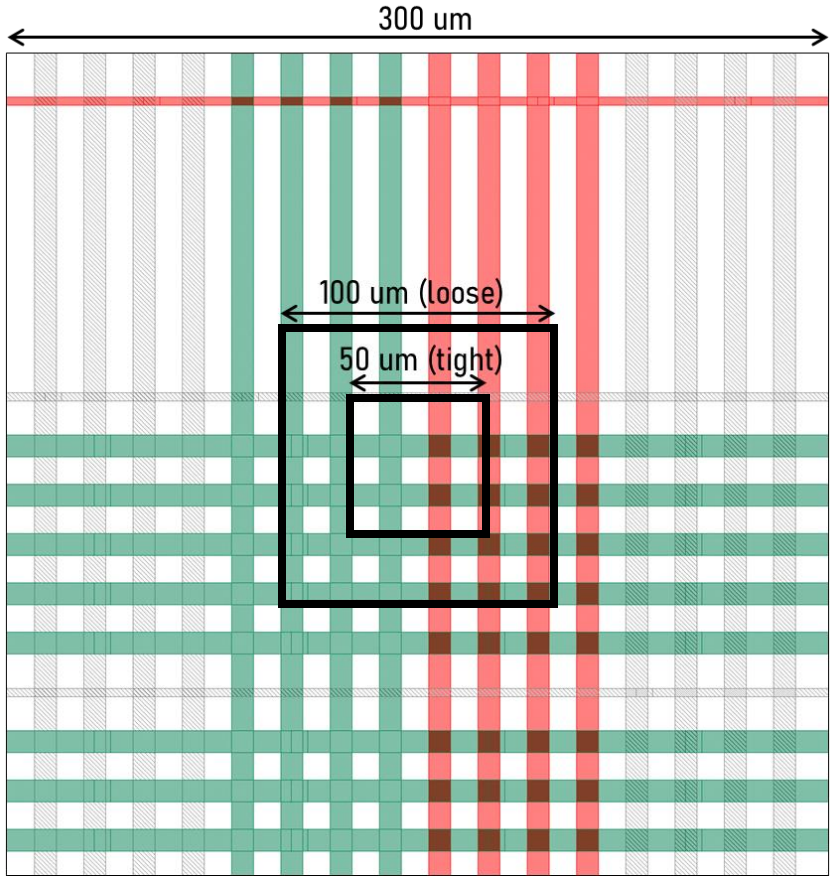
Correlation of power nets and hot spot locations

- Correlate single hotspot with single shorted net-pair
- Correlate hotspot location extracted with thermal camera with location in chip design

  Resolution window: 50µm (best) / 100µm (average)

Resolution window [um²]	Hypothesis A compatible	Hypothesis B compatible	Total counts*
50 x 50	89 %	16 %	156
100 x 100	94 %	31 %	156

*155/156 are compatible with Hypothesis A after individual analysis



DVDD

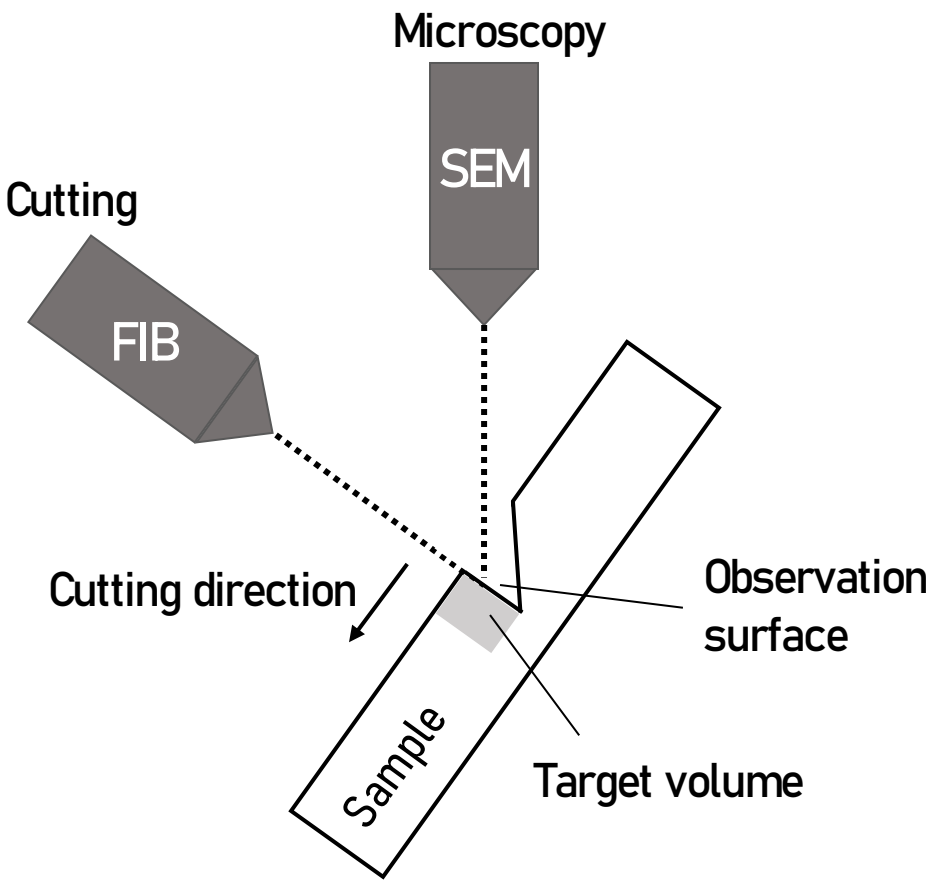
DVSS

Not affected nets

M8: vertical

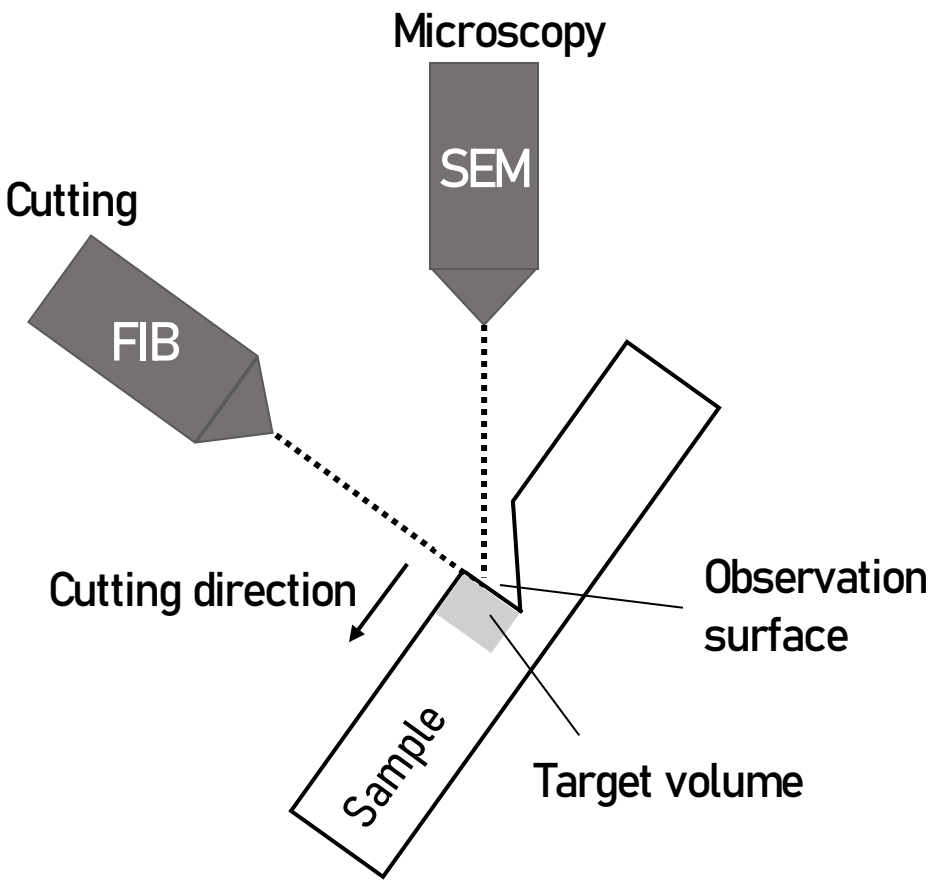
M7: horizontal

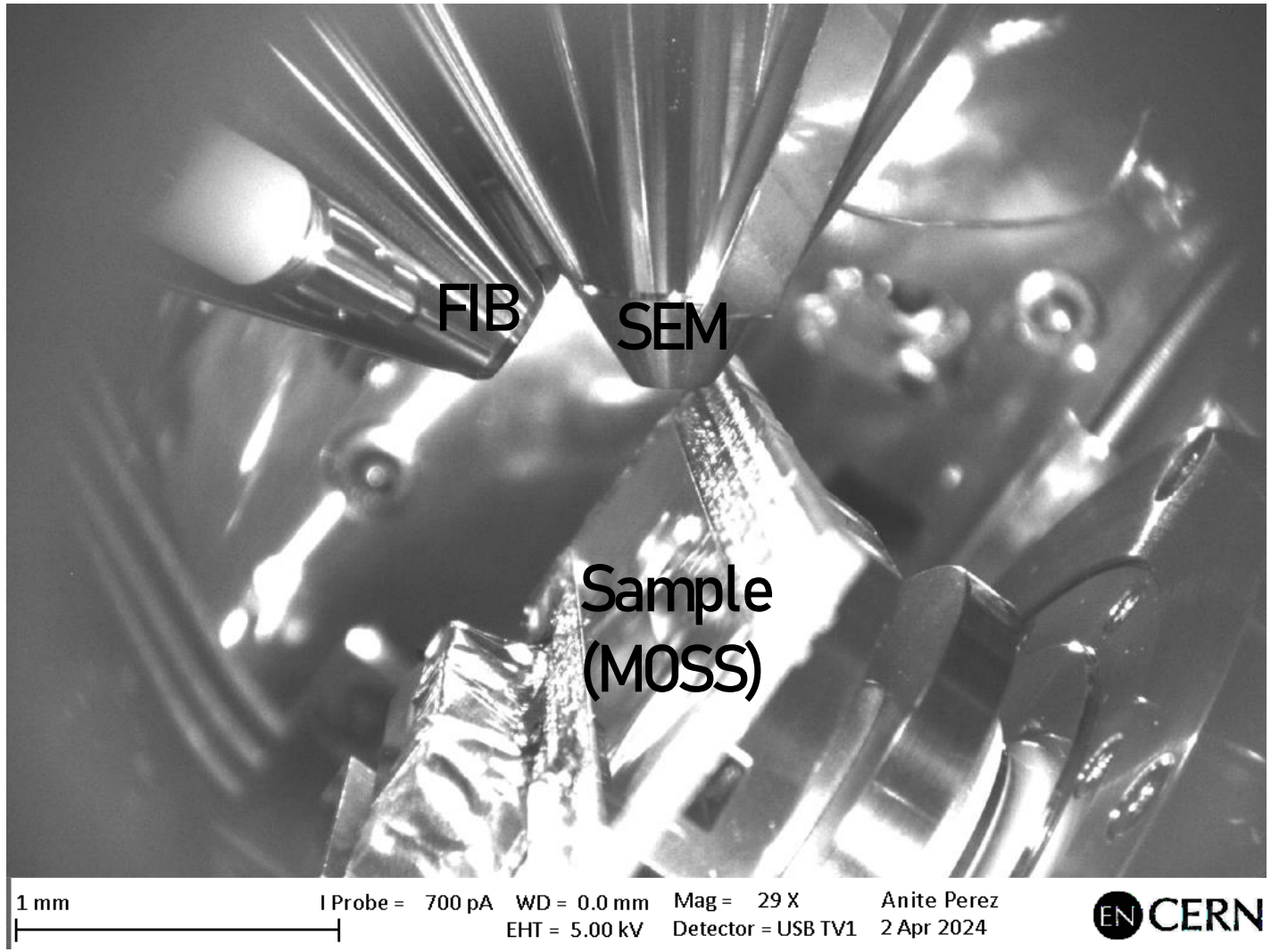
FIB-SEM analysis



FIB-SEM: Focused Ion Beam – Scanning Electron Microscopy

FIB-SEM analysis





M7-M8 short

- Clear connection between M7-M8 layer
- Chemical analysis: M7-M8 connection is copper

EDS = Energy-dispersive X-ray spectroscopy

M7-M8 short (after burn through)

- FIB-SEM analysis after burning through a short (additional MOSS)
- Cavity formation around the fault
- O(10 nm) gap – long term stability not guaranteed (thermal/mechanical deformation):
  -> Faults not seen when powering on without impedance or power ramping/thermal camera

Confirmation and mitigation of M7-M8 shorts

- M7/M8 are processed differently than lower metal layers -> occurrence of shorts only in M7/M8 is plausible
- Foundry confirms processing issue in M7/M8 with this lot

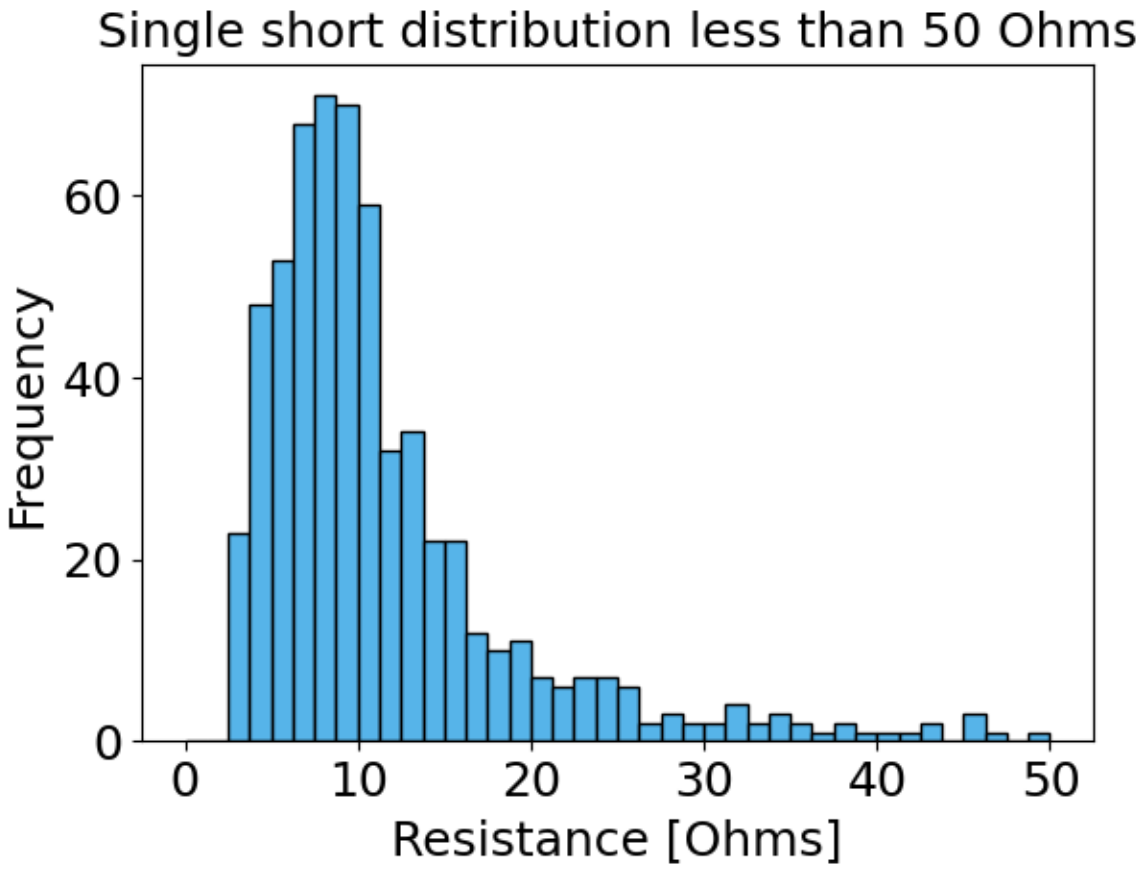
- For next chip (ER2, MOSAIX): M7/M8 will be replaced by a new (thicker) metal stack. Foundry confirmed no issues with new stack, and provided corresponding design rules

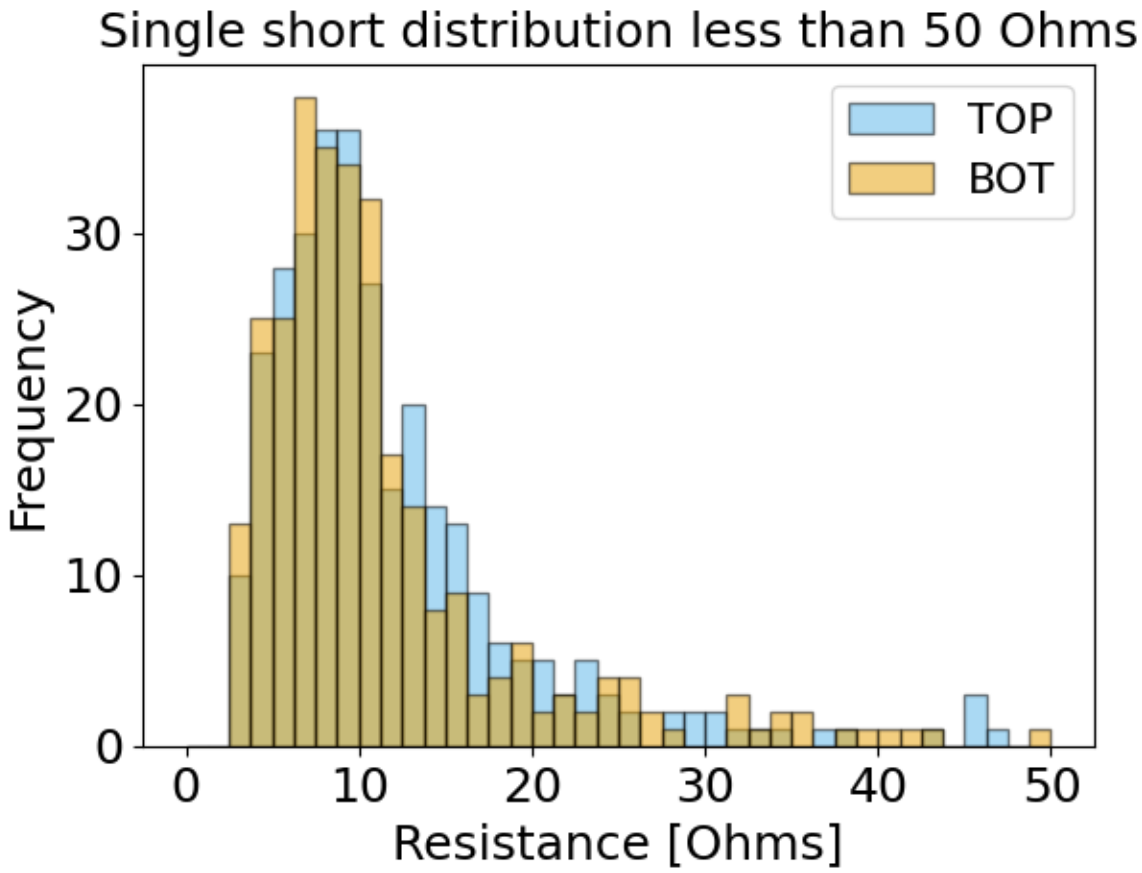
Summary

- Impedance measurements and power ramps show shorts on all wafers
- Developed dedicated measurement setups and failure analysis methods
- Root cause of shorts identified, confirmed by Foundry
- Affected layers (M7/M8) in metal stack will be changed for lower resistivity in next submission (MOSAIX)

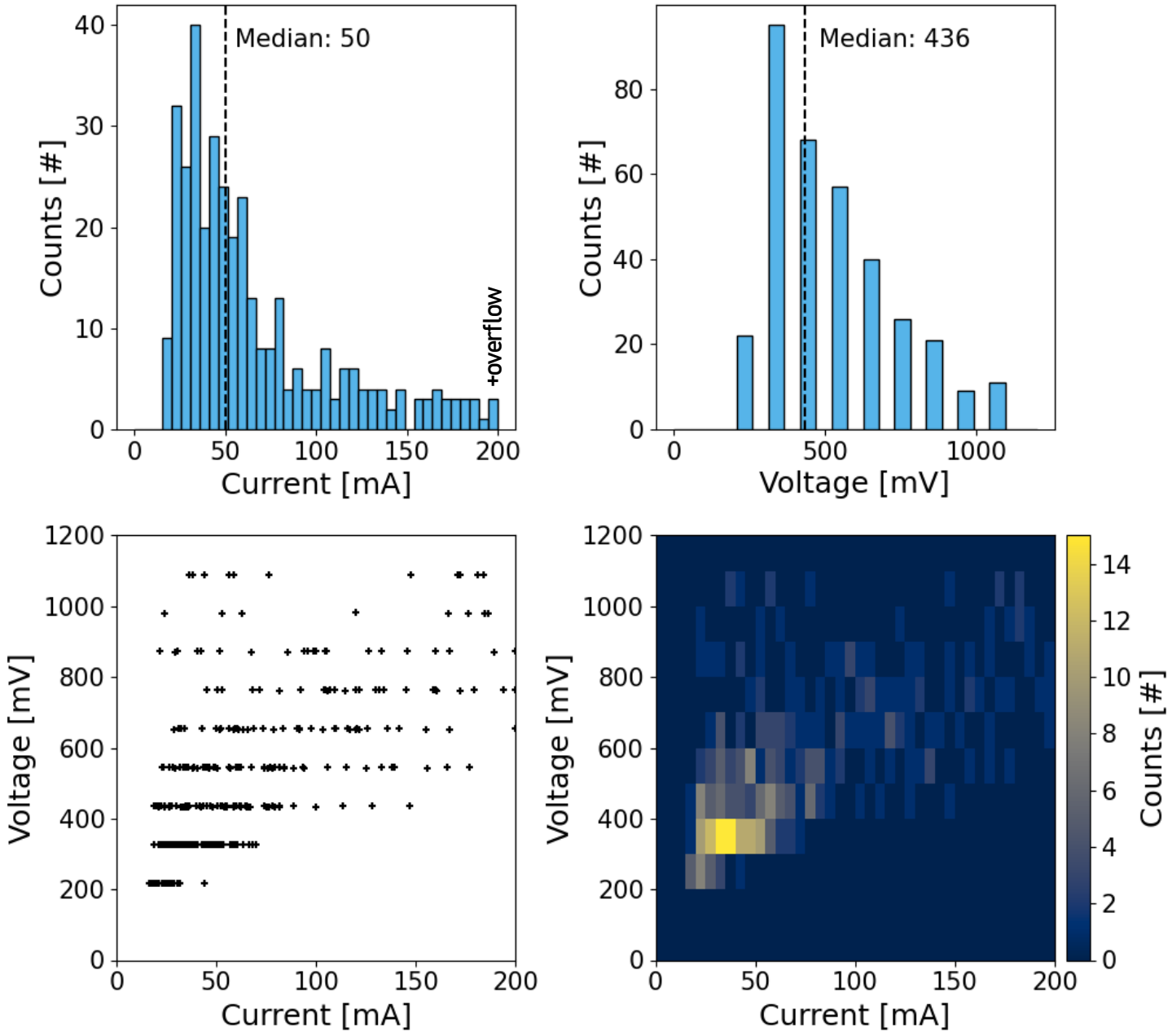
BACKUP

Impedance distribution single short



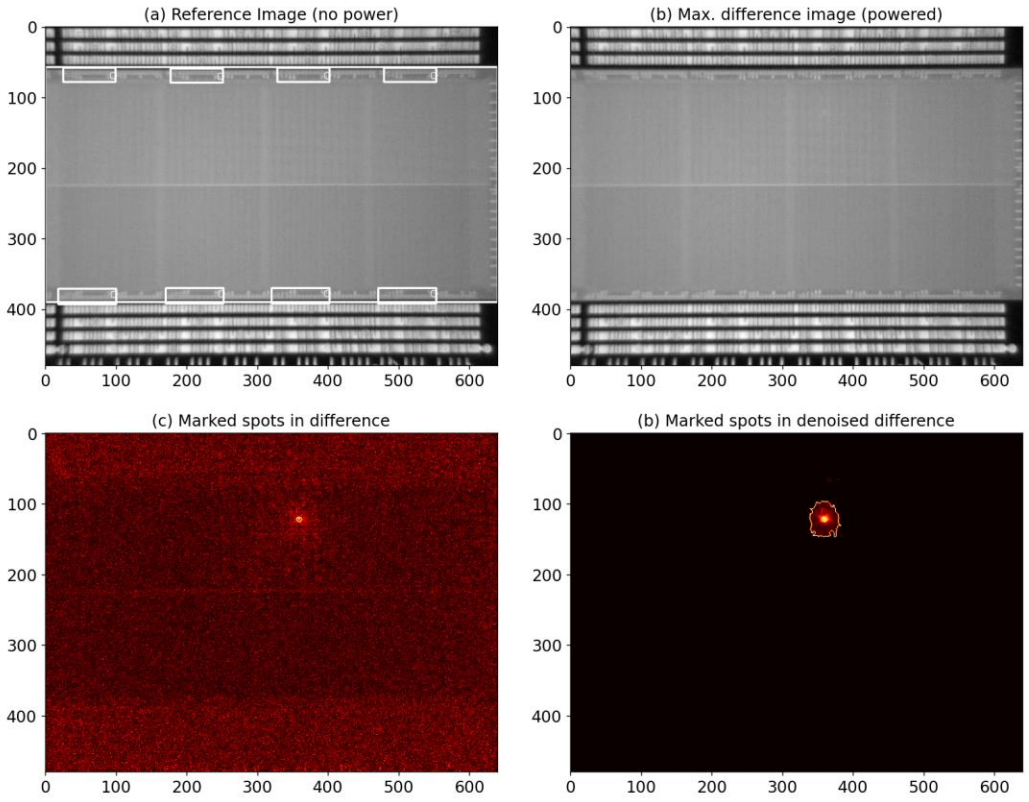


Burn through currents and voltages

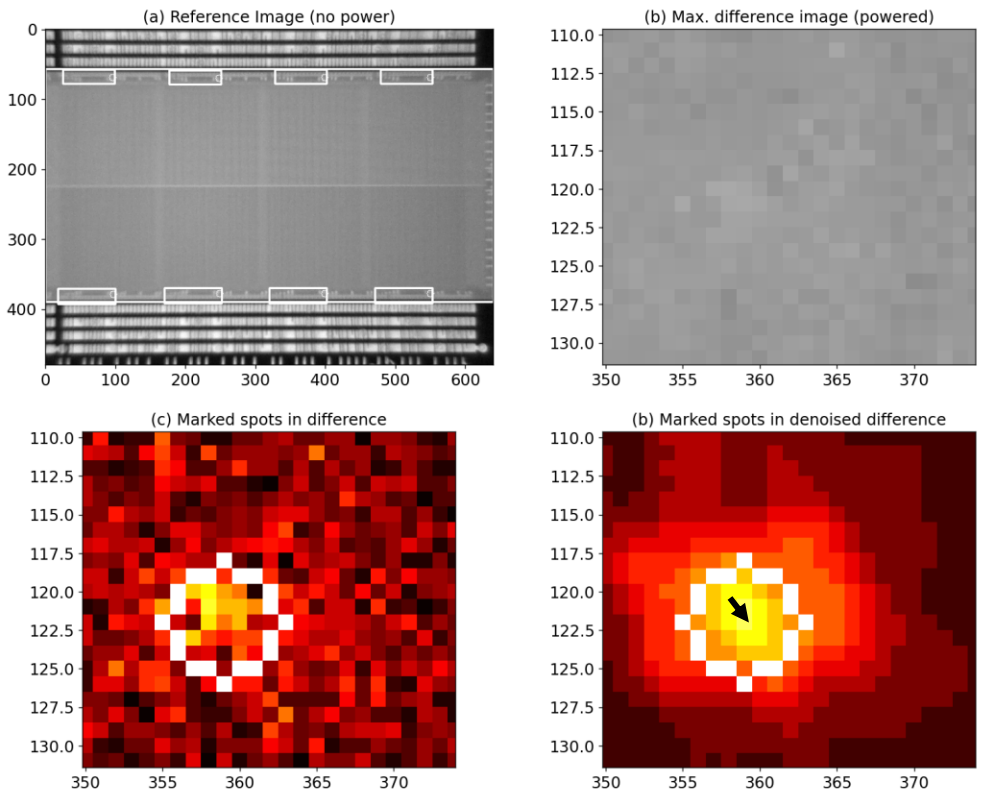


- Currents/voltages at burn through
- Condition: >10mA drop
- Set of 349 jumps
- 0V psub data set

Example of extended resolution window



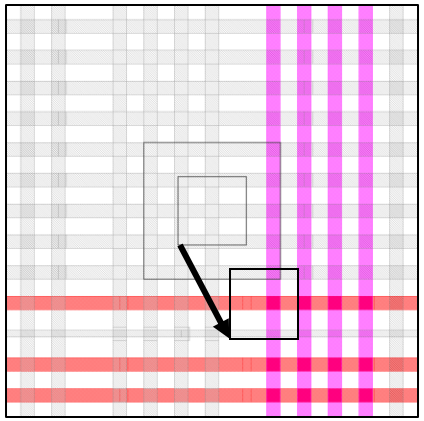
zoom



Very faint hotspots/no unique hot pixel

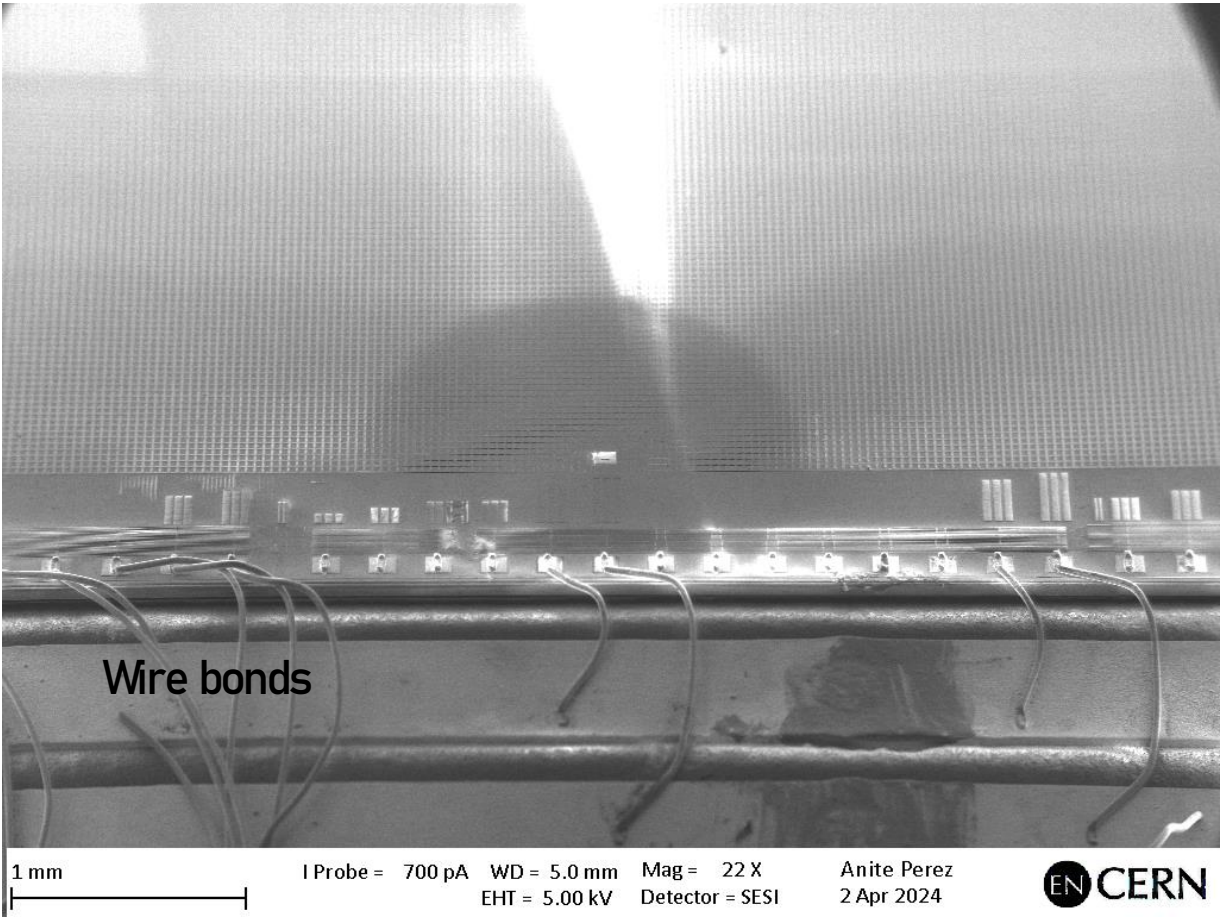
Here: Compatible in 150 um x 150 um window only

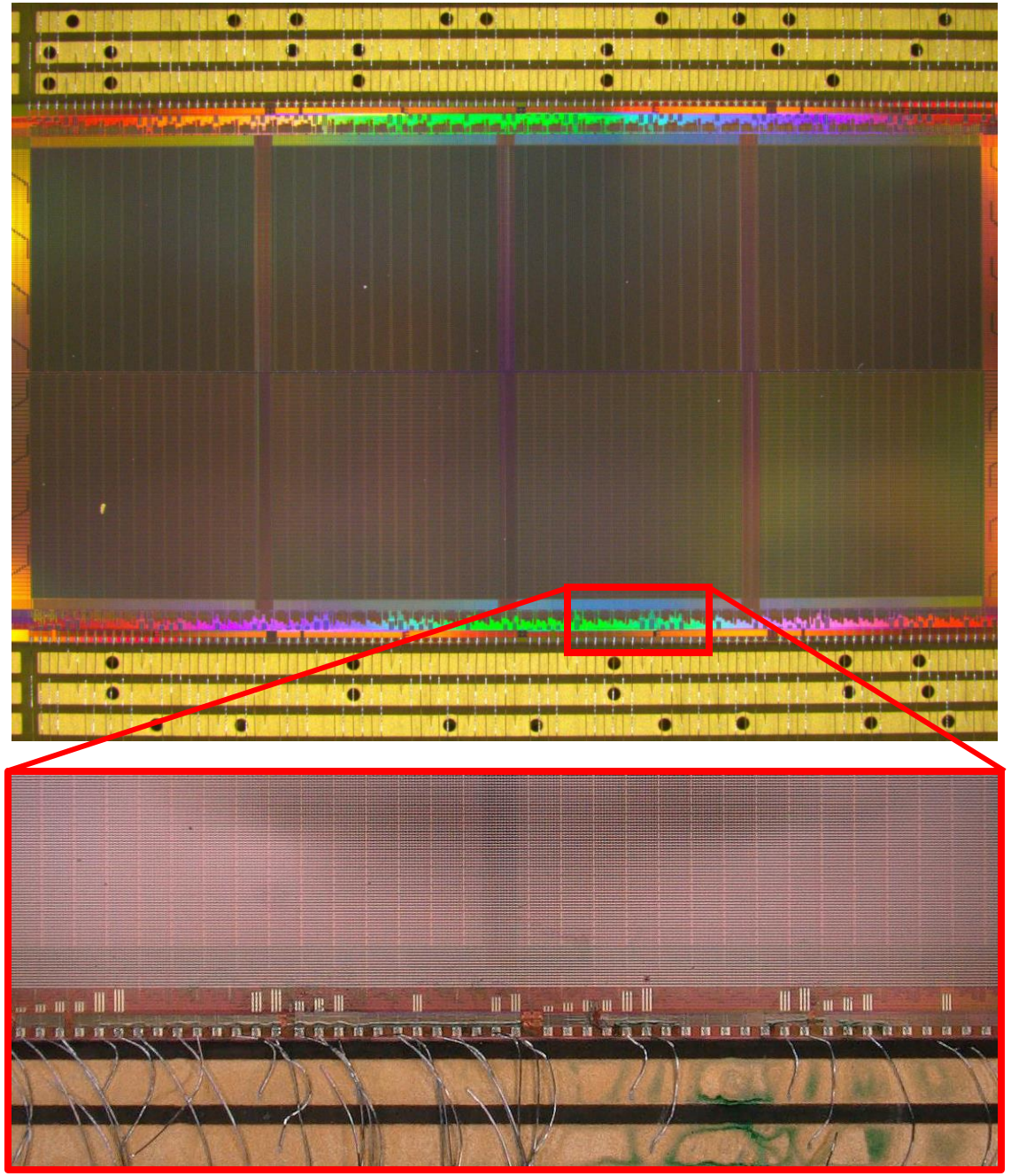
After re-checking, centre of gravity matches corresponding power net crossing



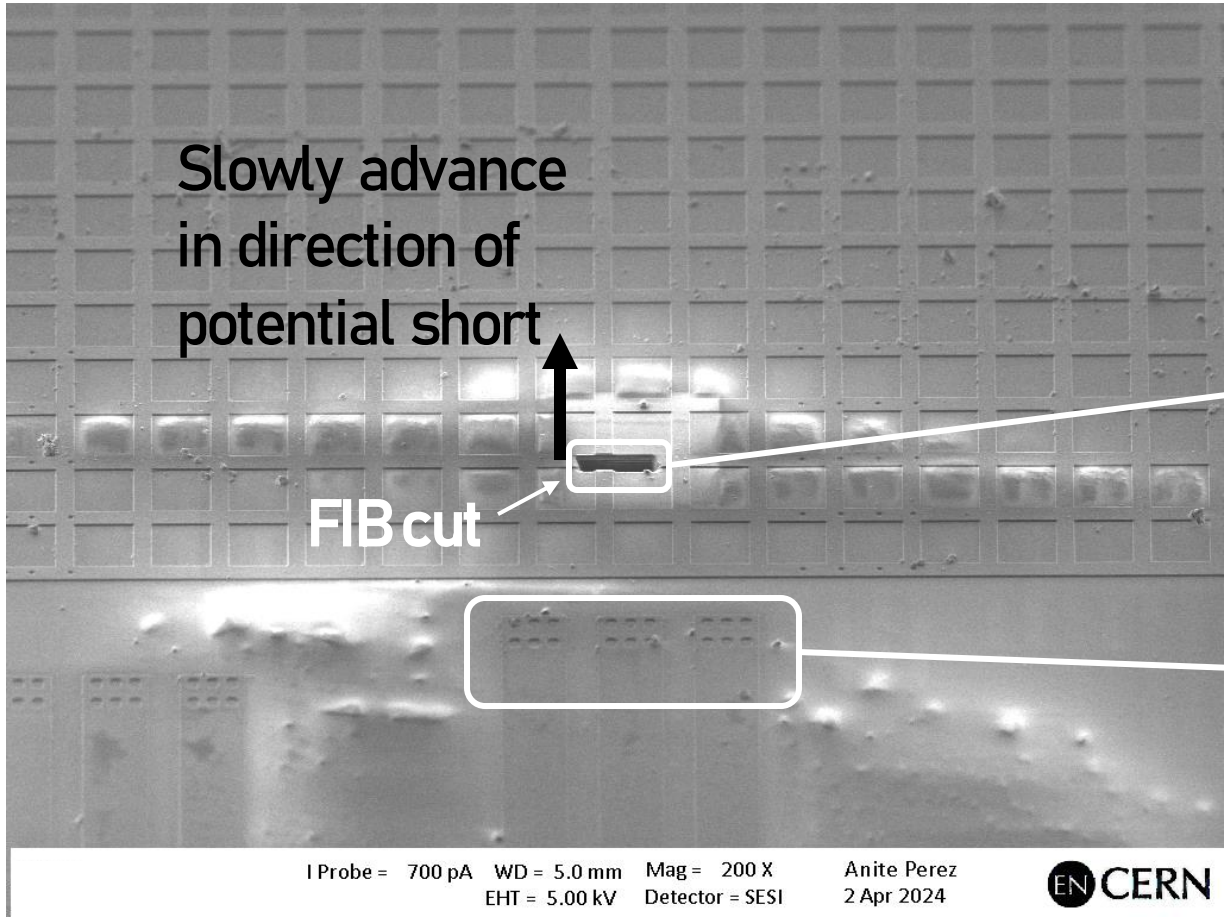
Chip layout overlay

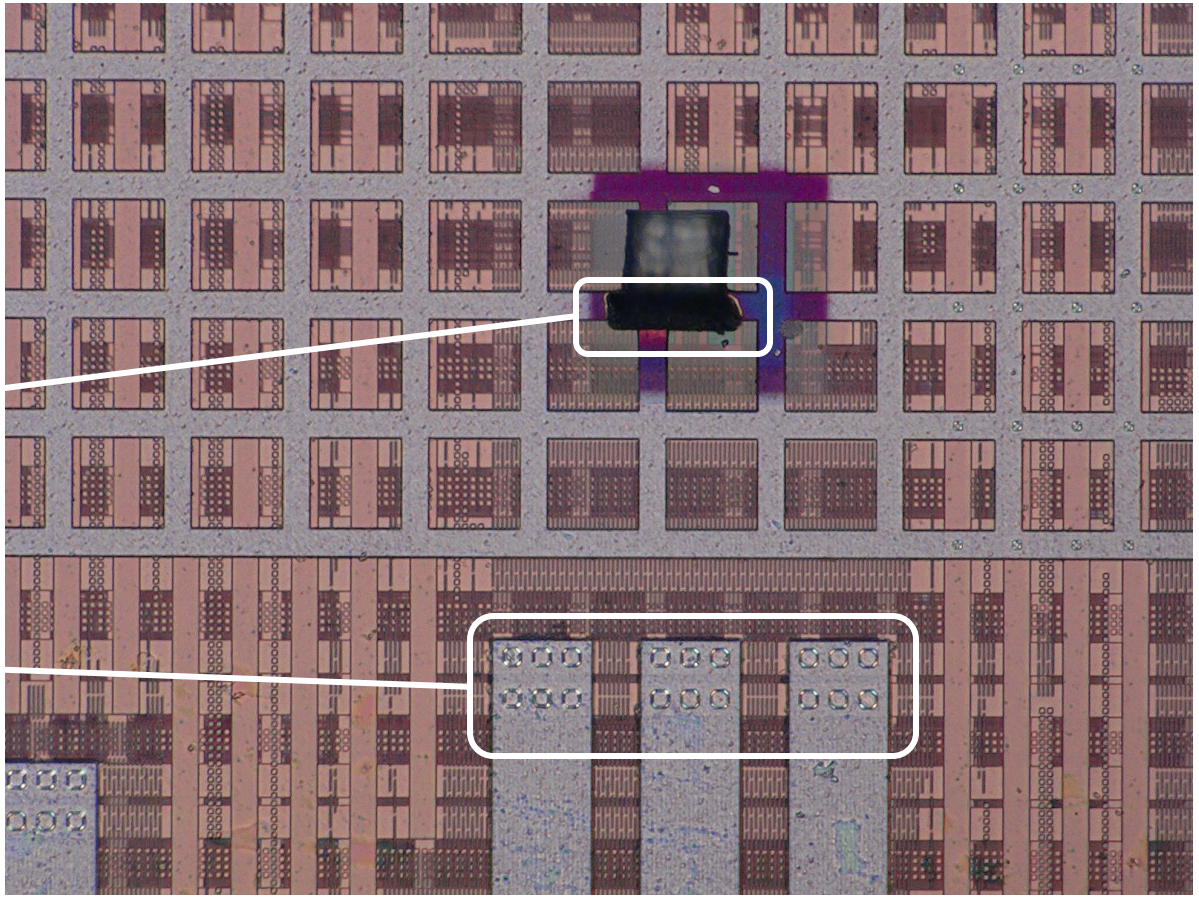
Localisation – FIB



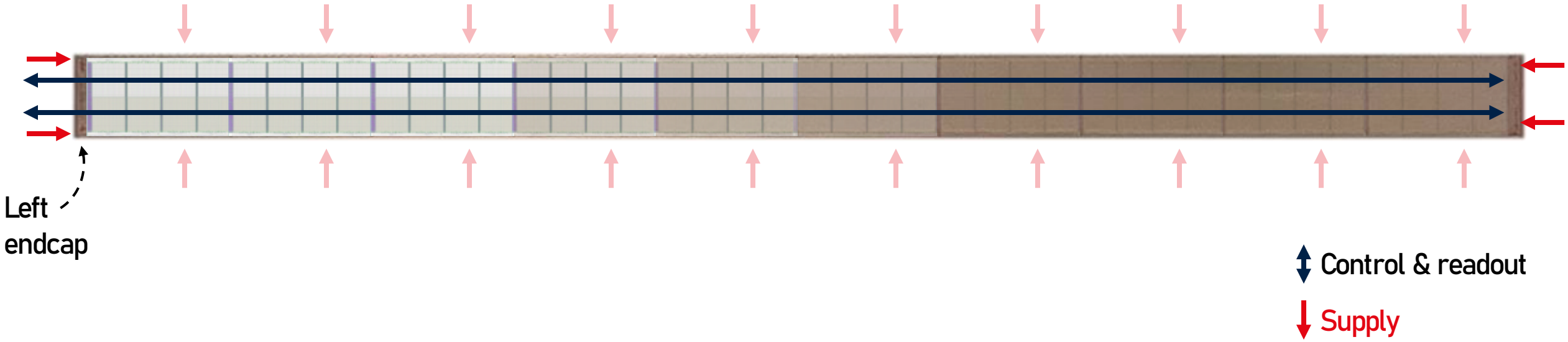


Localisation – FIB





MOSS – short edge communication



Test Half Units in parallel from left endcap via **stitched backbone** (top/bottom):

- Addressing 10 half units simultaneously
- Data transfer over 26 cm (with signal regeneration)
- Readout at left endcap at up to 40 Mbps / sensor

64 Power Domains + Substrate
107 Supply Nets
2192 bonding pads
390 Digital I/Os, 480 Analog I/Os