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Yield Characterisation and Failure Analysis of the Monolithic Stitched Sensor MOSS for ALICE ITS3

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The Monolithic Stitched Sensor (MOSS) is a prototype silicon pixel sensor of 26 x 1.4 cm^2 size with the primary goal of understanding the stitching technique and yield. It is a proof-of-concept chip for the final sensors of the ALICE ITS3 upgrade. Given the large size, high yield is paramount for the ITS3 sensors and an in-depth yield characterization was performed on MOSS sensors. Short circuit failures were observed across 24 wafers with varying frequency. Dedicated test systems and failure analysis methods were developed, and root cause analysis was performed. Methods, results, and potential mitigation techniques will be presented in this contribution.

Summary (500 words)

The ALICE experiment at the LHC at CERN will upgrade its innermost three tracking layers with the new Inner Tracking System 3 (ITS3). The ITS3 is based on wafer-scale, bent, monolithic active pixel sensors of up to 27 x 9.4 cm^2 size. To manufacture sensors larger than the design reticle size, stitching is employed. The Monolithic Stitched Sensor MOSS has been designed and manufactured to assess the feasibility of the stitching technique in terms of yield and performance for application in ALICE ITS3 and high-energy physics.

The MOSS sensor consists of 10 repeated sensor units (RSU) on one die of silicon, electrically interconnected via the on-chip metal stack stitching. It is fabricated in 65nm CMOS imaging technology. A lot of 24 wafers with 6 MOSS sensors each have been produced. Each RSU of the MOSS sensor has an independent top and bottom half unit. Altogether, 20 half units per chip with independent power domains exist. Each half unit is interfaced individually via bonding pads. This granular design allows for characterization in case of faults on part of the half-units, and detailed yield studies.

The large size of the ITS3 sensors does not allow to select chips without faults. Thus, the final sensor design includes functionality to disconnect faulty sub-units from the global power nets. Final design granularity and number of wafers to be produced are extrapolated from MOSS yield figures.

Each MOSS half unit has 8 power domains. An impedance measurement is performed for all $binom82 = 28$ net pair combinations for all 20 half units per chip. A semi-automated procedure was developed. Tests are performed both on wire bonded chips and on wafers with a probe card before thinning and dicing. Impedance measurements give an initial number of short circuits between power nets on the chips.

Individual power nets are ramped to nominal voltage, and currents measured. A thermal camera is used to localize hotspots, corresponding to short circuits. The failure site is correlated with chip layout, power net impedances, and currents during powering. This information allows to formulate a hypothesis on the predominant failure mode. Focused Ion Beam (FIB) and electron microscopy were employed to visualize an exemplary short circuit in the metal stack of the MOSS sensor, pointing to processing issues.

Yield figures are extracted from impedance, powering, and functional measurements, and provide a basis for the required design granularity of the final ITS3 sensors. The MOSS design is fully functional if no short circuits are observed. Half units with shorts were successfully operated, if shorts are opened by passing through a sufficiently high current. Succeeding impedance measurements show that shorts are removed permanently. Functional tests confirm these units can be operated according to specifications.

In this presentation, the focus will be on the yield of the MOSS sensor. Measurement techniques for failure and root cause analysis will be presented. The results of these measurements and yield figures will be shown. Potential mitigation techniques and implications on the chip design will be discussed.

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