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Design of 28nm readout ASIC prototype for 3D-integrated LGAD sensors

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Highly granular precision timing detectors are required to achieve scientific breakthroughs across HEP, NP, BES, and FES. To enable the development of these detectors, 3D-intgration between advanced sensor wafers and scaled CMOS technology nodes is required but is currently cost-prohibitive for use in scientific applications. Closing this technology gap is the joint SLAC, FNAL and LLNL effort pursuing development of LGAD structures compatible with fabrication in commercial 12-inch wafer processes that can be cost-effectively 3D-integrated with high-performance readout ASICs under development. The design of the first ASIC prototype is presented.

Summary (500 words)

Highly granular precision timing detectors are required to achieve scientific breakthroughs across HEP, NP, BES, and FES applications, and their critical need was highlighted by DOE BRN, European Strategy for Particle Physics, and Snowmass. To enable the development of these detectors, 3D-intgration between advanced sensor wafers and scaled CMOS technology nodes is required but is currently cost-prohibitive for use in scientific applications and experiments. Closing this technology gap is the main objective of the joint SLAC, FNAL and LLNL effort "3D Integrated Sensing Solutions", supported by DOE's Accelerated Innovation in Emerging Technologies grant. In collaboration with leading semiconductor industry partner, this effort is pursuing development of LGAD structures compatible with fabrication in commercial 12-inch wafer processes that can be cost-effectively 3D-integrated with readout ASICs. In parallel with the LGAD development, a co-design effort in the development of high-performance readout ASICs is underway. The first prototype will be submitted in July and the design will be presented in this talk.

The readout ASIC is being developed in the 28 nm CMOS process that has emerged as the technology of choice for the next decade of developments in the field. The first prototype is a miniASIC run with 3 mm2 area incorporating a linear array of 50 μm and 100 μm pixels matched to LGAD cell variants. The pixels incorporate different flavors of low-jitter front-end amplifiers, fast comparators and sub-10ps Time-to-Digital Converter (TDC). Target performance is < 20 ps timing resolution for the whole system while maintaining the power consumption below 1 W/cm2.

The front-end amplifiers are developed in close co-design with sensor TCAD simulations with continuous communication of expected signal size, rise times, and capacitance estimates. The front-end is an open-loop amplifier at the frequencies of interest and uses active feedback to set the DC levels and recovery times. The comparator consists of a single common-source amplifier and the threshold is set by tuning of a common gate stage inside the pre-amplifier. The pre-layout estimate of the jitter contributed by the front end is 7 psrms which is heavily influenced by the signal size, rise time, and parasitic capacitance of the sensors. The TDC is a 2-dimnesional Vernier ring-oscillator architecture with embedded sliding-scale technique, capable of simultaneous measurements of TOA and TOT with resolutions of 6.25ps (8bit) and 50ps (5bit), respectively. The average TDC power consumption depends on hit occupancy and is 18.4μW for 10% and 2.9μW for 1% occupancy. The embedded sliding-scale technique allows for significant improvement of conversion linearity, and will greatly simplify the calibration of the TDCs, especially useful in high-channel count implementations targeted by this project.

The ASIC incorporates front-end charge injection circuitry to allow for test-bench characterization. The ASIC will also be wire-bounded to the dedicated LGAD cells on the sensor wafer for preliminary characterization of the full chain. The aim of the first prototype is to characterize and select best schemes that will be used in the successive MPW ASIC run producing a matrix of pixels to be bump-bounded to the developed LGAD sensors.

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