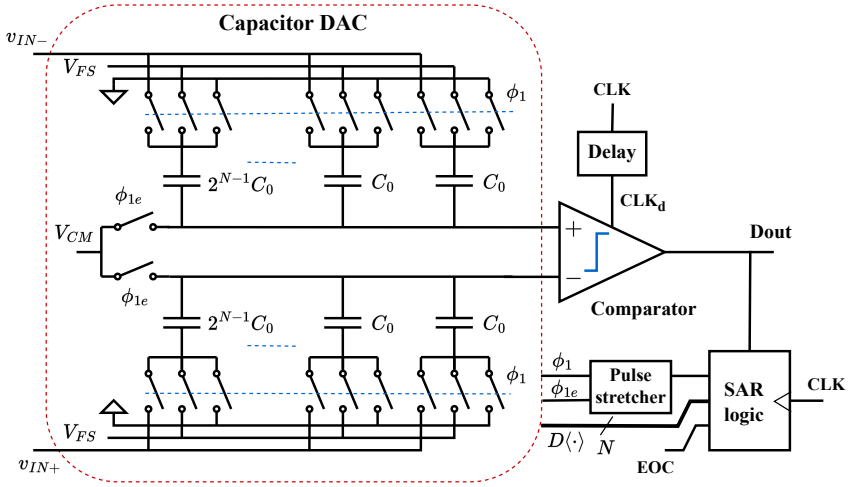

Figure 1: Top-level block diagram of the proposed SAR ADC.

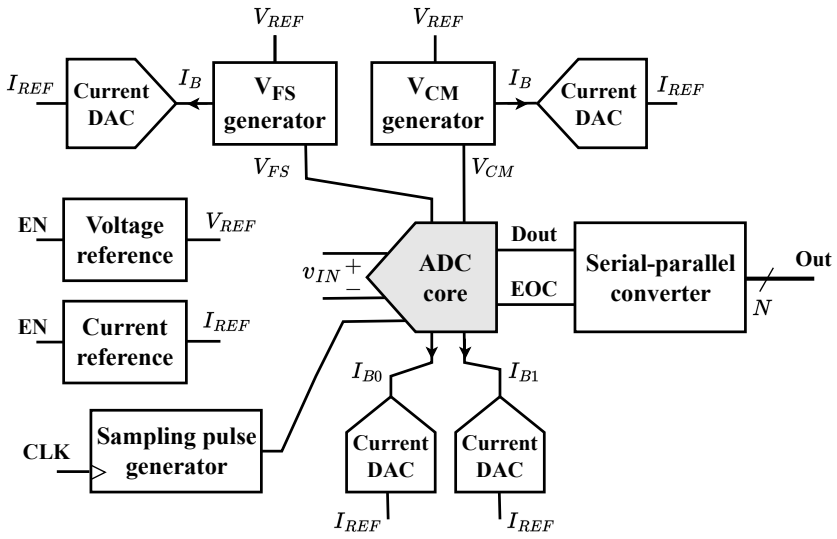

Figure 2: Block diagram of the complete SAR ADC, including the core, output serial-parallel converter, sampling pulse generator, current DACs to set bias currents, voltage and current references, a current distribution network, and V_{FS} and V_{CM} generators. The references are compensated to allow operation over a broad temperature range.

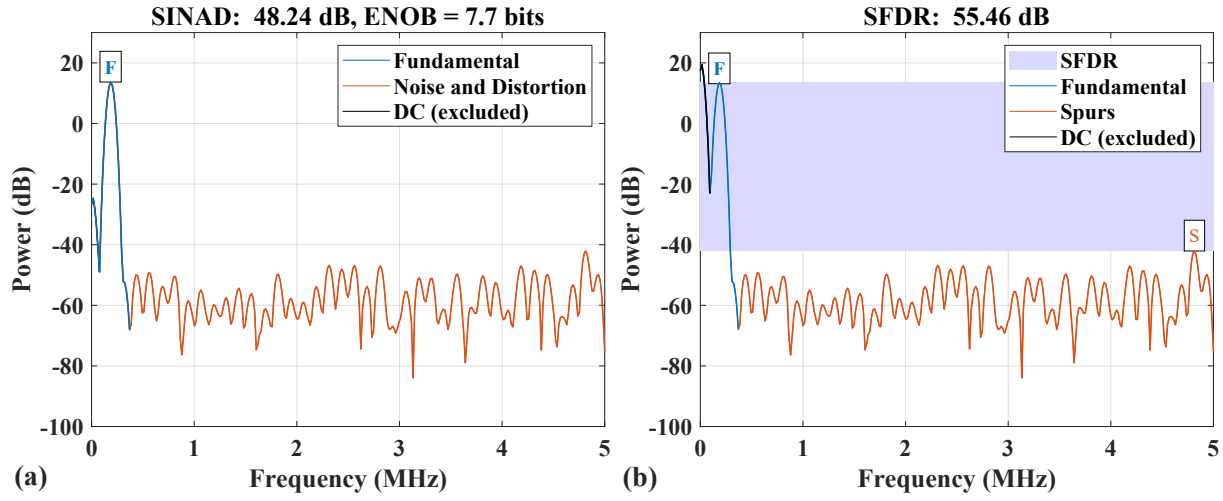

Figure 3: Simulated dynamic performance of the complete ADC at 300K and 10 MS/s for a nearly full-scale sinusoidal input: (a) SINAD and ENOB, and (b) SFDR.