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U.S. DEPARTMENT OF ENERGY

A Wide-Temperature-Range SAR ADC in Open-Source CMOS Technology

Soumyajit Mandal[1], Sanjeevi S. Karri[2], Sanchari Das[3], Bibhu Datta Sahoo[3]

[1]Brookhaven National Laboratory, [2]Prixarc, LLC, [3]University of Buffalo

October 3, 2024

TWEPP 2024, Glasgow

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Outline

- Motivation
- Open-source ASIC ecosystem
- Temperature-robust SAR ADC
- Area-efficient MOSCAP-based SAR ADC
- Efficient on-chip SAR ADC calibration
- Conclusion

Motivation for open-source chip design

- Remove one or both of the main “barriers to entry” for ASIC design:
  - CAD tools
  - Process design kits (PDKs)
- Takes inspiration from the many successful examples of free and open-source software (FOSS).
- Several free and open-source tools and PDKs have been around for a while, but the designs were not manufacturable.
- The first true FOSS ASIC flow (including a manufacturable PDK) was announced by SkyWater and Google in 2020.
  - Based on an open-source version of SkyWater’s 130 nm CMOS PDK (SKY130).
  - Has since been extended to other processes: GF180MCU (CMOS), IHP SG13G2 (BiCMOS)
  - MPW access is organized by eFabless (SKY130 and GF180MCU).

Potential advantages for HEP

- Related to PDKs
  - Simplify collaborations with universities, small companies, and other institutions
  - Allow easy sharing of designs across multiple institutions (including international collaborators)
- Related to CAD tools
  - Reduce (or entirely eliminate) CAD tool licensing costs.
  - Allow users to easily customize tools and flows
- Related to both PDKs and CAD tools
  - Take advantage of students' familiarity with open-source software development to attract new ASIC designers to the field
  - To get started, one can simply clone the Git repository at https://github.com/RTimothyEdwards/open_pdks

Original news stories

- Timeframe: 2021-2022

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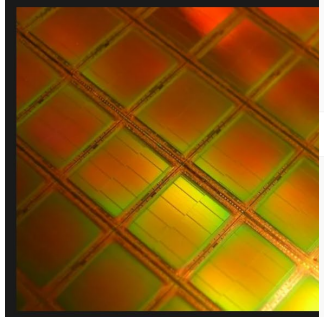
HOME BLOG HACKADAY.IO TINDIE HACKADAY PRIZE SUBMIT ABOUT May 16, 2022

THE OPEN SOURCE ASICS HACK CHAT REDEFINES POSSIBLE

by: Tom Nardi



There was a time when all that was available to the electroni
vacuum tubes. Then along comes the integrated circuit, and
affordable programmable microcontrollers arrived on the sc
easier, and the line between hardware and software started
community was introduced to field programmable gate array
them. While not as widely applicable as the IC or MCU, the p
once again opened doors that were previously locked tight.

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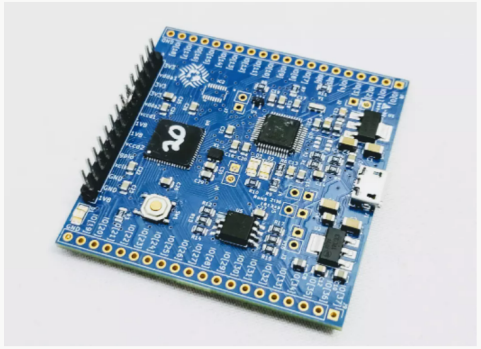
FEBRUARY 8, 2022 BY JEAN-LUC AUFRANC (CNXSOFT) - 4 COMMENTS

CLEAR is an open-source FPGA ASIC provided by Efabless' chipIgnite

Open-source SoC designs are available to run on FPGA hardware, but few make it to silicon due to the costs involved. That's why a couple of years ago the Google SkyWater PDK (process design kit) was released together with an offer to manufacture up to 100 pieces for free to selected designs in collaboration with Efabless.

Efabless chipIgnite is an evolution of that offer with $9,750 being enough funds to manufacture 100 QFN or 300 WCSP parts, or alternatively 1,000 parts for $20 each ($20,000). Based on the company's Caravel template SoC and the openFPGA generator framework, **CLEAR** open-source FPGA ASIC design is meant to promote and demonstrate the chipIgnite "paid IC creation" solution. You can participate by joining a group buying campaign on GroupGets to get a development board based on CLEAR for $74.99 plus shipping.



CLEAR open-source FPGA ASIC features:

- FPGA – Small 8×8 (64) CLB eFPGA
- CPU – VexRISCV-based CPU
- Memory – 3 kilobytes of on-chip RAM (2 kB of OpenRAM and 1 kB of DFFRAM)
- Storage – external QSPI flash
- Peripherals – SPI master, UART, 39x software configurable GPIO, Counter/Timers, Logic Analyzer
- Misc – Programmable internal clock frequency

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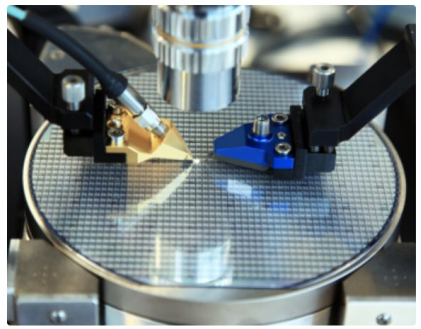
Google, SkyWater Partner on Open ASIC Designs

November 12, 2020 by George Leopold



via Shutterstock

and manufactured to serve one purpose and cannot be reprogrammed fo

SkyWater, the pure play semiconductor foundry based in Bloomington, M
process design kit would be selected and manufactured using its 130-nm

A portal launched by San Jose-based Efabless includes a workflow that a

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YOUR OWN OPEN SOURCE ASIC: SKYWATER-PDK PLANS FIRST 130 NM WAFER IN 2020

by: Al Williams 51 Comments June 30, 2020

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If you want to make your own chip and aren't Microsoft rich, who do you turn to?

$10,000 and Efabless may be what you're looking for

Agam Shah Thu 17 Mar 2022 // 01:05 UTC

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INTERVIEW The likes of Google, Facebook, and Microsoft can design custom chips and have them manufactured using their billions of dollars in the bank.

Smaller outfits wishing to make their own processors or microcontrollers, say, aren't as fortunate as they lack the funds and resources. Getting even a small volume of physical chips in the hands of engineers and developers to experiment with is a big challenge. FPGAs are an option, though they have their limits, and you might just want the experience or benefits of taping out your own ASIC.

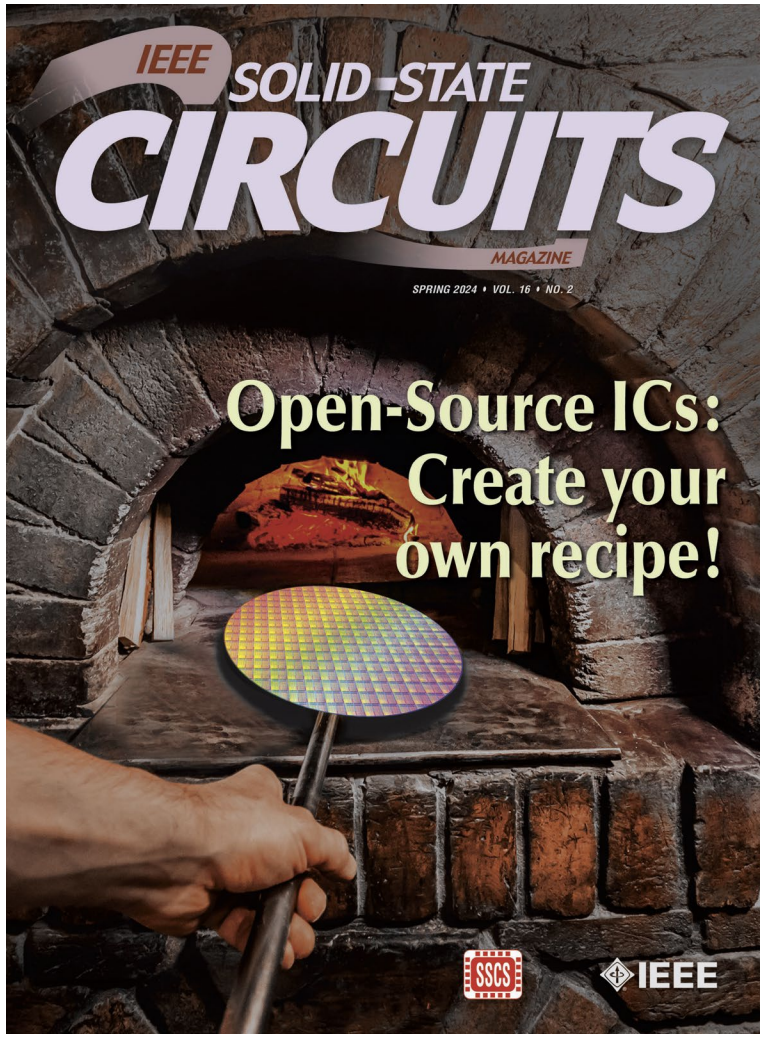
Now a biz called Efabless hopes to close the capability gap by helping people get their semiconductor blueprints into a factory for manufacturing at low cost. Getting access to a fab has become especially challenging with demand for chips outstripping assembly line output globally.

> **Our goal is to put design in the hands of not only chip designers who just didn't have the resources, but to make it so simple that anybody could create a chip**

"Our goal is to put design in the hands of not only chip designers who just didn't have the resources, but to make it so simple that anybody could create a chip," Michael Wishart, CEO of Efabless, told *The Register* this week.

The company is connecting resource-constrained chip startups and universities on tight budgets to manufacturers, which then supply small volumes of completed components. The proliferation of open architectures like RISC-V, and wider availability and improvement of chip design tools, known as EDA software, have arguably contributed to a boom in custom chip designs, mostly by lowering the barrier to entry.

A more recent summary



- Provides a good overview of the open-source ASIC ecosystem
- Note: The articles themselves are *not* open access…

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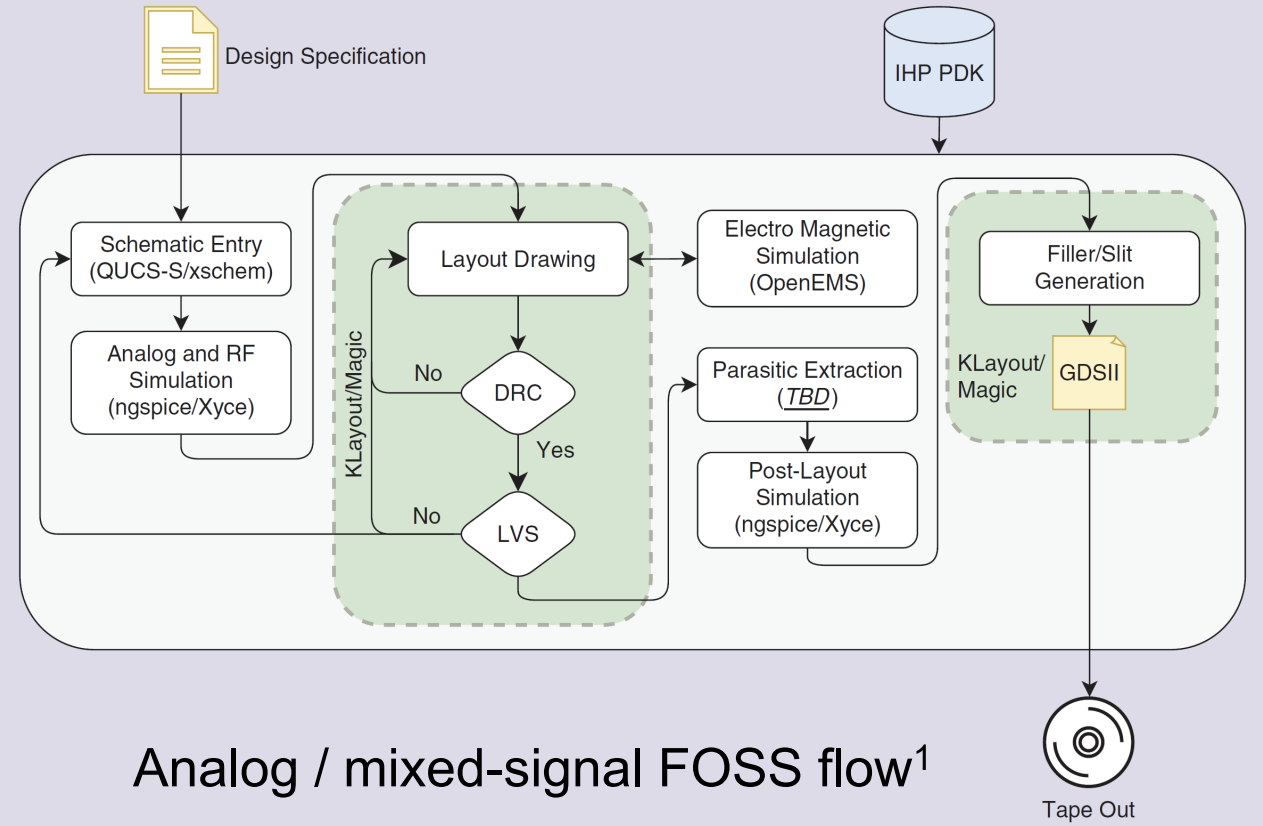
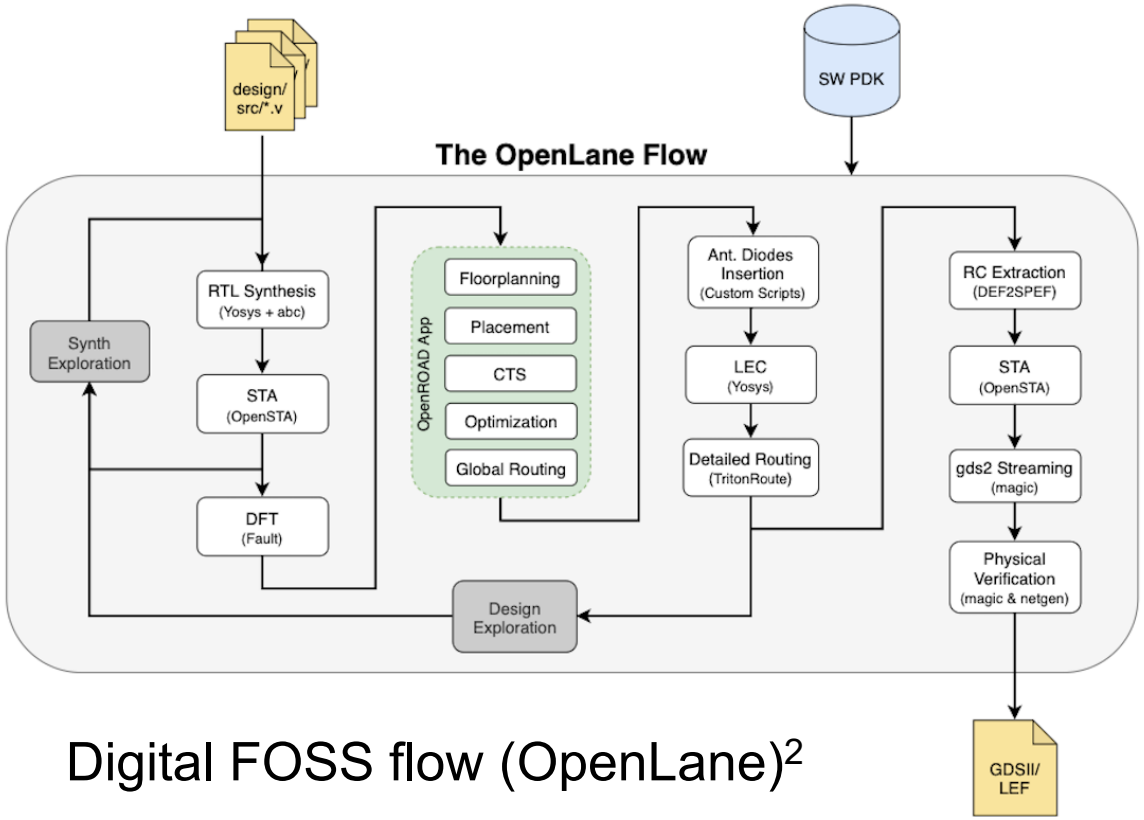
IEEE SSCS Magazine, Spring 2024

Available tool flows



Analog / mixed-signal FOSS flow[1]



Digital FOSS flow (OpenLane)[2]

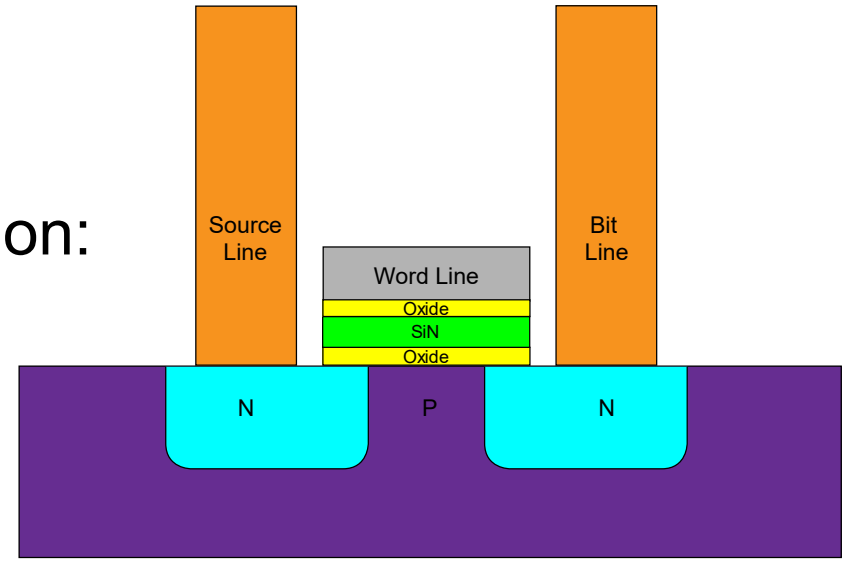
- Alternative: Free Cadence PDK for SKY130 (launched in early 2024)
  - Can be downloaded from the Cadence support website, supports both analog and digital flows

[1]K. Herman *et al.*, "On the Versatility of the IHP BiCMOS Open Source and Manufacturable PDK: A step towards the future where anybody can design and build a chip," in *IEEE Solid-State Circuits Magazine*, vol. 16, no. 2, pp. 30-38, Spring 2024

[2]www.zerotoasiccourse.com/terminology/openlane

The SkyWater 130nm process

- SKY130 is a mature 180nm-130nm hybrid technology developed by Cypress Semiconductor that has been used for many production parts.
- The open-source version is a silicon–oxide–nitride–oxide–silicon (SONOS) technology (130nm node) with 1.8V nominal V_{DD} and 2.5V/5V I/O.
  - 5 metal layers, plus a high-resistivity (~2 Ω/□) “local interconnect” layer below M1
  - Inductor-capable (no standard cells in PDK, but can be custom-designed)
  - Poly resistors, MIM capacitors
  - Non-volatile memory (NVM) cells using SONOS
  - HV transistor options
- More details available in the PDK documentation:
  - https://skywater-pdk.readthedocs.io/en/main/
  - Documentation is incomplete…



SONOS memory cell

MPW fabrication options

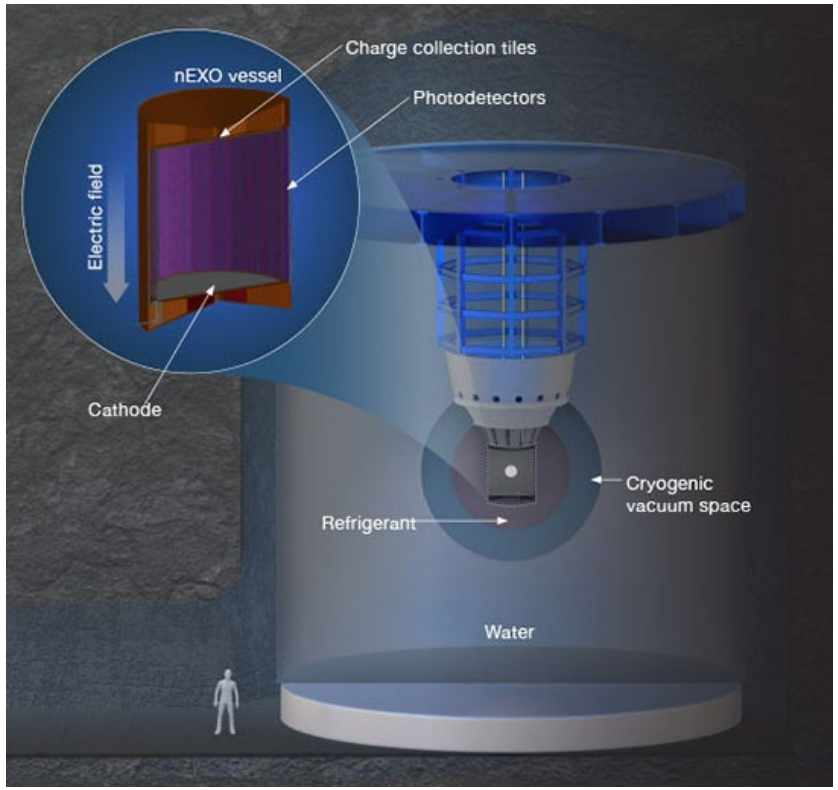
- All options are offered by eFabless using the SKY130 process
- Designs do not have to be open-source
- About 50% of runs (~2 per year) use the SKY130B variant which includes on-chip ReRAM
- Typical turnaround time is 6 months

	Layout area	Cost	Available I/O	Runs
chipIgnite	10 mm^2, plus housekeeping SoC	$9,750 for 100 packaged chips or bare dies	38 GPIO, analog or digital	Every 3 months
chipIgnite Mini	1.3 mm x 1.6 mm, plus housekeeping SoC	$3,500 for 25 packaged chips	36 GPIO, digital only, multiplexed between designs	Every 3 months
Tiny Tapeout*	160 µm x 100 µm	$300 for first tile, $50 for additional tiles	38, analog or digital, multiplexed between designs	Every 3 months

*Details at https://tinytapeout.com/

Why an open-source SAR ADC?

- Rare-event search experiments, such as DUNE and nEXO, require cryogenic AFEs connected via lossy channels (e.g., radio-pure power/data cables within the noble liquid TPC).
- The availability of moderate resolution (~12 bit) cryogenic ADCs allows AFE outputs to be digitized locally, eliminating SNR loss during transmission
  - Examples include the DUNE ColdADC, which is designed to work inside liquid Argon (85K)[1]
- Additionally, low resolution (8-10 bit) cryogenic ADCs are needed for auxiliary tasks such as supply voltage monitoring
  - Availability as easy-to-use blocks would allow such “utility” ADCs to be easily integrated into larger ASICs
  - Temperature-robust designs are required to enable widespread use and minimize dependence on die temperature variations
- Implementation in open-source processes such as SKY130 would further simplify use and adoption
  - Could be easily integrated within SKY130 prototypes of Q-Pix[2]



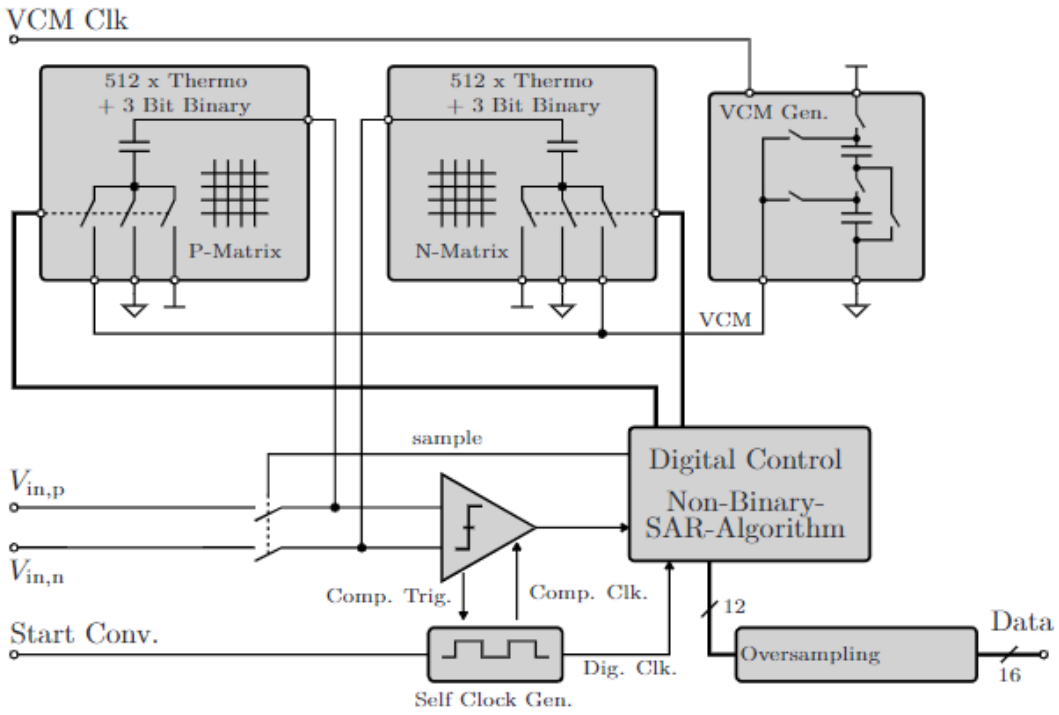
Overview of the nEXO TPC for measuring the energy and location of double beta decays (within liquid Xenon at 165K)

[1]Grace, C. R., et al. "ColdADC: A 16-Channel Digitizer ASIC with 186 μV-rms noise and 10.5-bit ENOB at 77 K for the Deep Underground Neutrino Experiment." *2020 IEEE NSS/MIC*, 2020.

[2] Asaadi, Jonathan, Daniel A. Dwyer, and Brooke Russell. "Novel Liquid Argon Time-Projection Chamber Readouts." *Annual Review of Nuclear and Particle Science* 74 (2024).

Prior work on open-source SAR ADCs

- Designed in SKY130 by Harald Pretl's group at JKU (Linz, Austria)
- Non-binary weights for redundancy (error correction), asynchronous, 12-bit, up to 1.2 MS/s
- Custom MOM unit capacitors, C_u = 0.447 fF
- Built-in FIR low-pass filters for increased resolution via oversampling and averaging
- Integrated switched capacitor V_{CM} generator
- Layout area = 442 µm x 402 µm
- Fully open source, available on Github: https://github.com/iic-jku/SKY130_SAR-ADC1



Moser, Manuel. "Design of a Low-Power 12-bit Non-Binary Charge-Redistribution SAR-ADC utilizing the SKY130 Open-Source Technology." MSc Thesis, Johannes Kepler University, Linz (2023).

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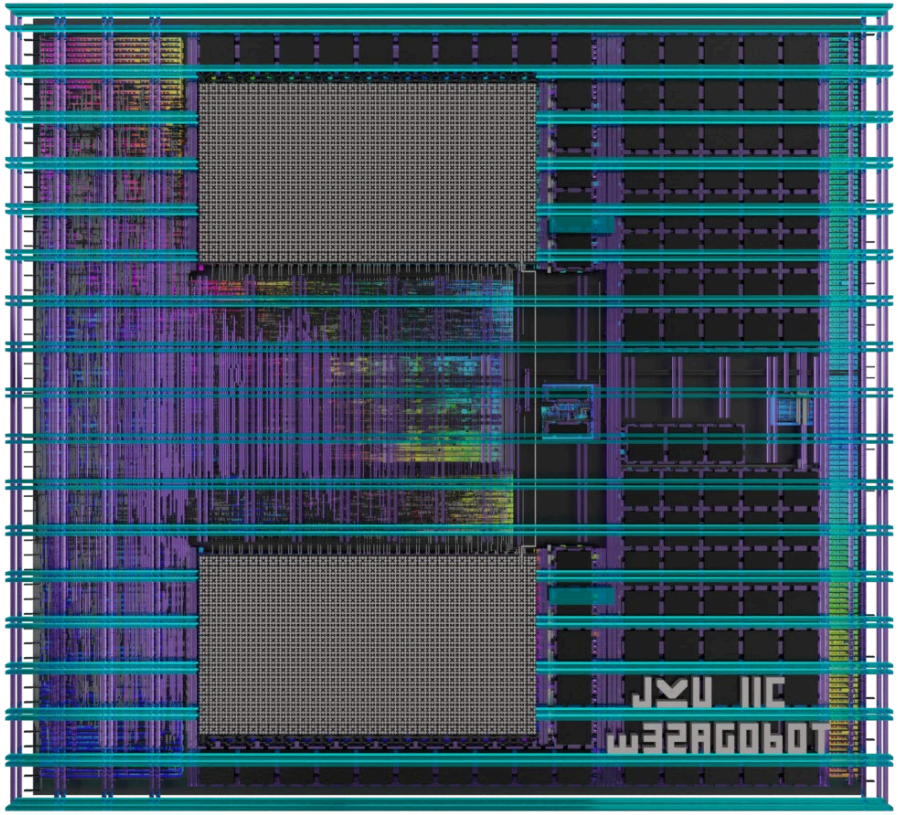

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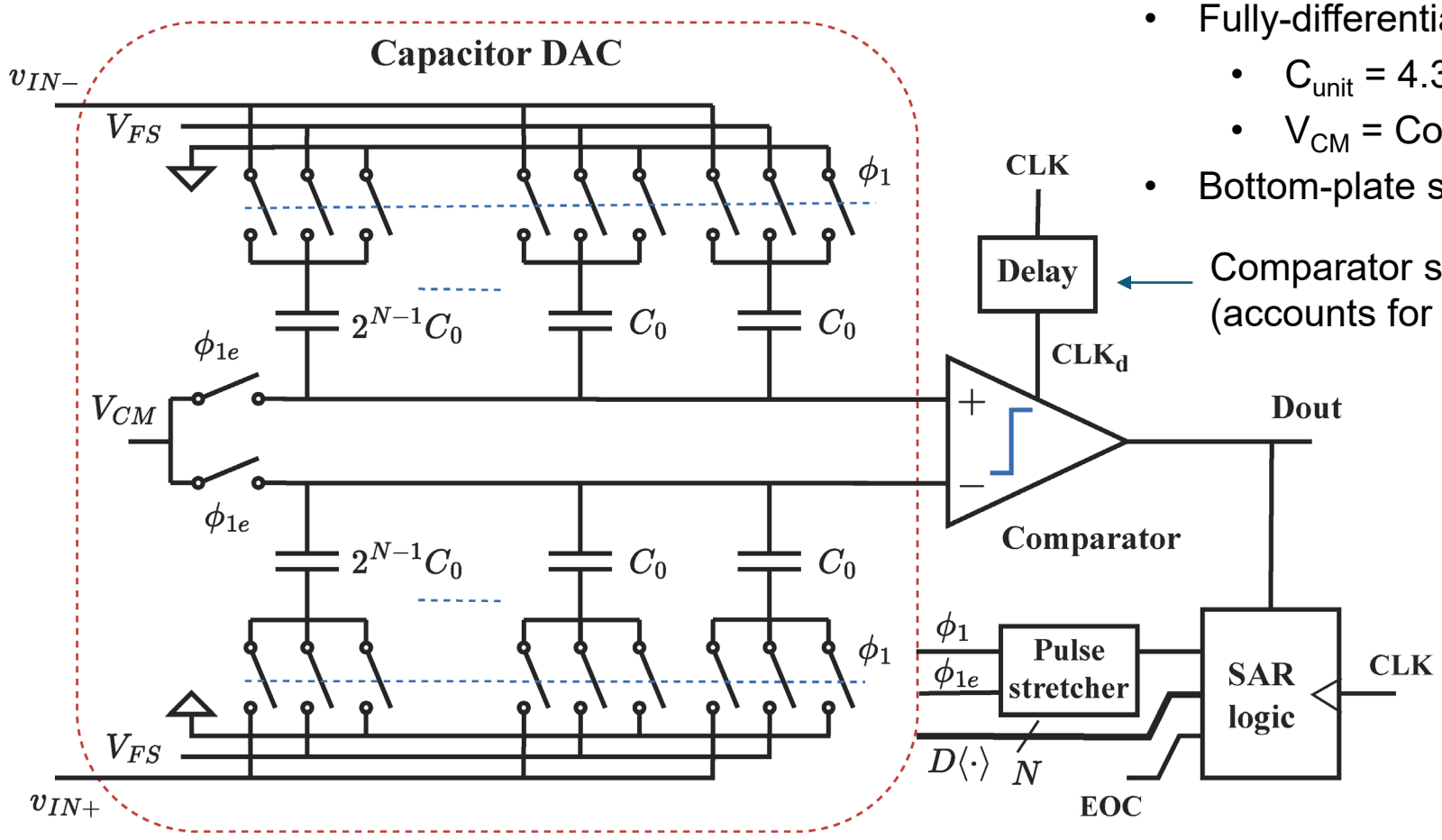
Proposed SAR ADC core

- Combines the capacitor DAC, comparator, and SAR logic
- Serial data output clocked at $f_{clk} = 12f_s$, plus an "end of conversion" (EOC) signal at f_s



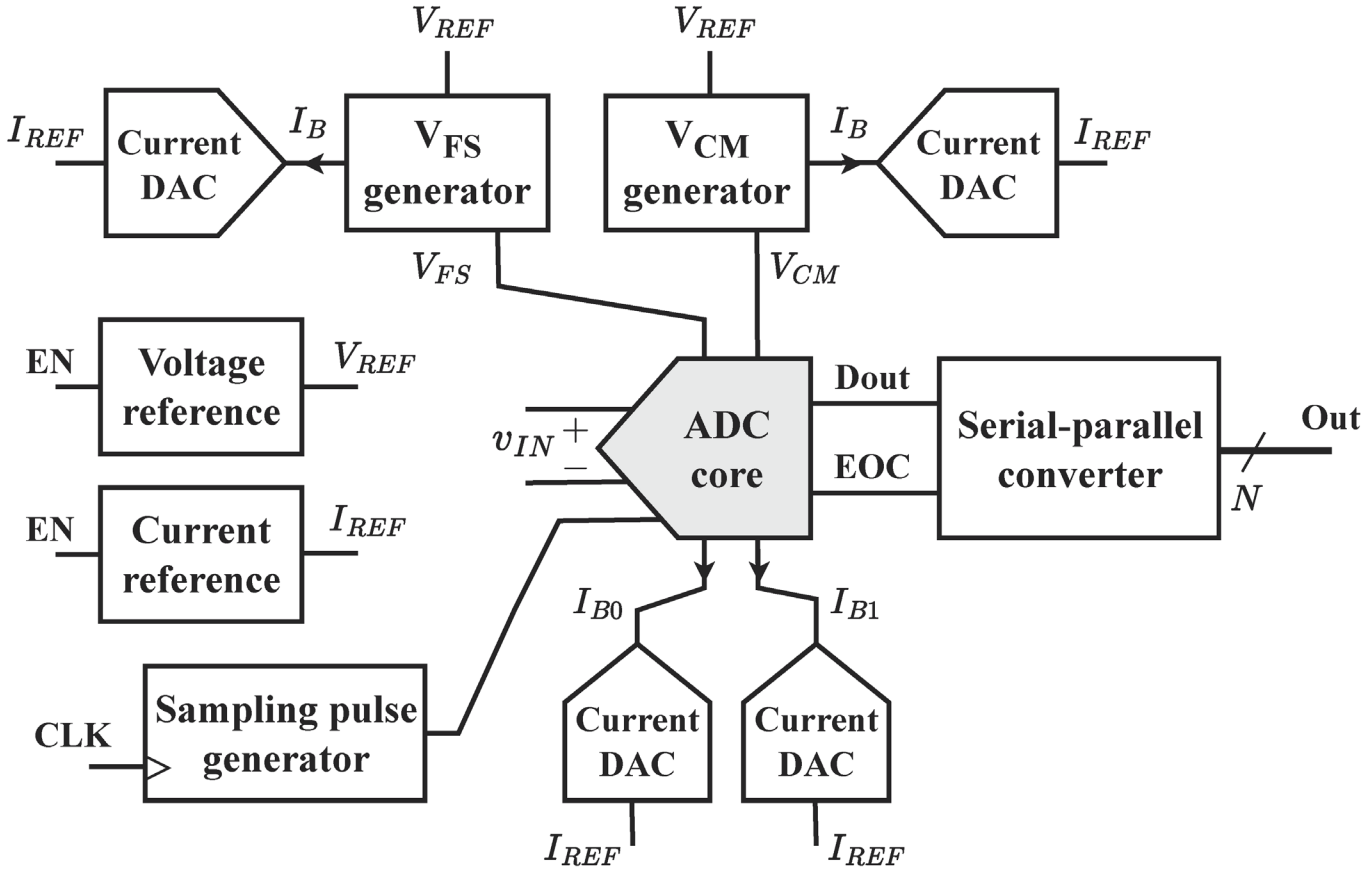
- Fully-differential binary weighted 8-bit capacitor DAC
  - C_{unit} = 4.37 fF (smallest supported by PDK)
  - V_{CM} = Common-mode voltage ≈ $V_{REF}/2$
- Bottom-plate sampling to improve linearity

Comparator sampling delay
(accounts for DAC settling time)

- Two-stage dynamic comparator
  - Inverter-based preamplifier to reduce input-referred offset and kickback into the DAC.
  - StrongARM latch to generate logic-level outputs.
- Synchronous SAR logic

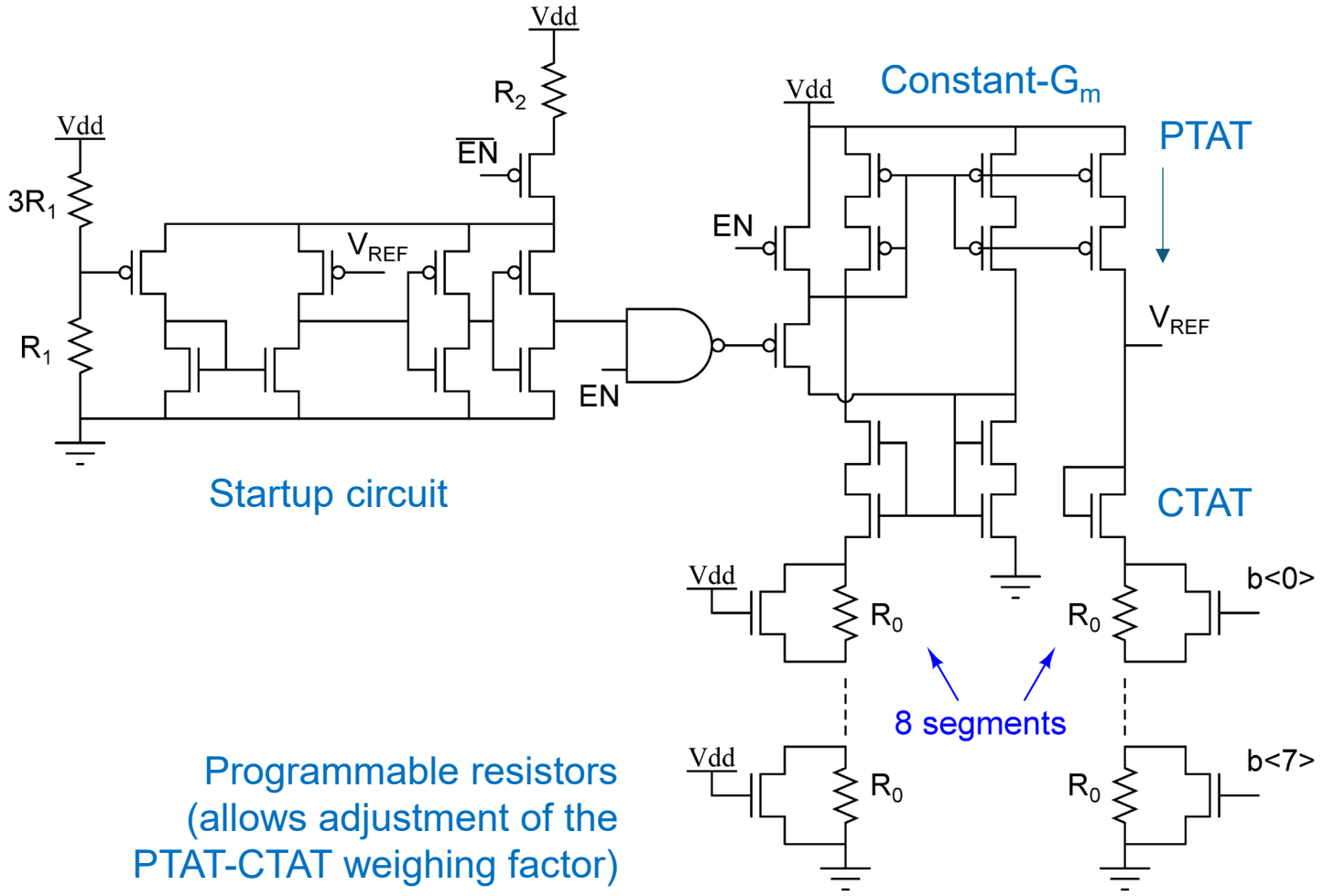
Complete SAR ADC block

- Self-contained design including
  - Built-in voltage and current references
  - A sampling pulse generator
  - A digital interface for setting parameters
- The voltage and current references are temperature-compensated to allow operation over a broad temperature range



Temperature-compensated reference

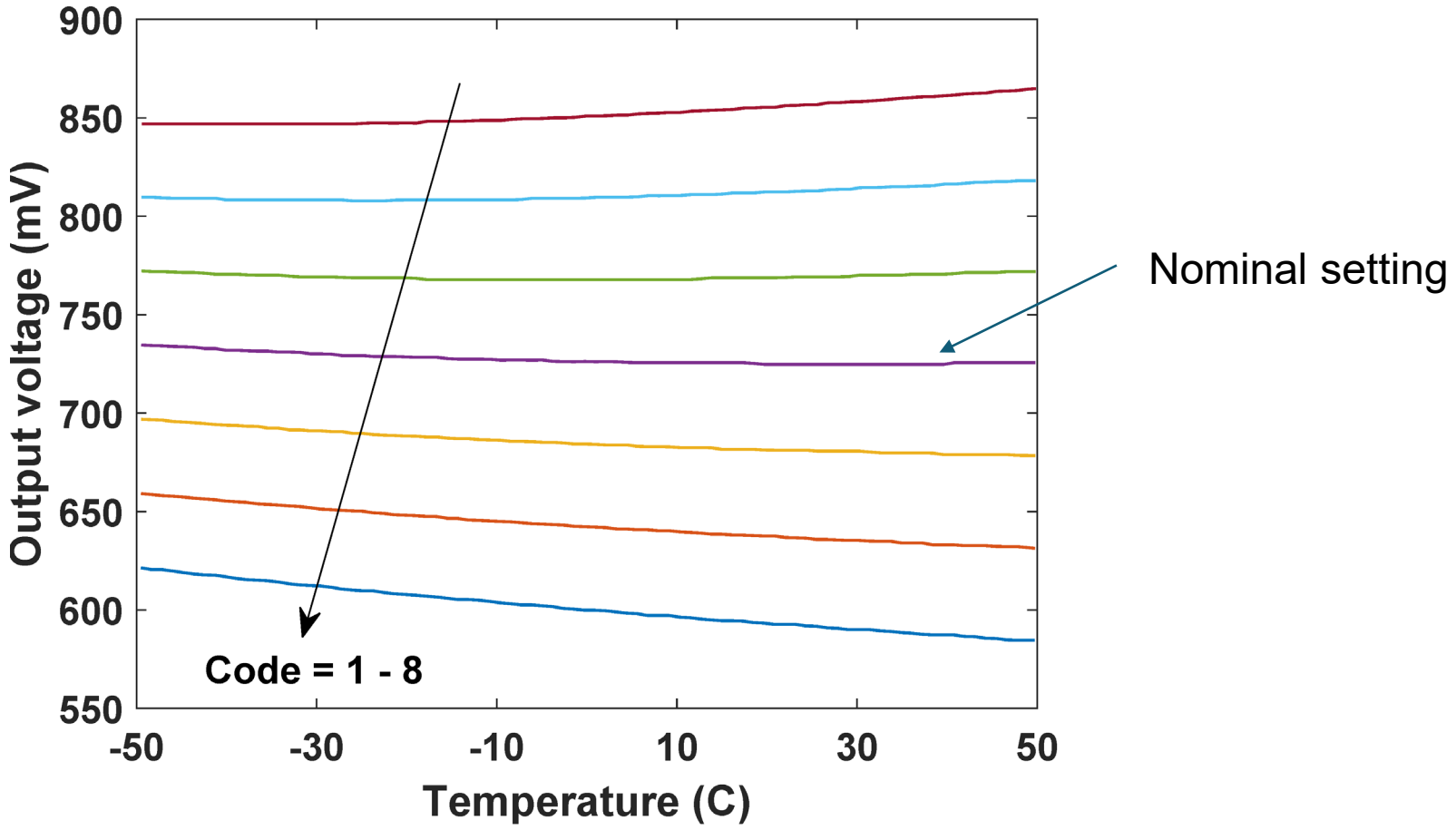
- Traditional substrate PNP-based bandgap references are not desirable for cryogenic operation due to performance degradation of the BJTs
- Replaced by a similar MOS-based voltage reference topology
  - Weighted sum of PTAT voltage (from a constant-Gm circuit) and CTAT voltage (from V_{GS} of a MOSFET) provides temperature compensation
  - Current mirrors are self-cascaded (with regular and low-V_T devices) to improve supply regulation
  - Constant-G_m operated in subthreshold to minimize power consumption
  - Includes an active startup circuit to ensure reliable operation over a broad temperature range



Temperature-compensated reference (2)

- Range of simulated temperatures limited by available device models
- PTAT-CTAT weighing factor can be digitally programmed to obtain optimum compensation over the desired operating temperature range

V_{DD} = 1.8 V



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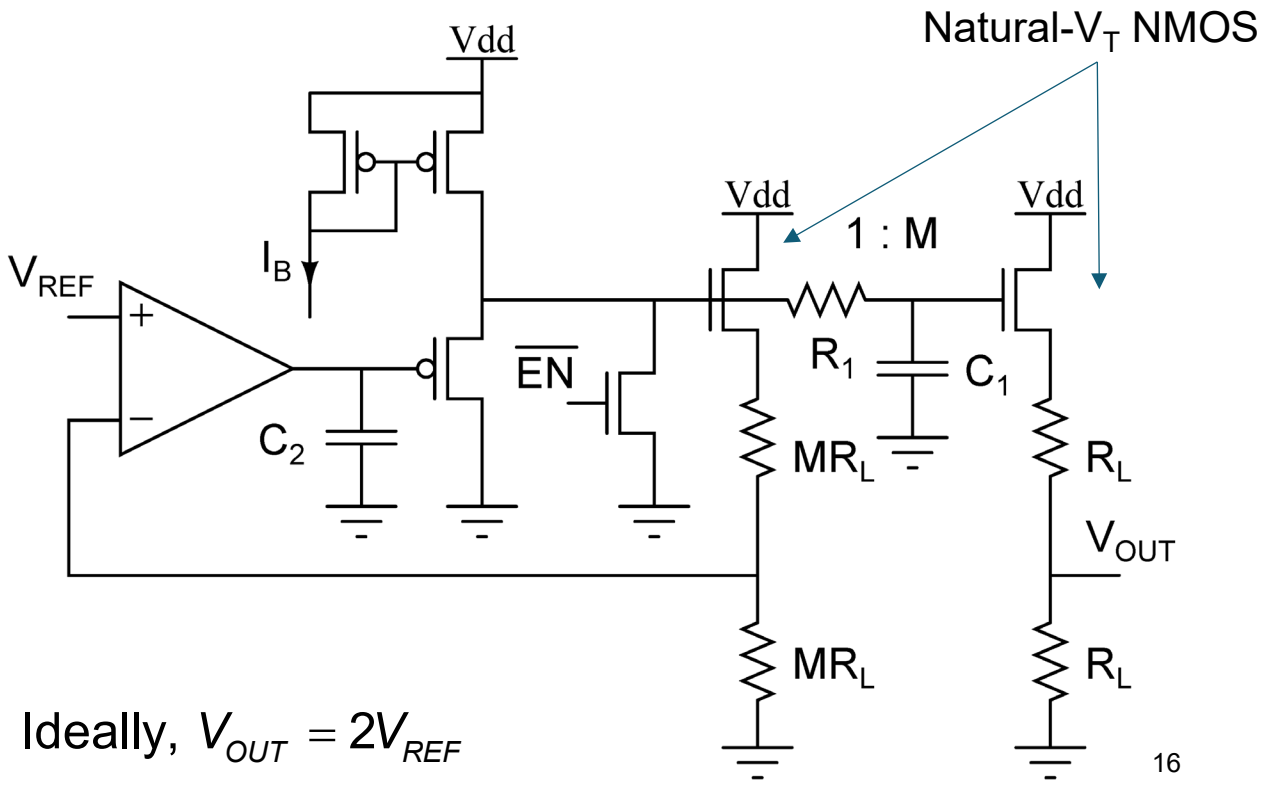
Reference voltage generator

- Sets the full-scale voltage of the ADC from a temperature-compensated input, V_{REF}
- Design uses a replica source follower to ensure low output impedance and stability in the presence of kickback from the DAC
- Source followers use natural-V_T (normally-on) NMOS to reduce V_{GS}, thus allowing output voltages close to V_{DD} even in the presence of body effect (due to lack of a triple-well option)
- Includes shutdown function to save power
- Trade-off between output impedance (R_L || $1/g_m$) and power consumption
  - Nominal V_{REF} = 0.725 V
  - Output resistance, R_L = 2.2 kΩ
  - Current consumption ≈ 750 µA (dominated by output stage)
- Similar design used for V_{CM}, but with minor differences:
  - Feedback divider ratio = 1 to get $V_{OUT} = V_{REF}$
  - Output voltage is 2x lower, so no source follower required for level shifting



Ideally, $V_{OUT} = 2V_{REF}$

Current reference

- Uses the weighted sum of two constant-G_m current references to create a temperature-compensated reference current for the comparator and reference voltage generators.
- The two constant-G_m references use resistors with different temperature coefficients, leading to PTAT-like behavior but with different slopes, α.

$$I_1 = I_{01}\left(1+\alpha_1\Delta T\right), \quad I_2 = I_{02}\left(1+\alpha_2\Delta T\right)$$

$$I_{out} = I_1 + c_2 I_2 = \left(I_{o1} + c_2 I_{o2}\right) + \left(I_{o1}\alpha_1 + c_2 I_{o2}\alpha_2\right)\Delta T$$

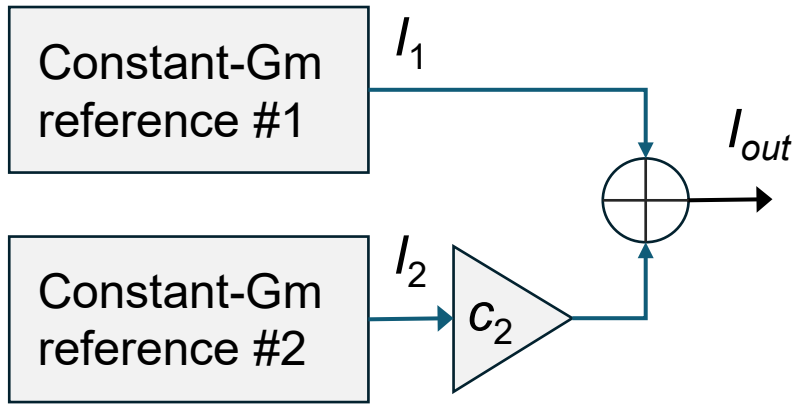
Temperature-independent if

$$I_{o1}\alpha_1 + c_2 I_{o2}\alpha_2 = 0 \Rightarrow \boxed{c_2 = -\left(\frac{I_{o1}\alpha_1}{I_{o2}\alpha_2}\right)}$$

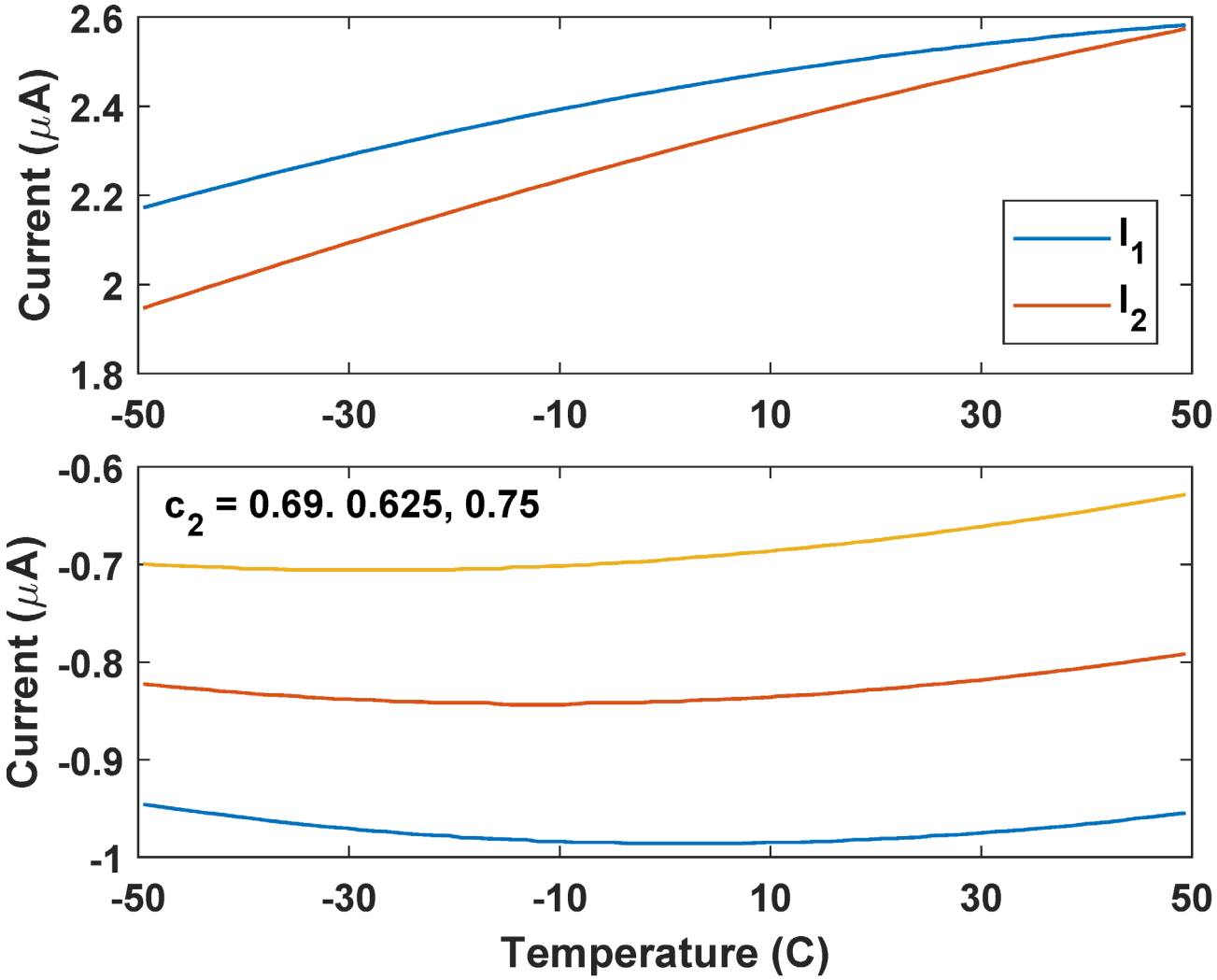
$$\Rightarrow \boxed{I_{out} = I_{o1}\left(1-\frac{\alpha_1}{\alpha_2}\right)}$$

Temperature-compensated output

- In our case, the two references use polysilicon and p-type diffusion resistors, respectively.



Current reference (2)



- Value of c_2 can be programmed (using switches) to obtain optimum compensation over the operating temperature range
  - Currently set to 0.69
  - Nominal output current ≈ 0.85 μA

Individual currents

Compensated current

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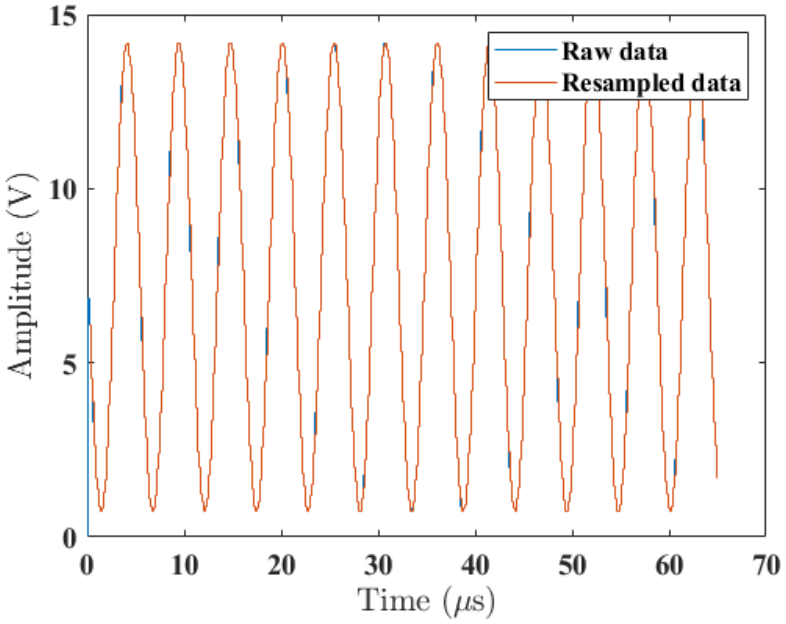
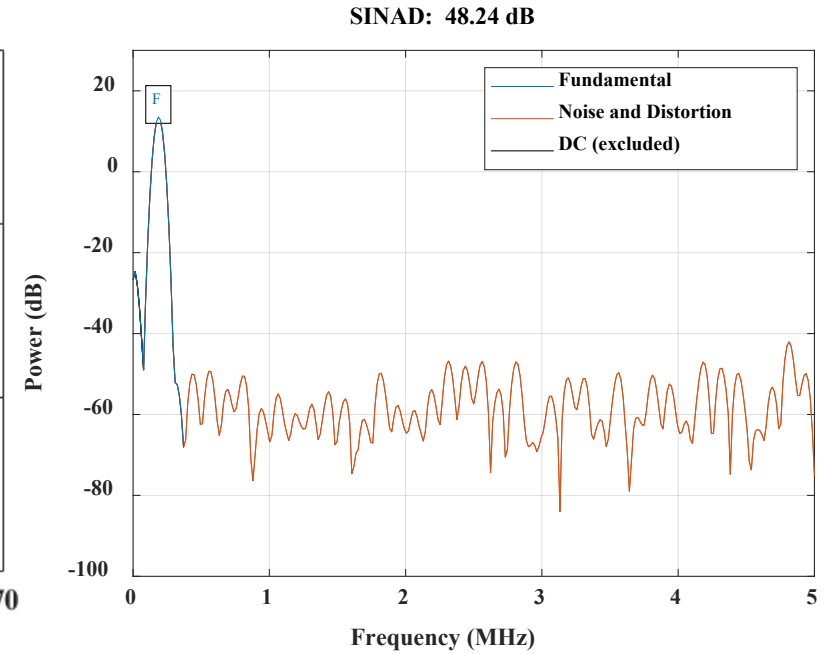
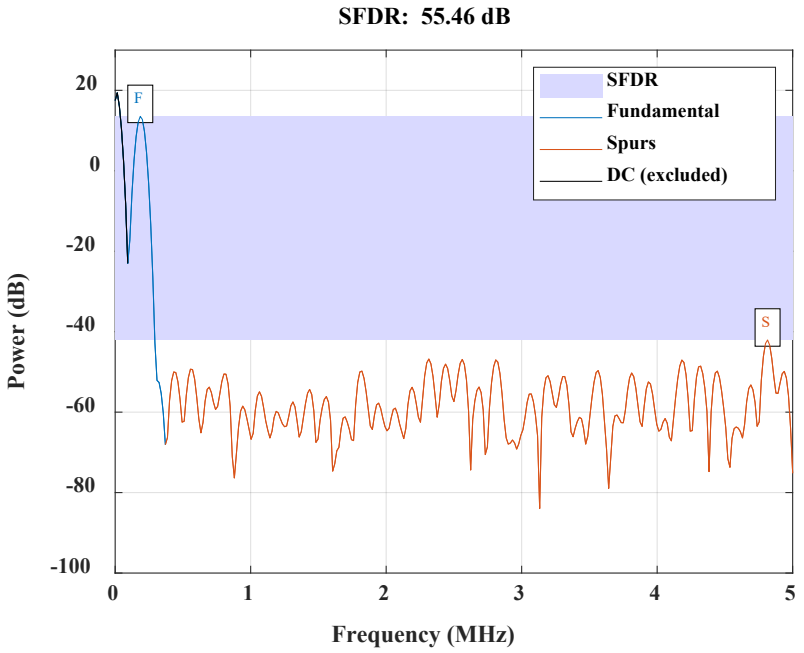
Full ADC simulation results at 10 MS/s

- Full-scale voltage, V_{FS} = 1.45 V, common-mode voltage, V_{CM} = 0.725 V
- Sine wave input at (3/160) x f_s = 187.5 kHz, nearly full-scale (1.3 V_{pp})
- Power supply voltage, V_{DD} = 1.8 V
- SNDR and SFDR computed using MATLAB







SNDR = 48.24 dB
ENOB = 7.7 bits

SFDR = 55.46 dB

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Performance summary

- ADC performance is nearly ideal up to 10 MS/s: sampling rate can be further increased (probably until at least 20 MS/s)
- Power consumption is currently dominated by the static power of the V_{REF} and V_{CM} generators
- Many possible optimizations to reduce power consumption:
  - ADC performance is not mismatch limited, so the unit capacitor sizes can be reduced by designing custom MOM unit capacitors
  - SAR logic can be made asynchronous to reduce conversion time by ~2x
  - A variety of improved DAC switching schemes can be used to greatly reduce switching power
  - Power consumption of V_{REF} and V_{CM} generators can be reduced at the cost of increased settling errors
  - Digital redundancy can be added to further reduce DAC and voltage reference settling errors

Sampling rate	Average current (V_{DD} = 1.8 V)
2 MS/s	1.55 mA
5 MS/s	1.67 mA
10 MS/s	1.80 mA

Includes static power (dominated by V_{REF} and V_{CM} generators) of ~1.52 mA

Allow trade-off to be adjusted by using MOS switches to make the value of R_L programmable

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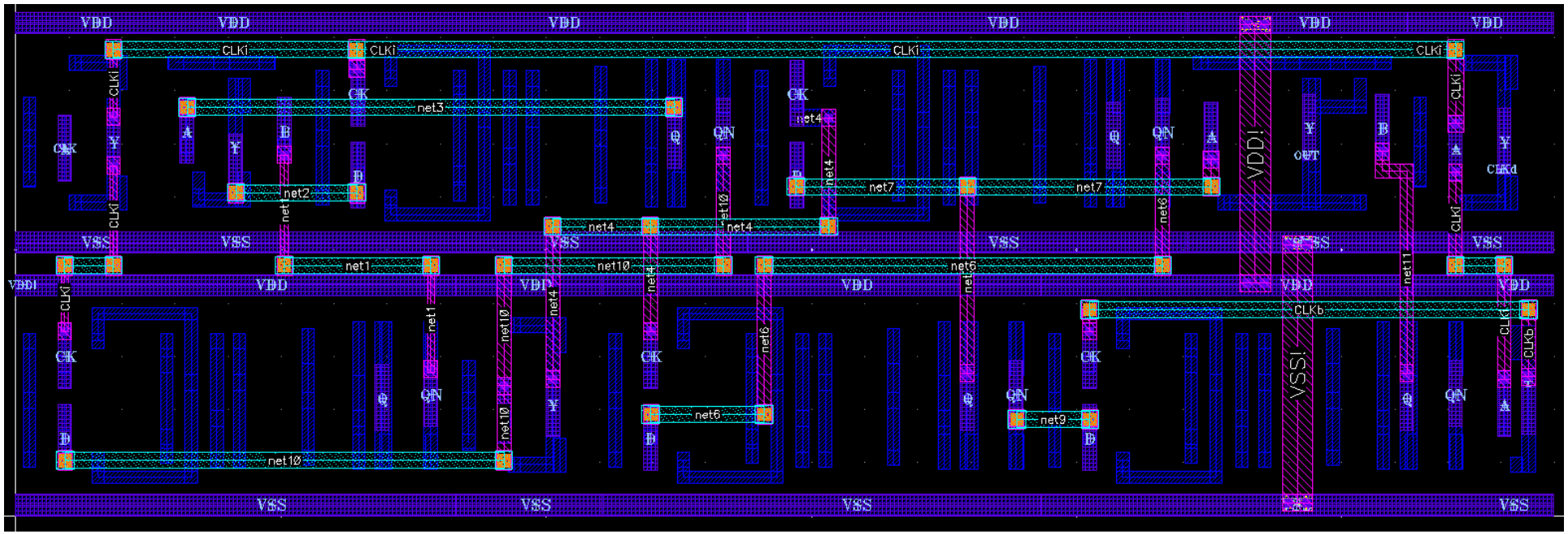
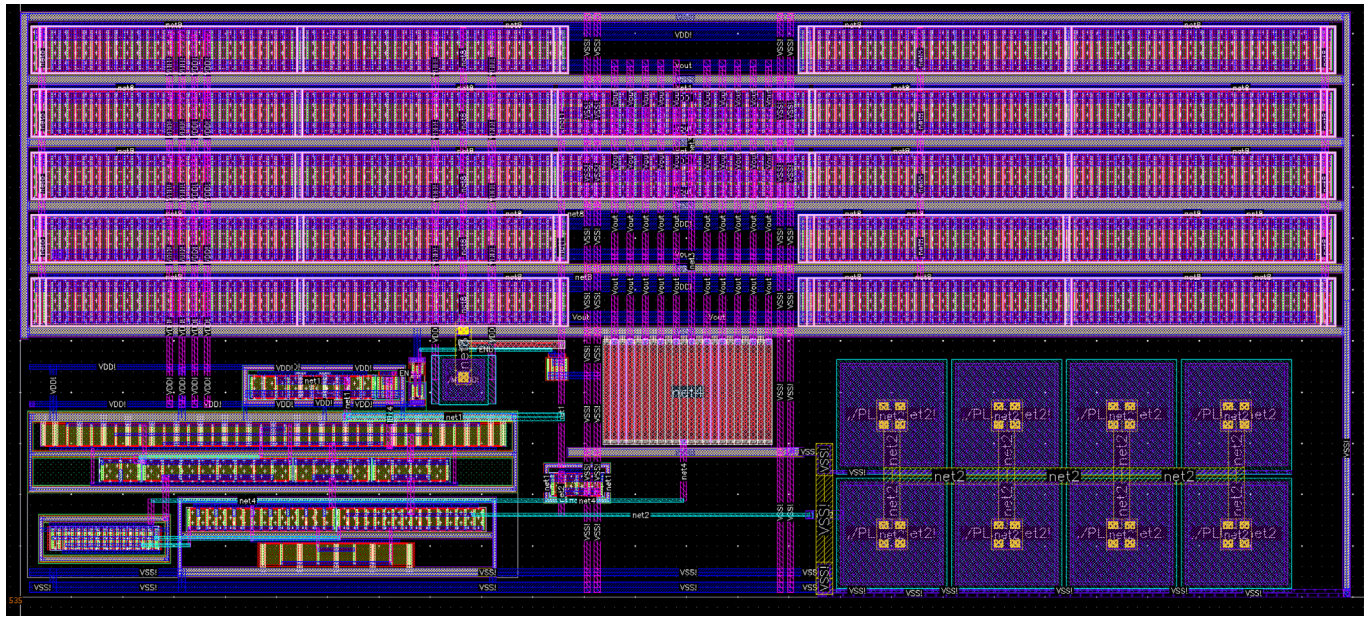
ADC layout

- Layout of the SAR ADC design is underway
  - Tapeout planned in November 2024
- DRC and LVS rule decks (for Pegasus or PVS) are available in the Cadence SKY130 PDK.
  - PEX rule files are not yet included

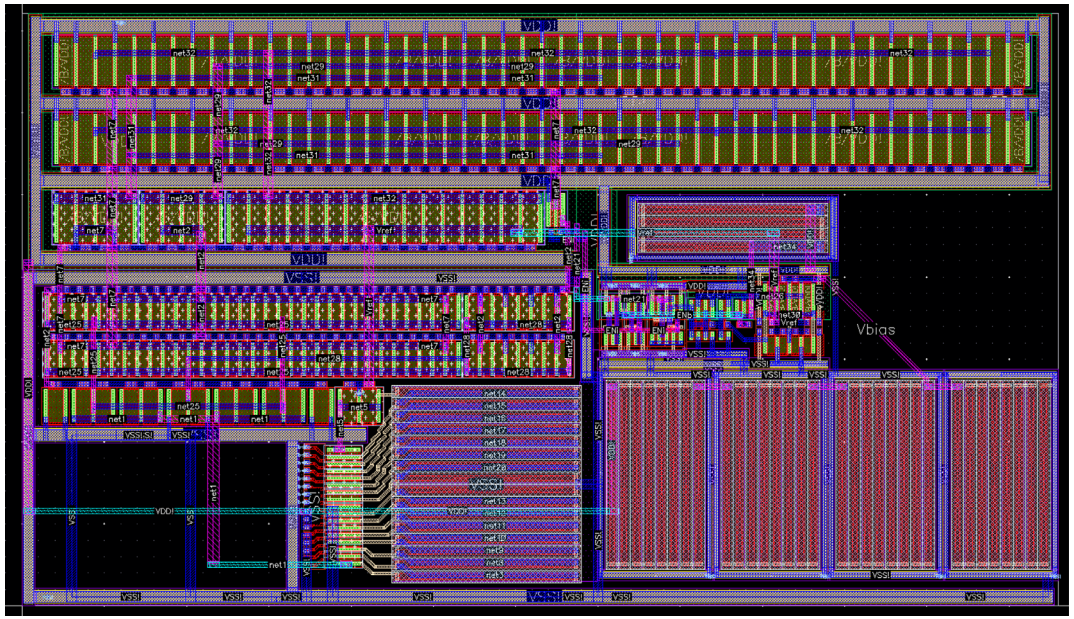


Layout of the sampling clock generator block

Layout of key blocks



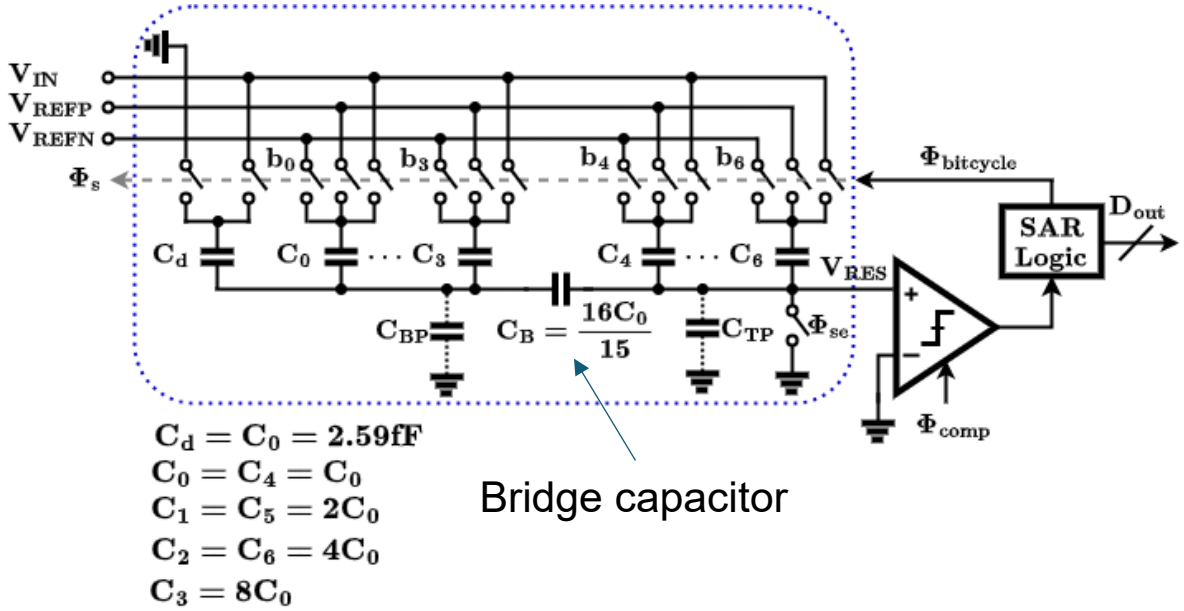
ADC reference voltage generator
Size = 130 µm x 56 µm



CMOS “bandgap” voltage reference
Size = 62 µm x 36 µm

Efficient ADC layout using MOSCAPs

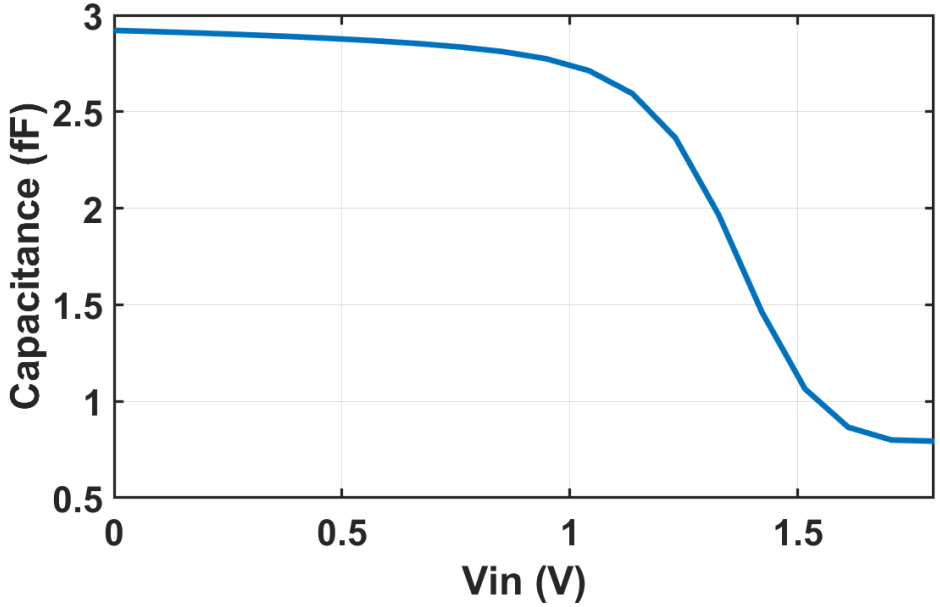
- Idea: Can the capacitor DAC be implemented using MOS capacitors?
  - MOS capacitor arrays can be densely packed while using only the two lowest metal layers, leading to an efficient ADC layout compared to conventional MOM or MIM capacitors
  - The entire ADC can be laid out below a metal shield, allowing the area to be reused for metal-metal capacitors (MOM or MIM) and/or routing on the higher layers
- But MOS capacitors are nonlinear!
  - Yes, but the distortion generated by capacitive nonlinearity is acceptable when it is smaller than that due to other nonlinear error sources (capacitor mismatch and quantization noise)
  - Thus, such arrays may be acceptable for moderate-resolution converters

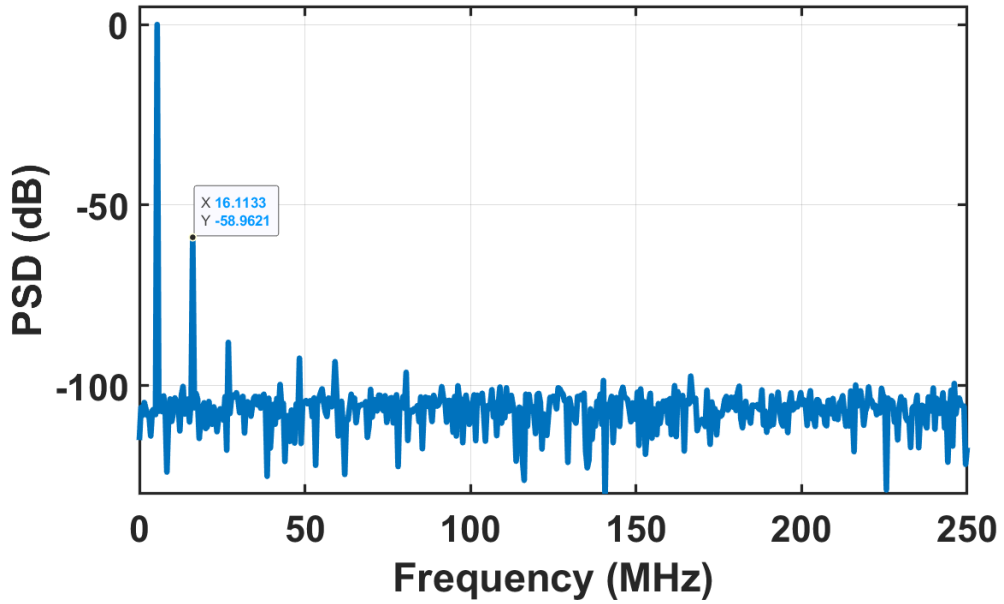


- The DAC can be implemented as a split-capacitor array to further reduce layout area
  - Caveat: A MOS "bridge" capacitor must be in its own well due to its body connection, which increases area due to well spacing rules and degrades linearity due to bottom plate parasitic
  - The bridge capacitor is thus best implemented using a metal-metal structure

Efficient ADC layout using MOSCAPs (2)

- Simulations of minimum-sized MOS capacitor array in SKY130
- The capacitance is most stable at low input voltages
  - Varies by ~1.2% from 0-0.5 V, resulting in SFDR = -58 dB due to third harmonic created during the sampling phase
  - Expected ENOB = 7.5 bits with V_{FS} = 0.5 V at 500 MS/s
  - Input-referred full-scale voltage can be increased by using an input attenuator
  - Gate leakage error should become noticeable at low sampling rates, but is very small in 130 nm
- Practical issue: matching properties of MOSCAPs are not reported in the literature
  - Mismatch likely follows a Pelgrom-like relationship ($\sigma_{\Delta C/C} = K_C/(WL)^{1/2}$), but the matching constant, K_C, is unknown
  - Tapeout will include MOSCAPs of different sizes to allow the matching properties to be experimentally studied





Conclusions and future work

- Open-source PDKs are promising for “utility” blocks such as moderate-resolution ADCs
- These designs could be either used independently or integrated within larger ASICs
  - Of course, the latter requires more widespread adoption of open-source processes by HEP projects
  - Long-term sustainability of the open-source model is also critically dependent on industry support
- As an example, we presented an open-source 8-bit SAR ADC with temperature-robust biasing
  - Early-stage work, to be taped out later in the year
- Future work will include higher-resolution open-source SAR ADCs by utilizing:
  - Deterministic dither-based calibration
  - Oversampling and noise shaping

Backup slides

Subtitle

Challenges

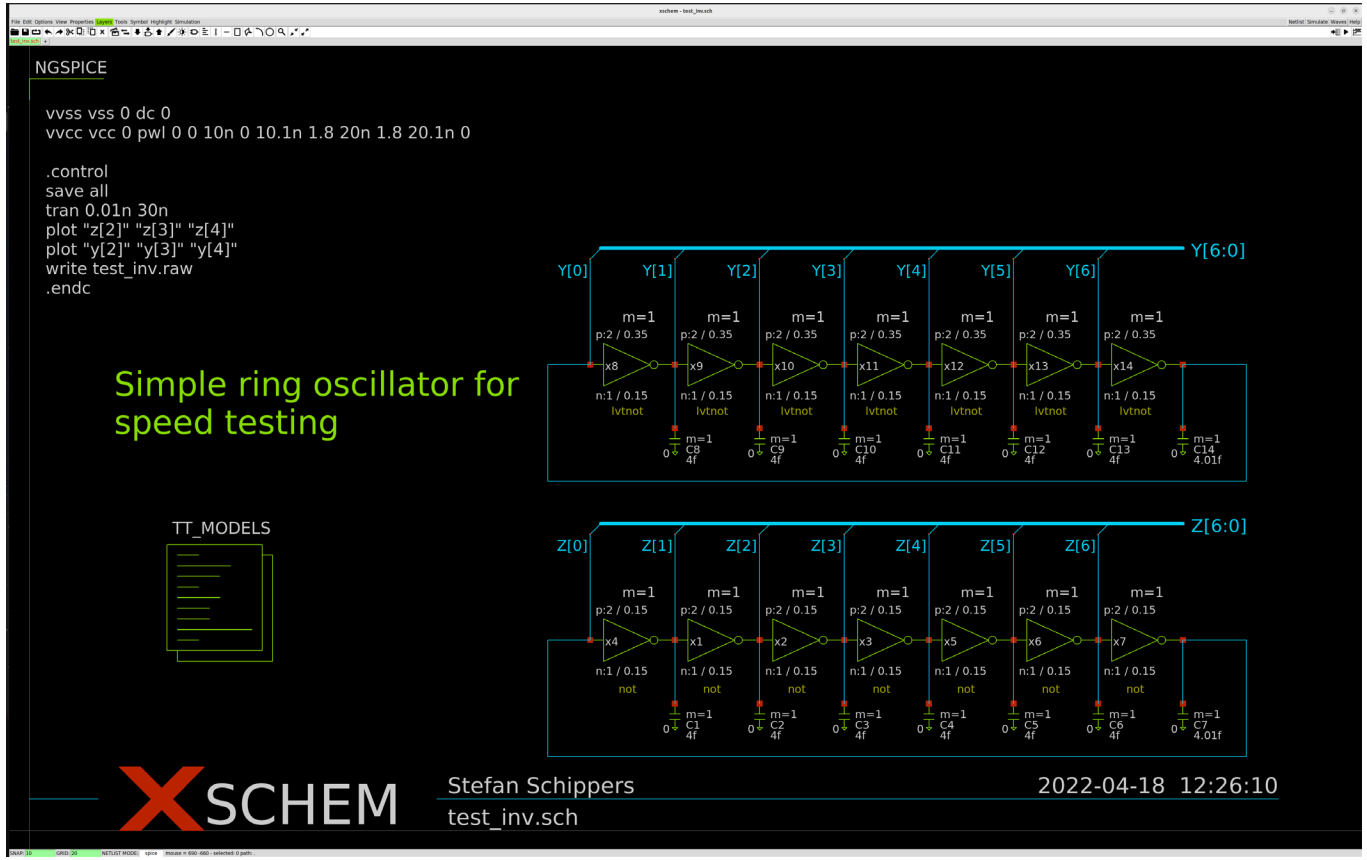
- Limited availability of open-source PDKs:
  - So far, only a few processes are available
  - Support for ReRAM macros and the SkyWater 90 nm process may be added soon
- FOSS CAD tools do not have all the capabilities of commercial tools.
  - They also do not include much technical support.
  - There is no straightforward process for tool management (e.g., rolling out updates), although the community is working to make the process easier.

Open-source circuit simulators

- Analog simulators
  - ngspice (http://ngspice.sourceforge.net/)
  - Xyce (https://xyce.sandia.gov/)
- While powerful, these simulators only support a limited set of simulation methods.
  - Important simulation methods for time-varying circuits (pss, pac, pnoise, etc.) are not yet available.
  - No true mixed-signal simulation tools available

Open-source schematic editors

- Analog / mixed-signal designs
  - Xschem (https://github.com/StefanSchippers/xschem)
  - Mosaic (https://github.com/NyanCAD/Mosaic)



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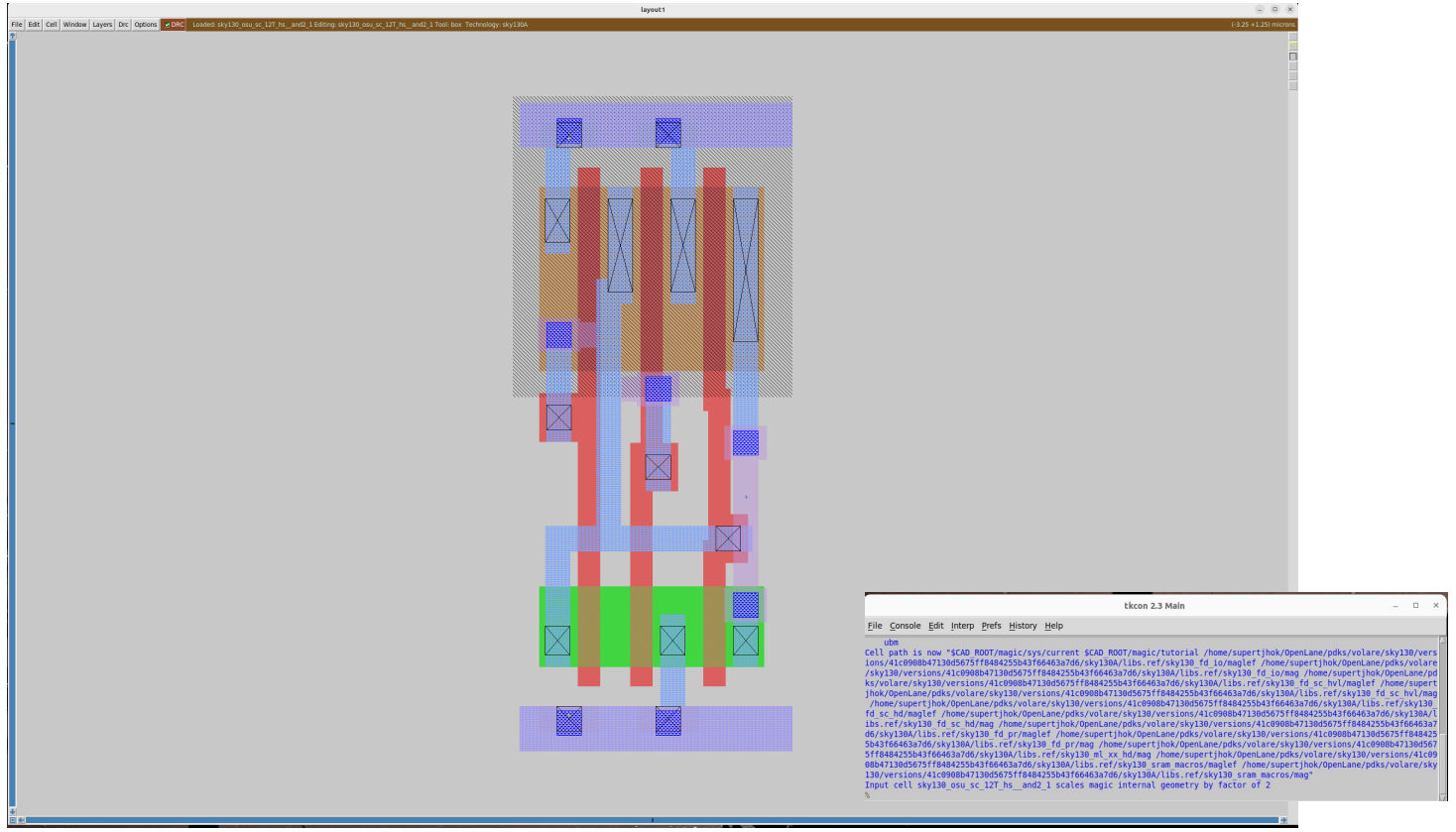
Open-source layout tools

- MAGIC (https://github.com/RTimothyEdwards/magic)
- KLayout (https://www.klayout.de)

- The default SKY130 layout flow (including DRC/LVS) is based on MAGIC.
- Klayout is mostly used as a GDS viewer, although it also has limited editing and DRC/LVS capabilities.



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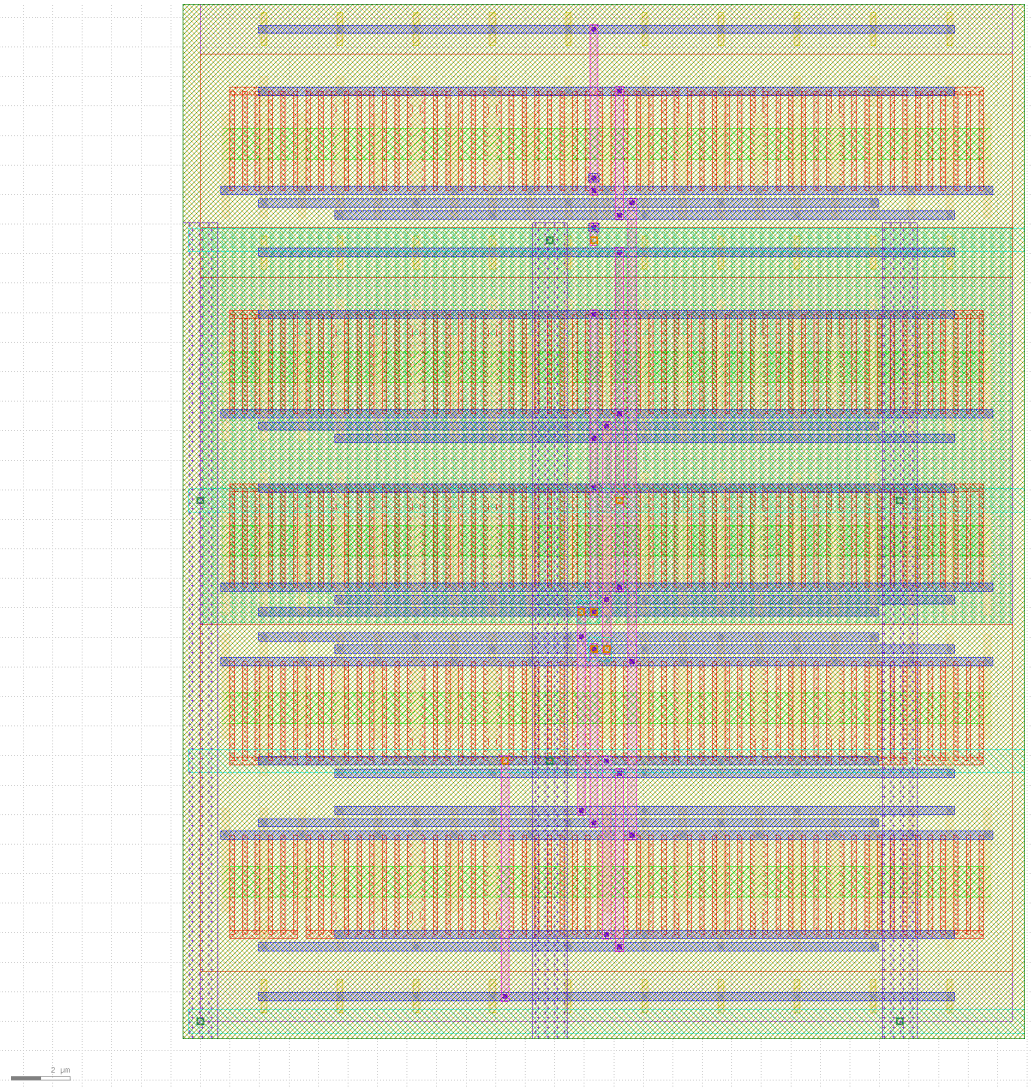
Digital design flow

- The default SKY130 installation includes a well-characterized digital standard cell library developed by Oklahoma State University (OSU).
- OpenLane (https://github.com/The-OpenROAD-Project/OpenLane).
  - OpenLane is an automated RTL to GDSII flow based on several components including OpenROAD, Yosys, Magic, Netgen, CVC, SPEF-Extractor, CU-GR, Klayout, and custom scripts for design exploration and optimization.
  - The flow performs full ASIC implementation steps from RTL all the way down to GDSII.
  - Synthesis and place & route efficiency is not as good as state of the art commercial tools, but comparable (layout area is typically 1.5x to 2x larger)

Other interesting open-source projects

- Automated analog layout generation
  - ALIGN (https://github.com/ALIGN-analoglayout/ALIGN-public)
  - Sky130 PDK support for ALIGN (https://github.com/ALIGN-analoglayout/ALIGN-pdk-sky130)
  - MAGICAL (https://github.com/magical-eda/MAGICAL)
- These tools try to satisfy the usual analog layout constraints (such as matching).
  - In many cases, post-layout performance is similar to hand-optimized layout.



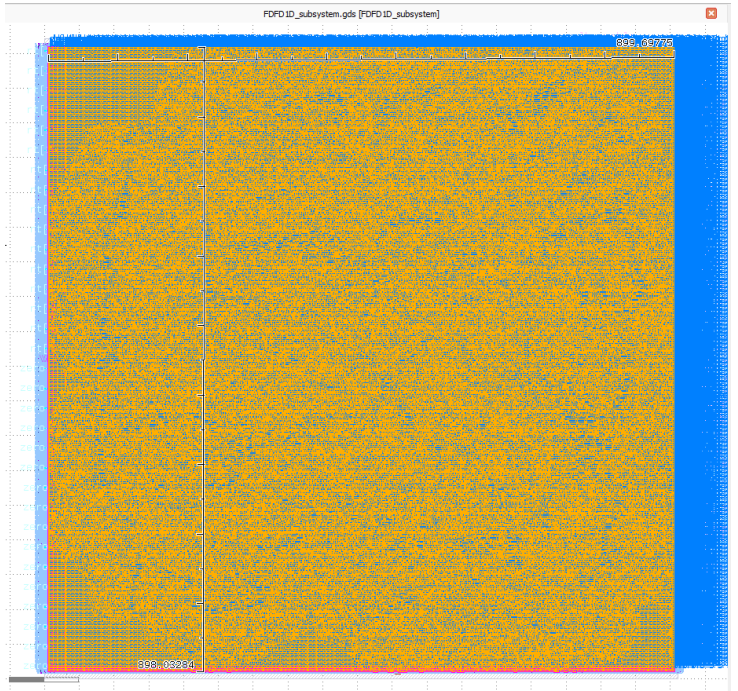
Automatically laid-out 5-transistor OTA in the SKY130 process

So how do I get started?

- The easiest way is probably to clone one of the following pre-configured Docker containers from GitHub:
  - IIC-OSIC-TOOLS: https://github.com/hpretl/iic-osic-tools
  - FOSS-ASIC-TOOLS: https://github.com/efabless/foss-asic-tools
- Alternatively, you can of course individually download and install each of the tools yourself…
- For the latest discussions, join the “skywater-pdk” Slack channel and its various sub-channels.
- Also, consider joining various related events:
  - IEEE SSCS “PICO” open-source chipathon: https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-design-contest
  - IEEE SSCS/CAS Foundations of mixed-signal ASIC design workshop (using Tiny Tapeout): https://events.vtools.ieee.org/m/432337
  - Zero to ASIC course: https://www.zerotoasiccourse.com/

Choice of fabrication process

- The SkyWater S130 CMOS process has several advantages:
  - Mature process (5M1P, MIM caps, multiple V_T options) with many successful products on the market
  - Excellent for analog / mixed-signal design (low gate leakage current, high-voltage transistors, high intrinsic device gain)
  - Free and open-source PDK available for both open-source CAD tools and Cadence
  - Additional (not open source) RRAM macro available from Weebit Nano
  - Fully-functional automated RTL-GDSII digital flow available using OpenLane (also free and open-source)
  - Large (and growing) database of working circuit designs are freely available
  - Supports low-cost chip prototyping ($9,750 including dicing, packaging, and assembly) using the chipIgnite program from eFabless
- Radiation and cryogenic models are not yet available, but:
  - Robust circuit designs can be completed in the absence of such models
  - Development of such models for the HEP community can be an interesting outcome of any funded project



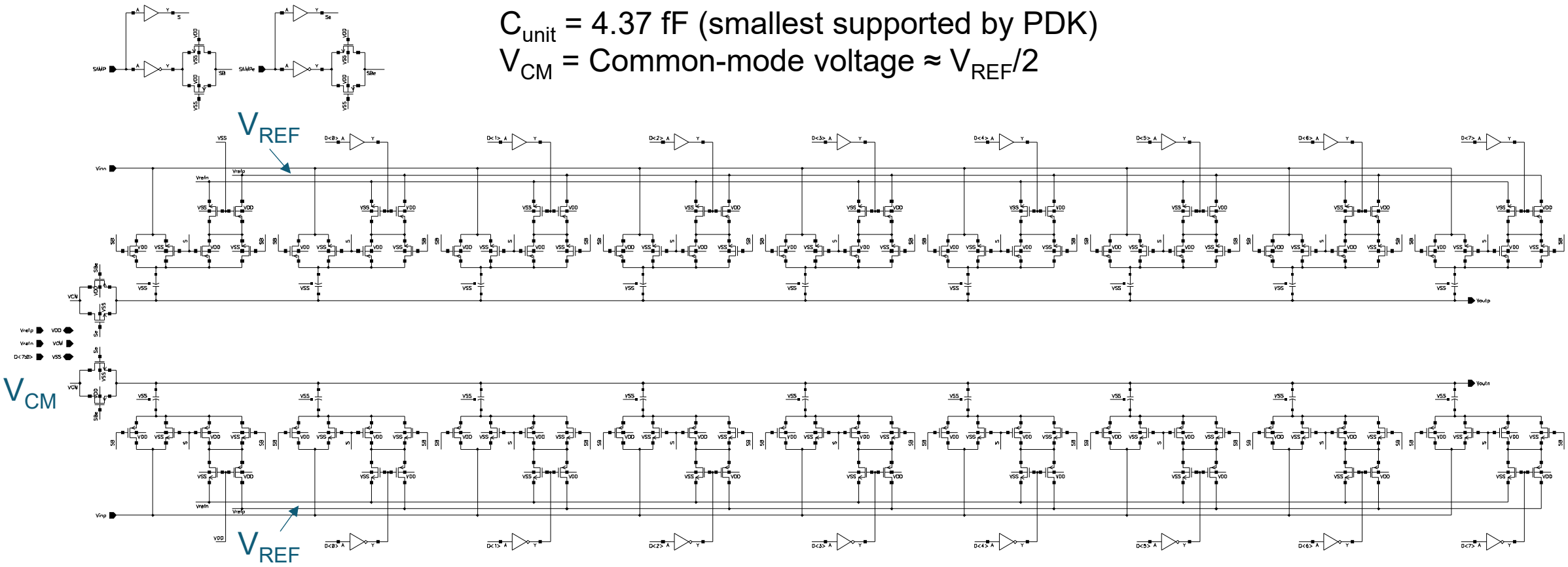
Layout of a digital processor (area = 900 µm x 900 µm) generated from RTL in the S130 process using the OpenLane flow

HEP = High-energy physics

Capacitor DAC

- Standard fully-differential binary weighted 8-bit capacitor DAC.
- Designed for bottom-plate sampling, which improves linearity.

C_{unit} = 4.37 fF (smallest supported by PDK)
V_{CM} = Common-mode voltage ≈ $V_{REF}/2$



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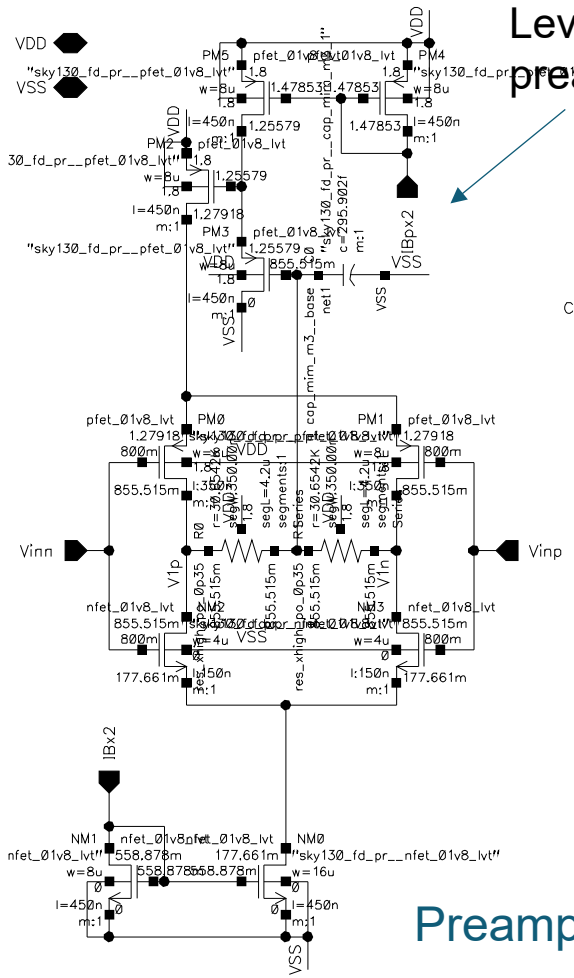
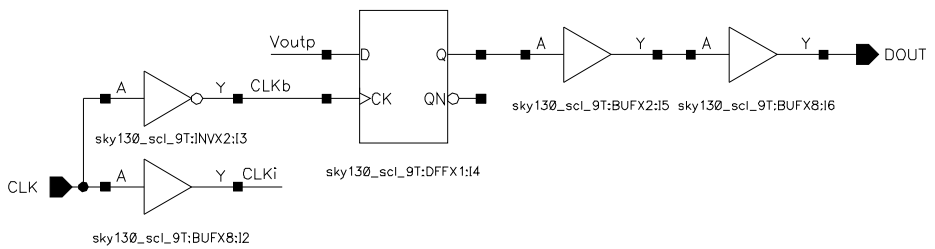
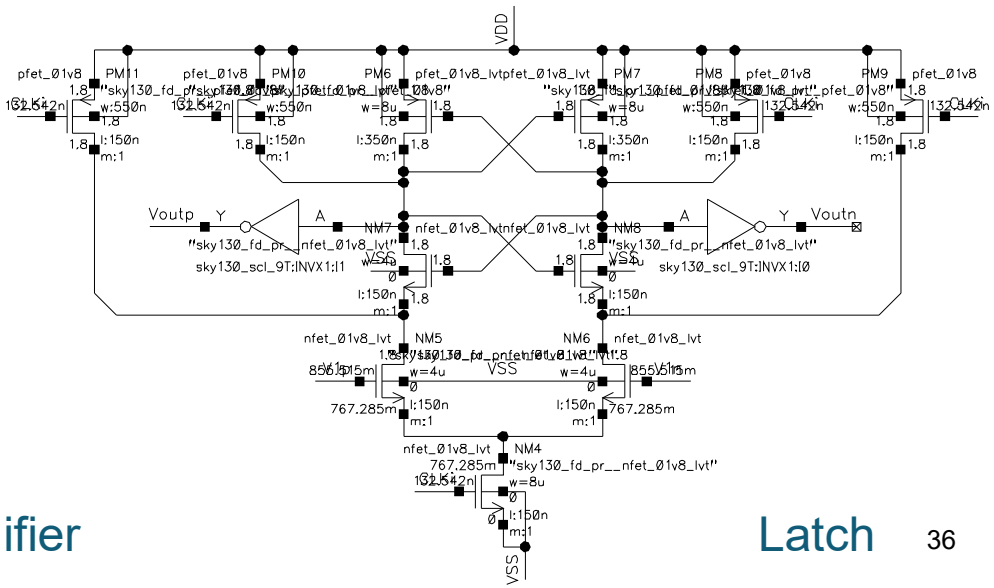
Dynamic comparator

- Two-stage dynamic comparator
  - Inverter-based preamplifier to reduce input-referred offset and kickback into the DAC.
  - StrongARM latch to generate logic-level outputs.



Level shifter for preamplifier's output V_{CM}



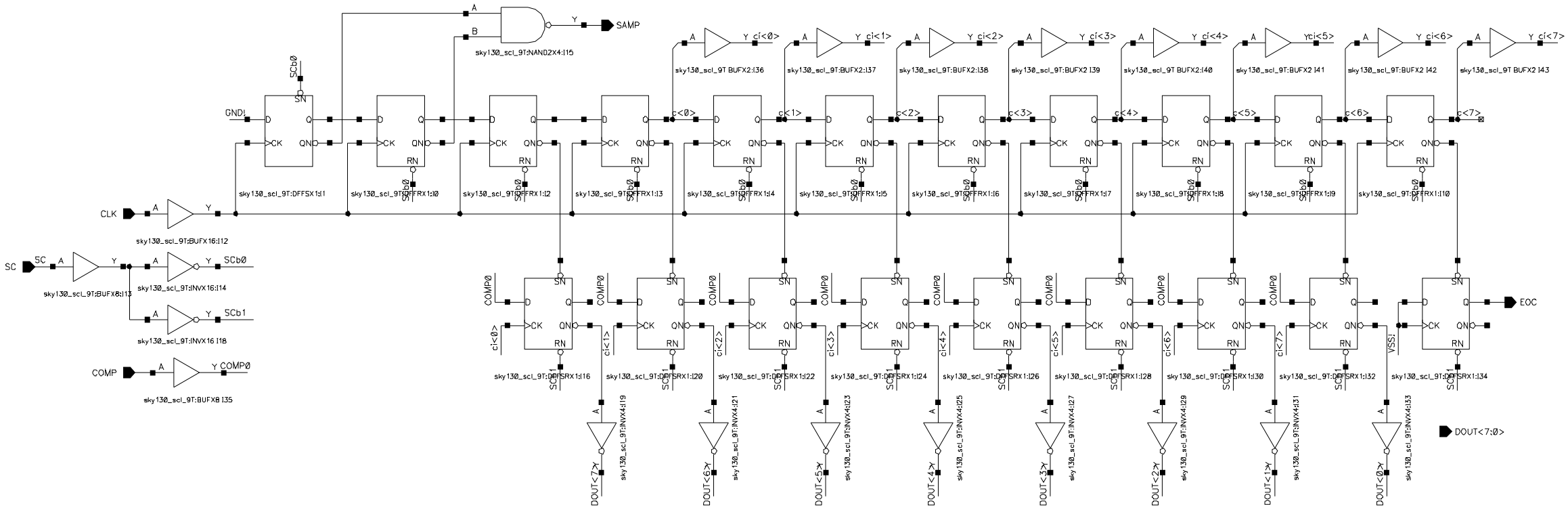


Preamplifier

Latch

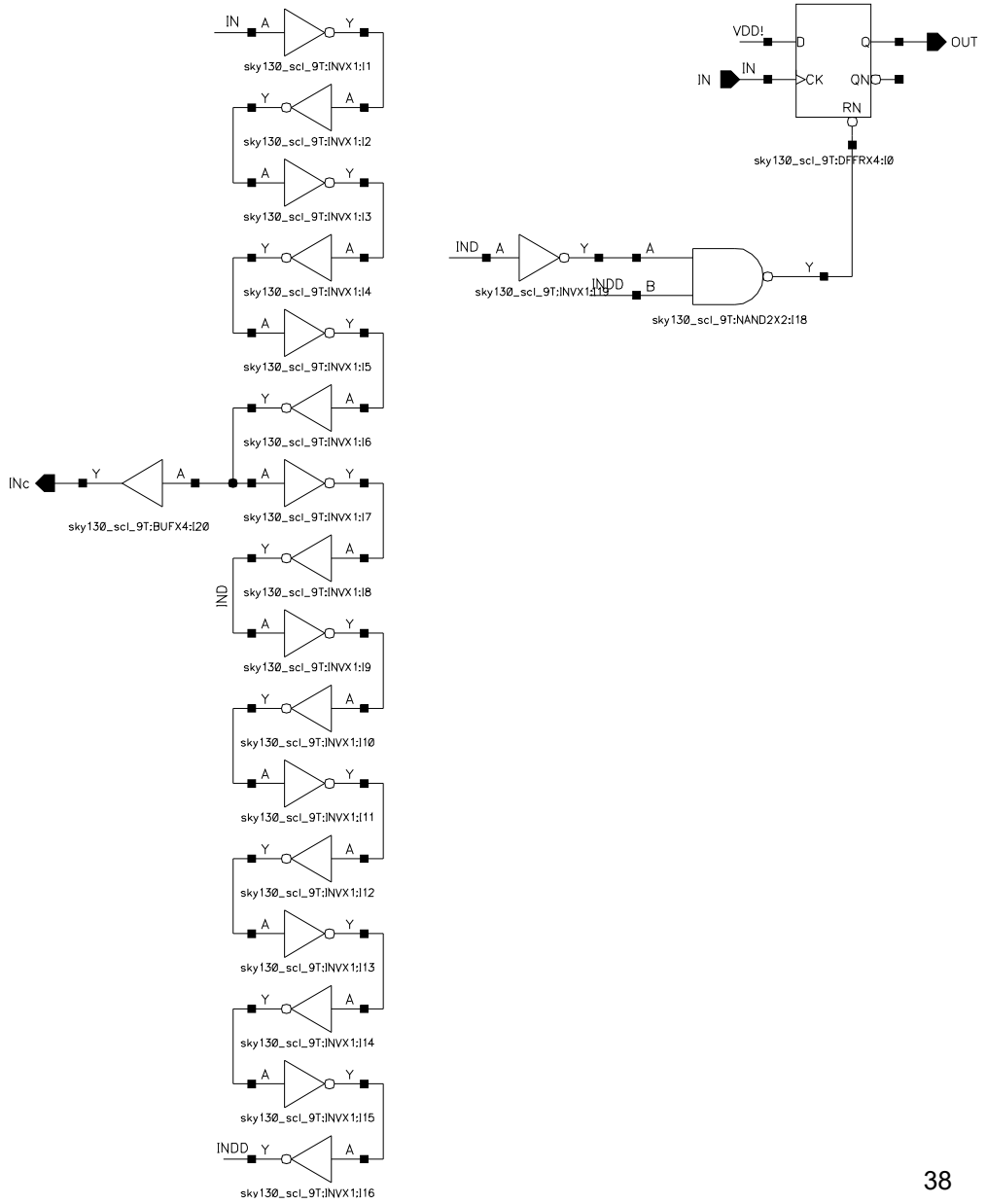
SAR logic

- Standard synchronous implementation using standard cells and static logic.
- Can be easily extended to higher-resolution designs.



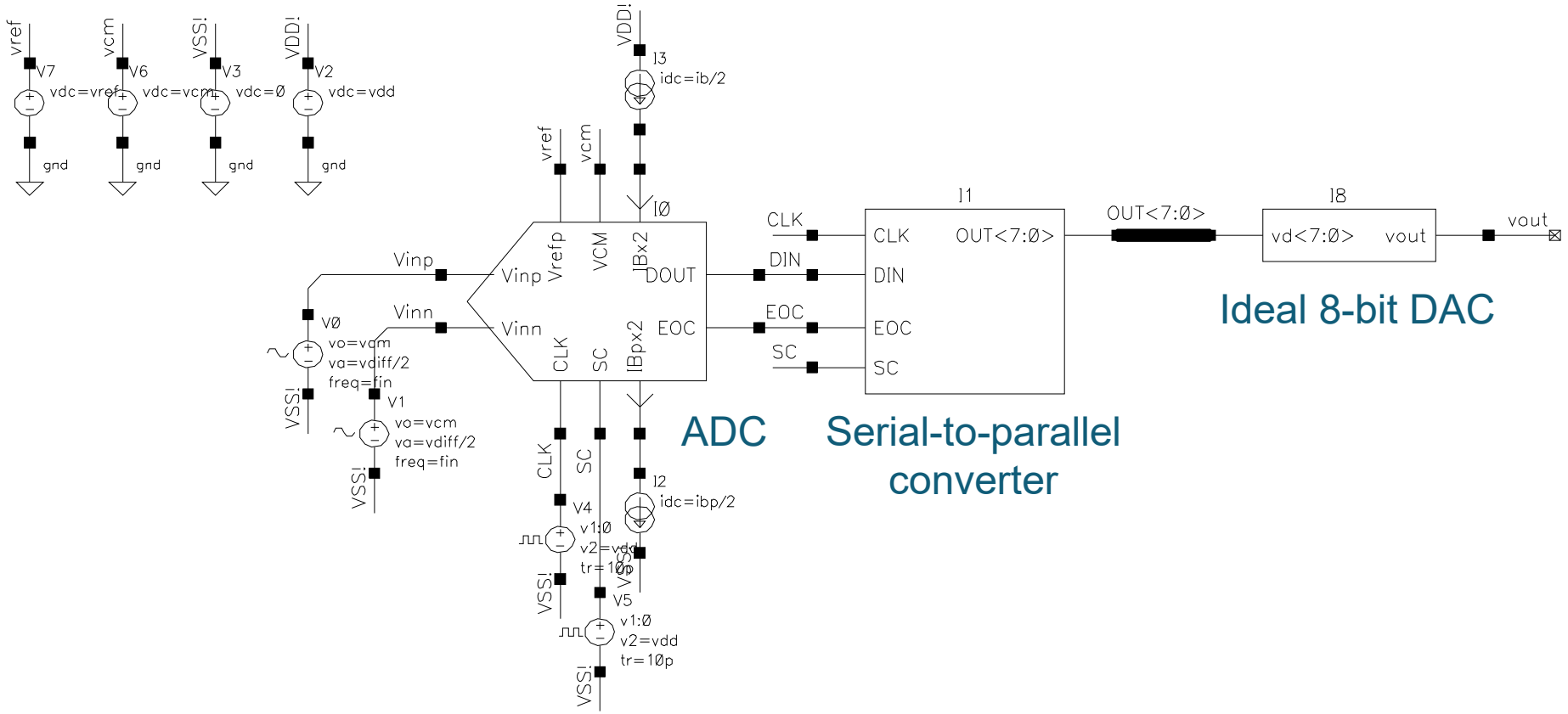
Pulse stretcher

- Used to generate SAMP and SAMPe control signals for the capacitive DAC.
- SAMPe controls the top-plate switch (connected to V_{CM}), which should turn off slightly before SAMP to prevent charge sharing.



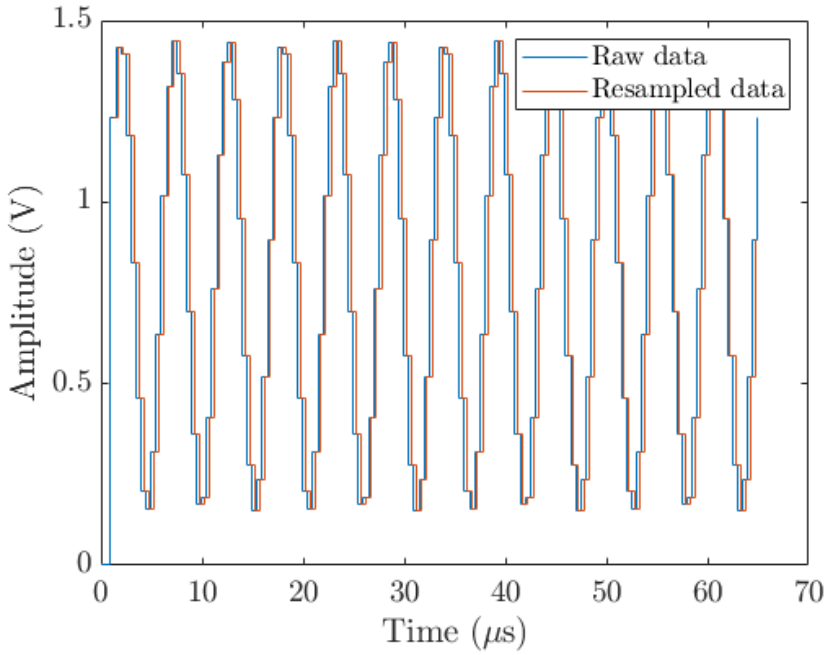
Test bench for the SAR ADC

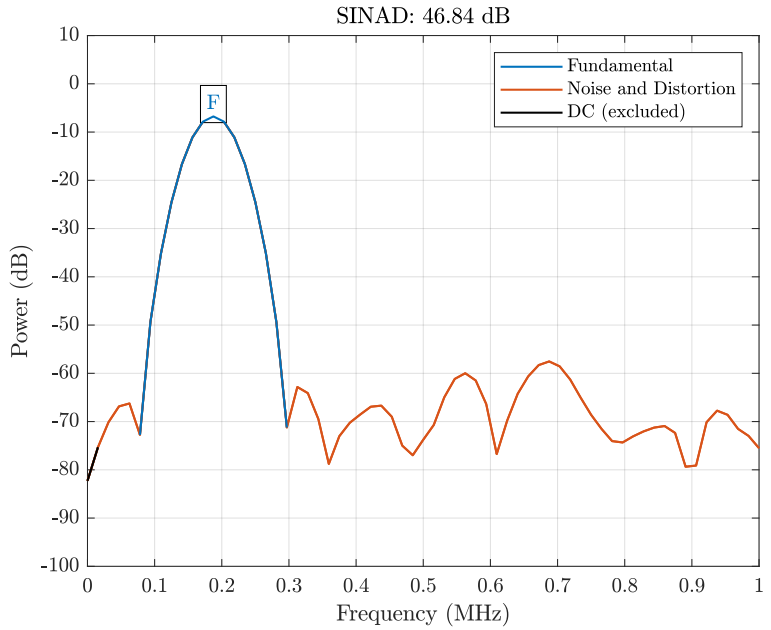
- Assumes ideal input voltage sources
- Also assumes ideal reference and common-mode voltages and bias currents



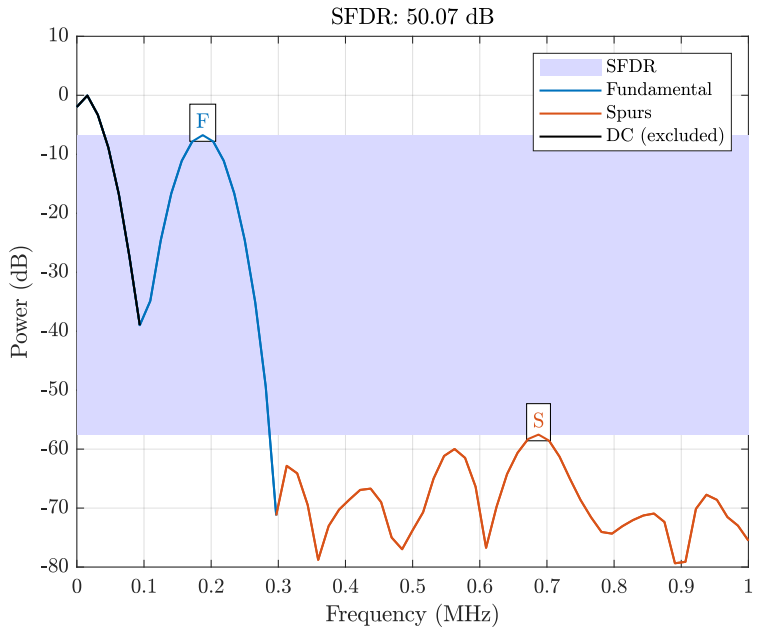
ADC simulation results at 2 MS/s

- Full-scale voltage, V_{FS} = 1.5 V, common-mode voltage, V_{CM} = 0.75 V
- Sine wave input at (3/32) x f_s = 187.5 kHz, nearly full-scale (1.3 V_{pp})
- Power supply voltage, V_{DD} = 1.8 V
- SNDR and SFDR computed using MATLAB





SNDR = 46.84 dB
ENOB = 7.5 bits



SFDR = 50.07 dB

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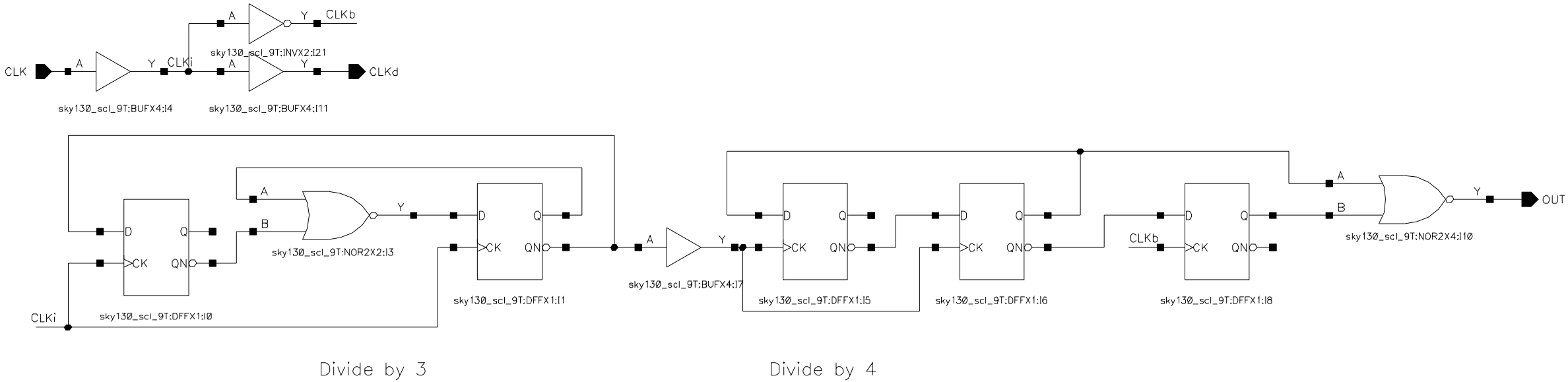
Sampling pulse generator

- Consists of a divide-by-12 circuit followed by a pulse generator
- The generated pulses have an output width of ≈$1/(2f_{clk})$



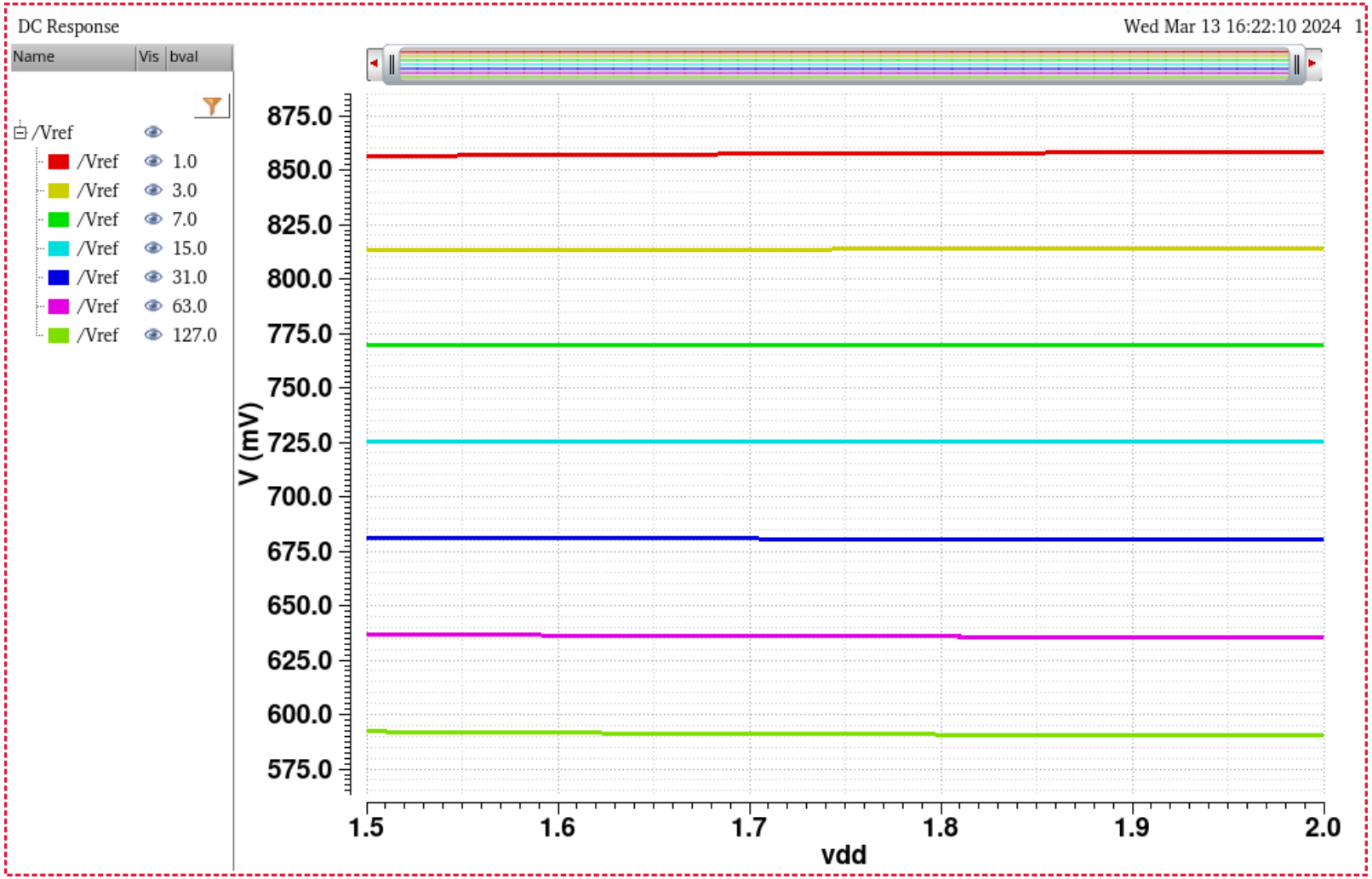
Divide by 3

Divide by 4

Temperature-compensated reference (3)

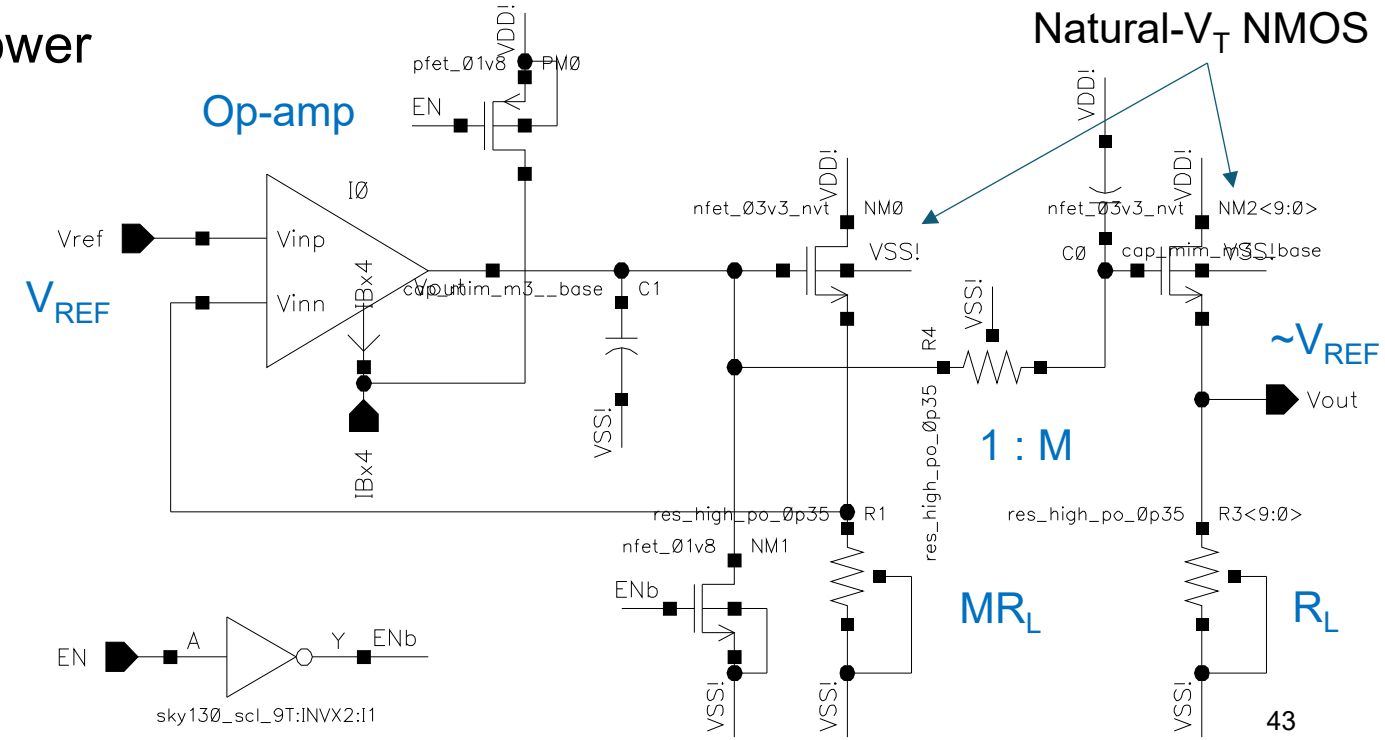
- Use of cascaded mirrors results in excellent supply regulation

Temperature = 25°C



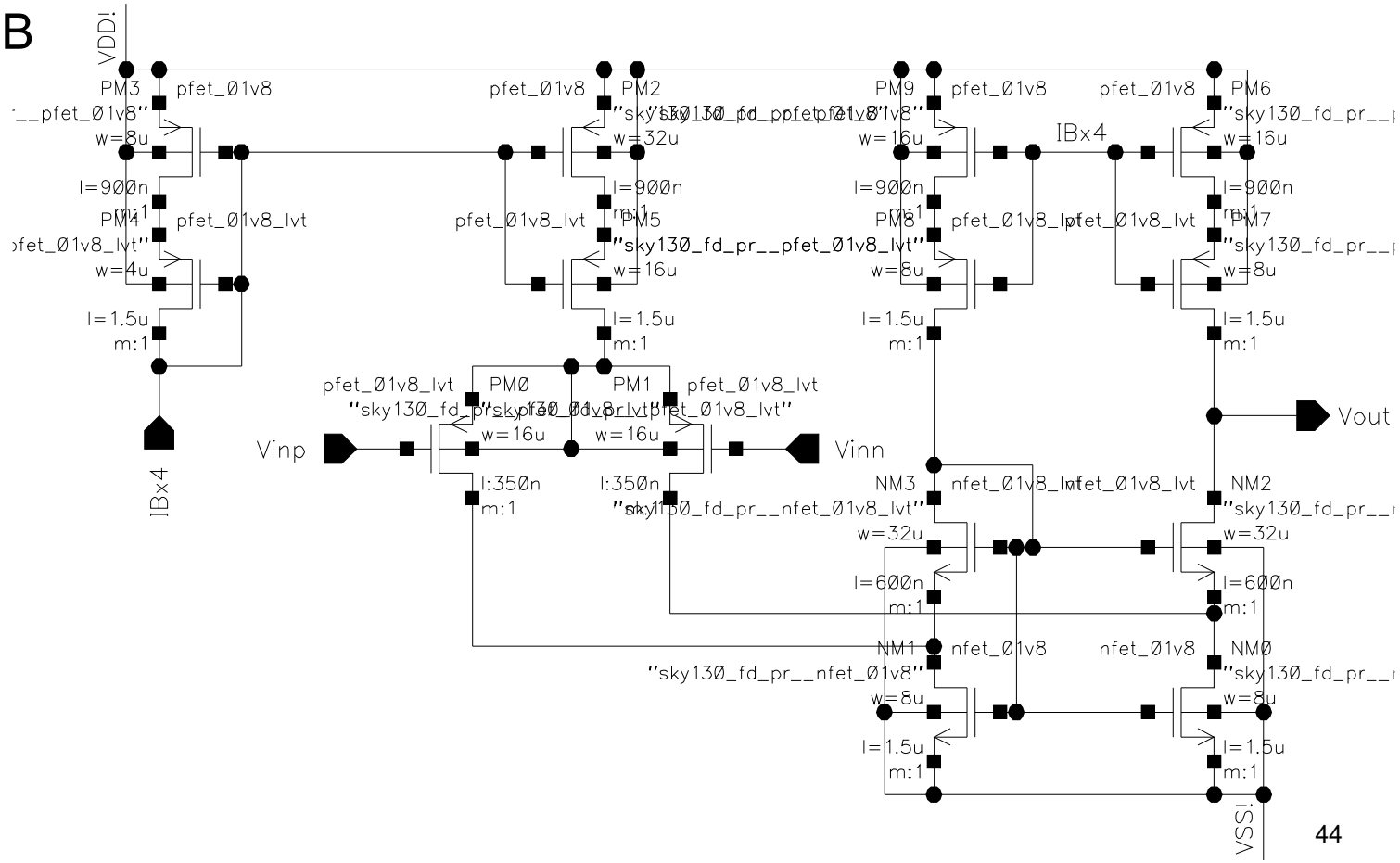
Common-mode voltage generator

- Similar to the reference voltage generator but does not need an intermediate level shifter since the output voltage is lower
- Trade-off between output impedance (R_L || $1/g_m$) and power consumption
  - Nominal V_{REF} = 0.725 V
  - Nominal output resistance, R_L = 1.1 kΩ
  - Results in a current consumption ≈ 750 µA (dominated by the output stage)
- Includes shutdown function to save power



Op-amp

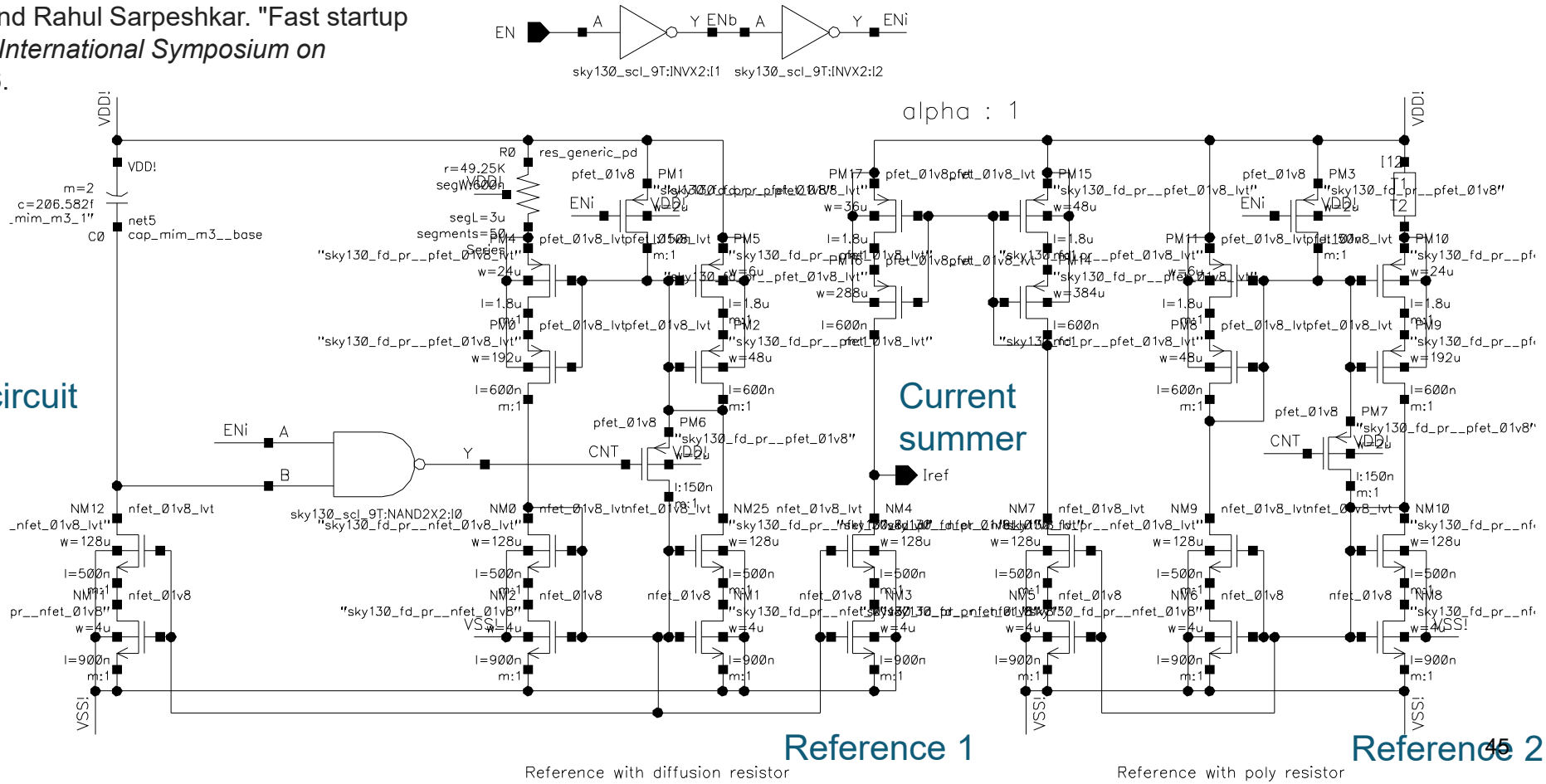
- Used by the V_{REF} and V_{CM} generators
- Standard folded-cascode design with PMOS inputs
- Compensated at the output node
- Simulated DC voltage gain = 60 dB



Current reference (2)

- Each reference is a standard constant-G_m circuit.
- Mirrors are self-cascaded (with regular and low-V_T transistors) to improve supply regulation.
- Includes POR-like capacitive startup circuit[1].

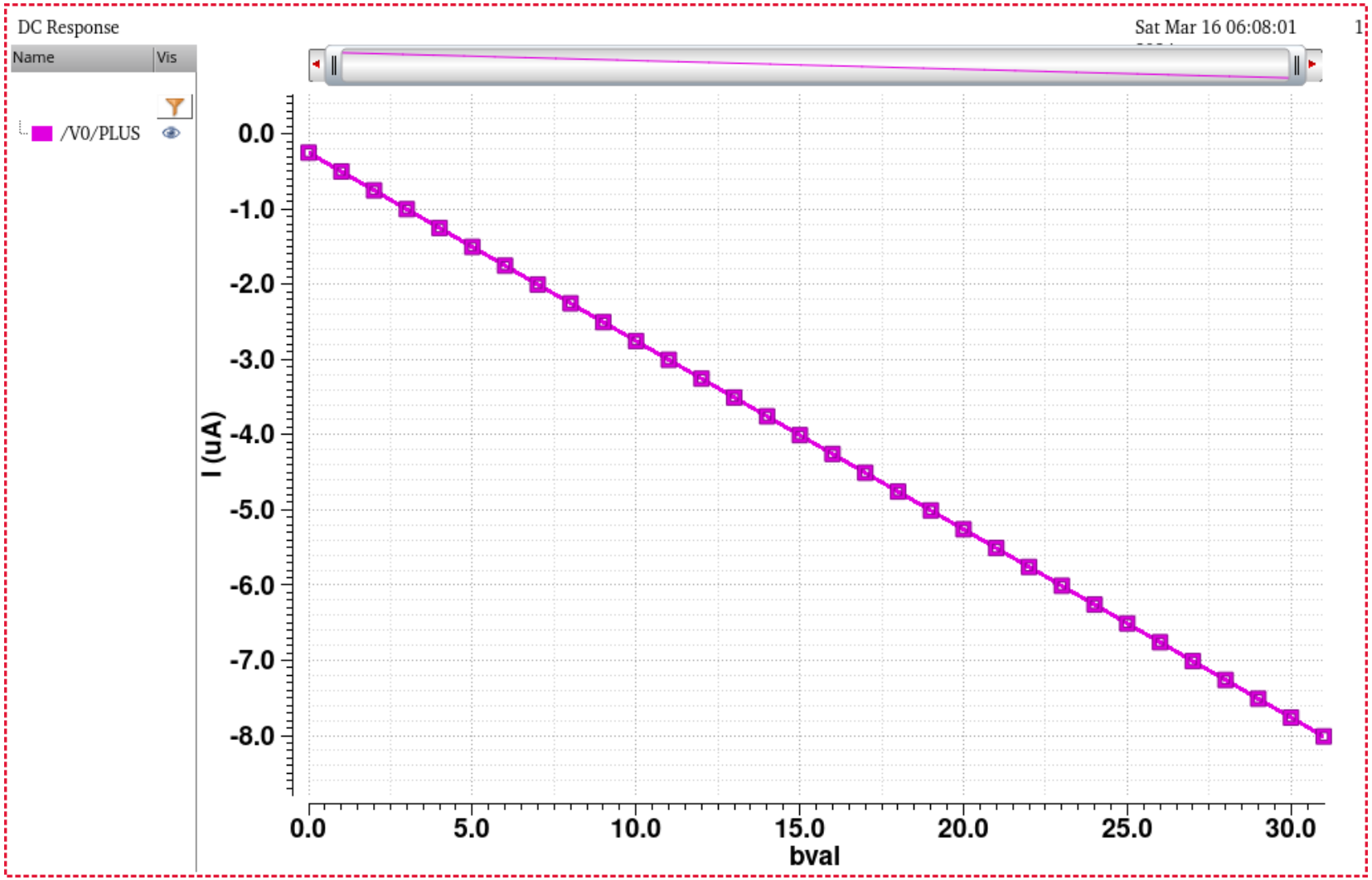
[1]Mandal, Soumyajit, Scott Arfin, and Rahul Sarpeshkar. "Fast startup CMOS current references." *IEEE International Symposium on Circuits and Systems*. IEEE, 2006.



Current DAC (2)

- Simulated transfer function shows high linearity.

I_{in} = 1 µA



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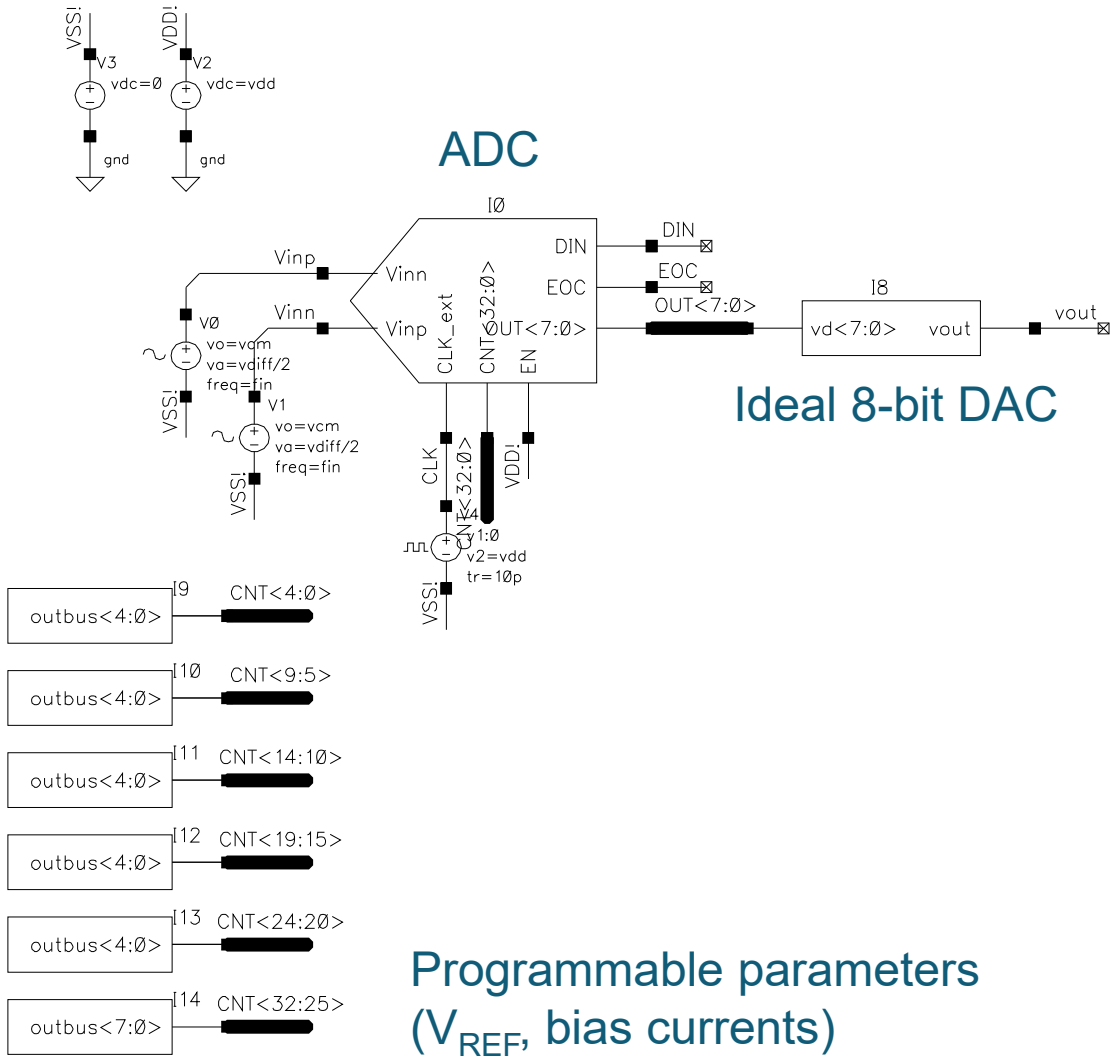
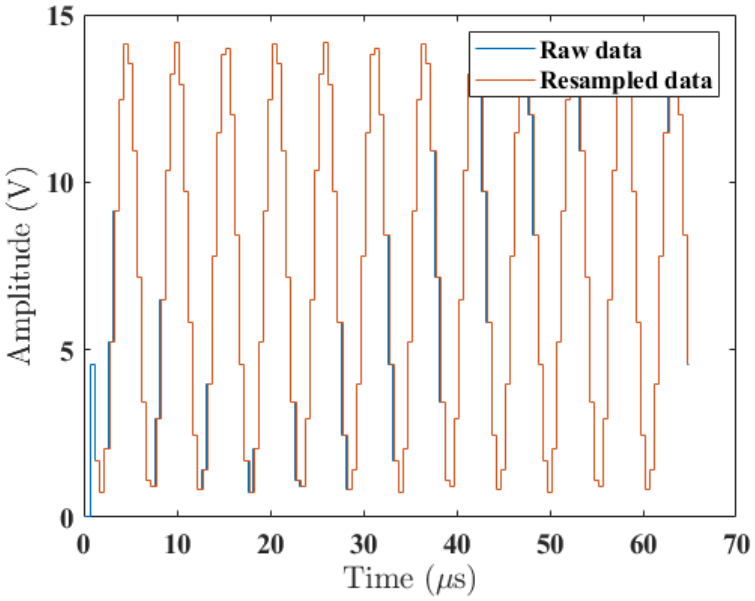
Test bench for the complete SAR ADC

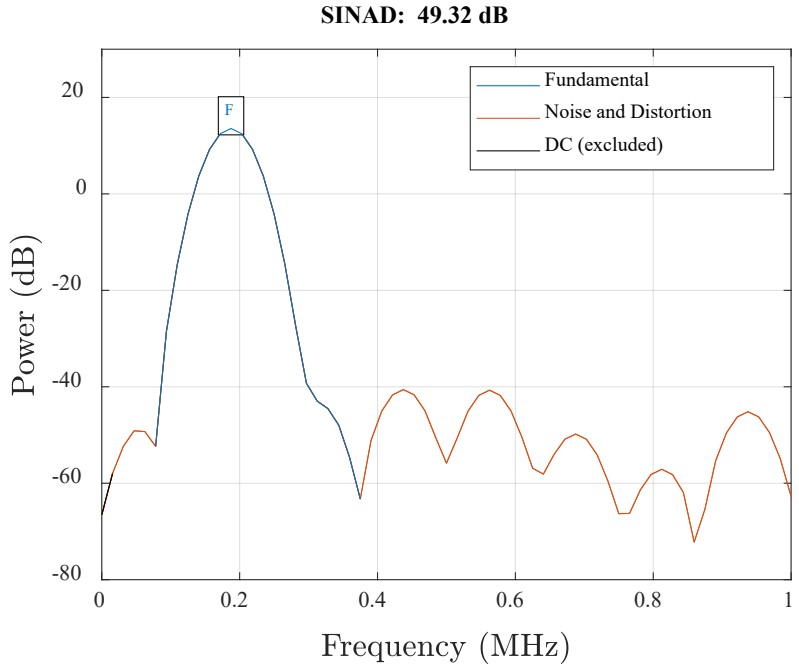
- Self-contained design, only needs the power supplies and clock (= $12f_s$) to function
- Includes shutdown function (EN) to save power when not being used



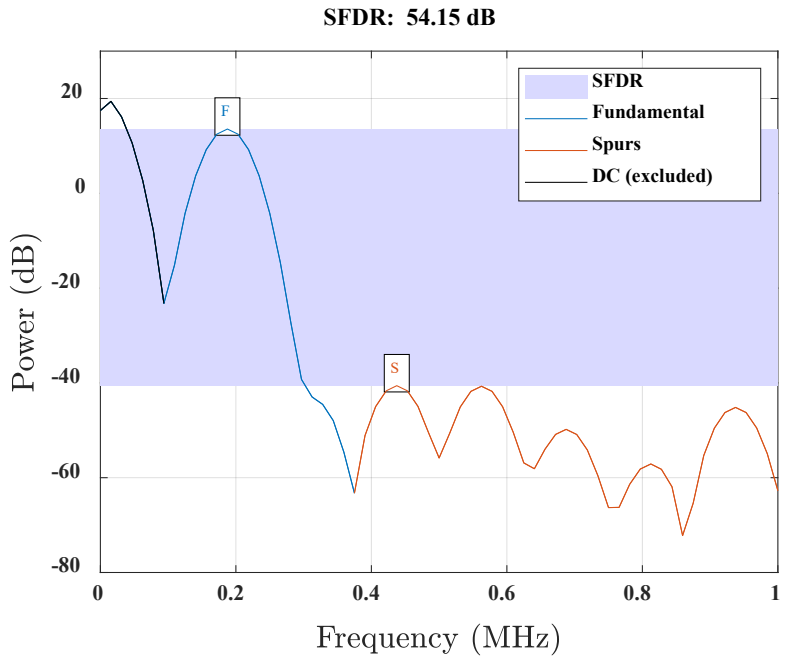
Full ADC simulation results at 2 MS/s

- Full-scale voltage, V_{FS} = 1.45 V, common-mode voltage, V_{CM} = 0.725 V
- Sine wave input at (3/32) x f_s = 187.5 kHz, nearly full-scale (1.3 V_{pp})
- Power supply voltage, V_{DD} = 1.8 V
- SNDR and SFDR computed using MATLAB





SNDR = 49.32 dB
ENOB = 7.9 bits



SFDR = 54.15 dB

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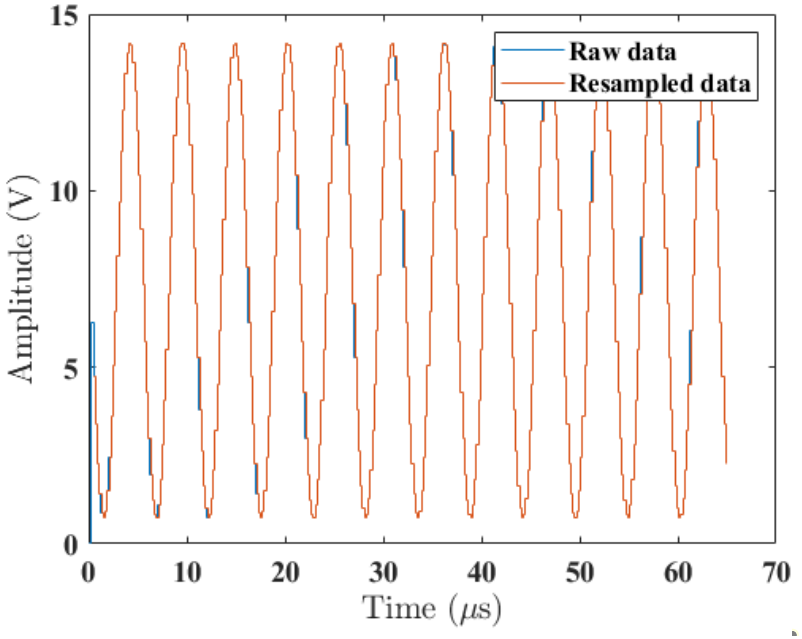
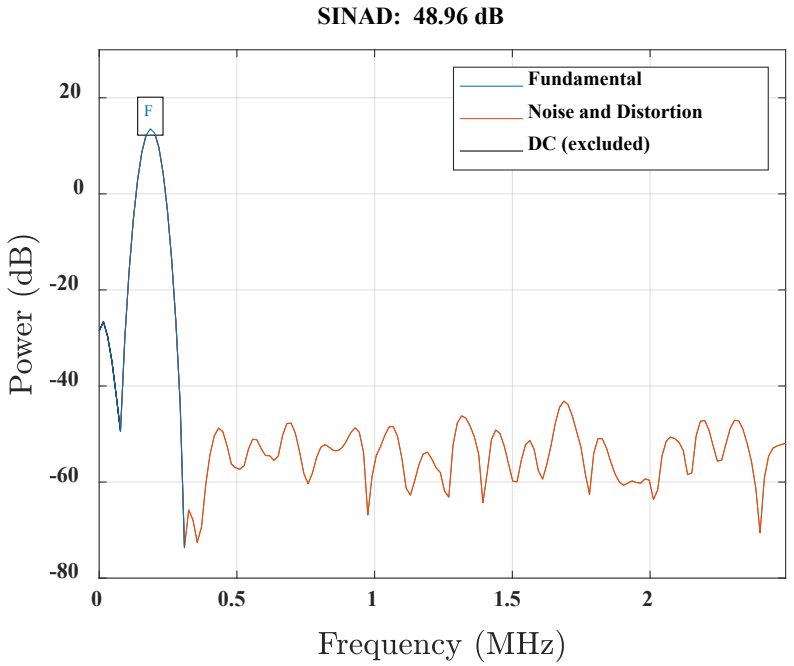
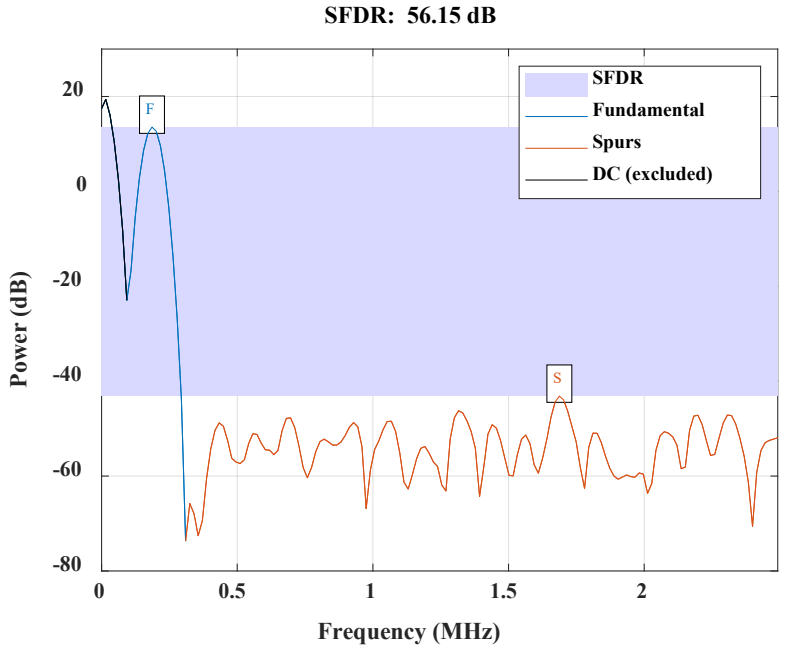
Full ADC simulation results at 5 MS/s

- Full-scale voltage, V_{FS} = 1.45 V, common-mode voltage, V_{CM} = 0.725 V
- Sine wave input at (3/80) x f_s = 187.5 kHz, nearly full-scale (1.3 V_{pp})
- Power supply voltage, V_{DD} = 1.8 V
- SNDR and SFDR computed using MATLAB





SNDR = 48.96 dB
ENOB = 7.8 bits



SFDR = 56.15 dB

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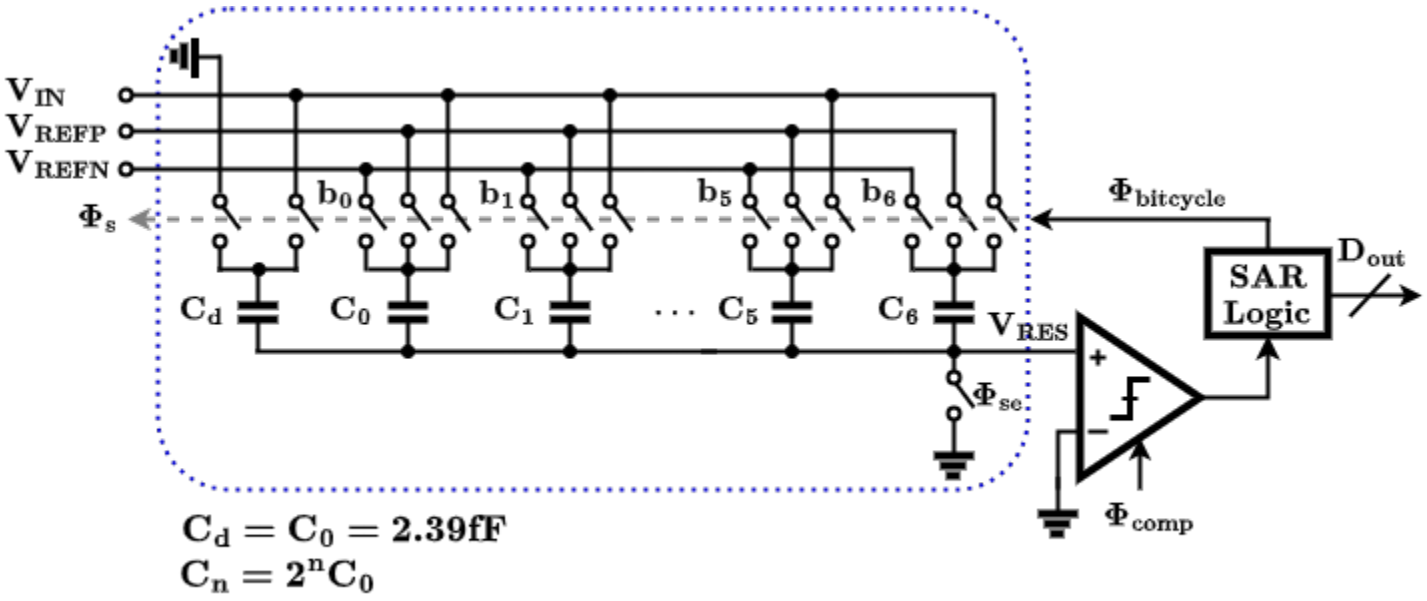
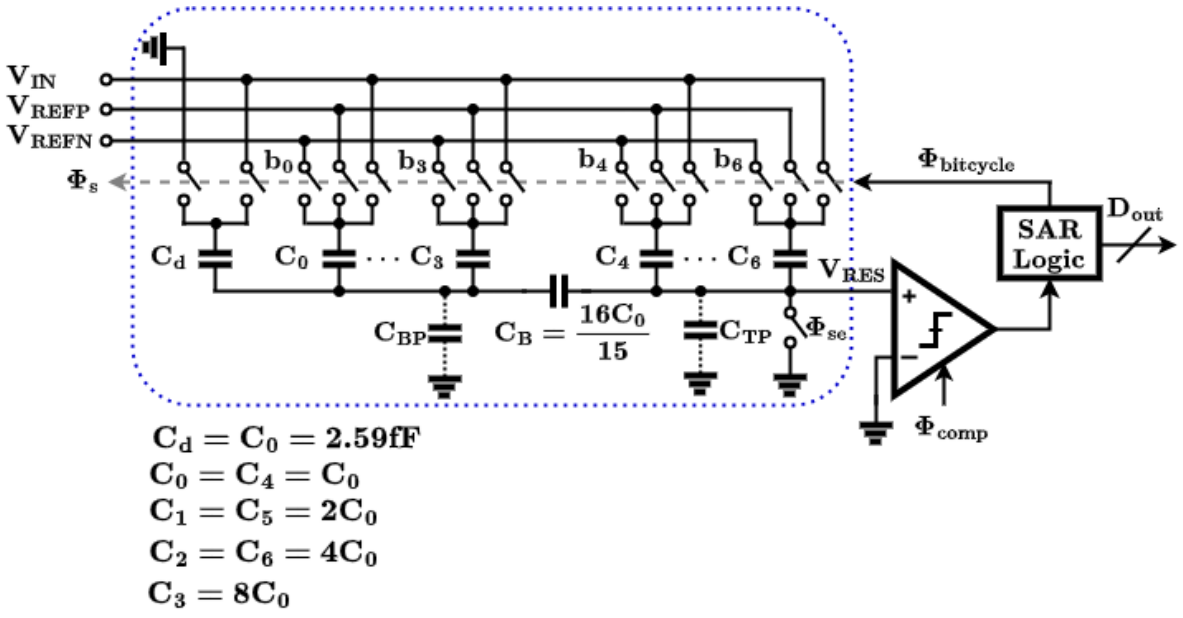
Binary weighted DAC



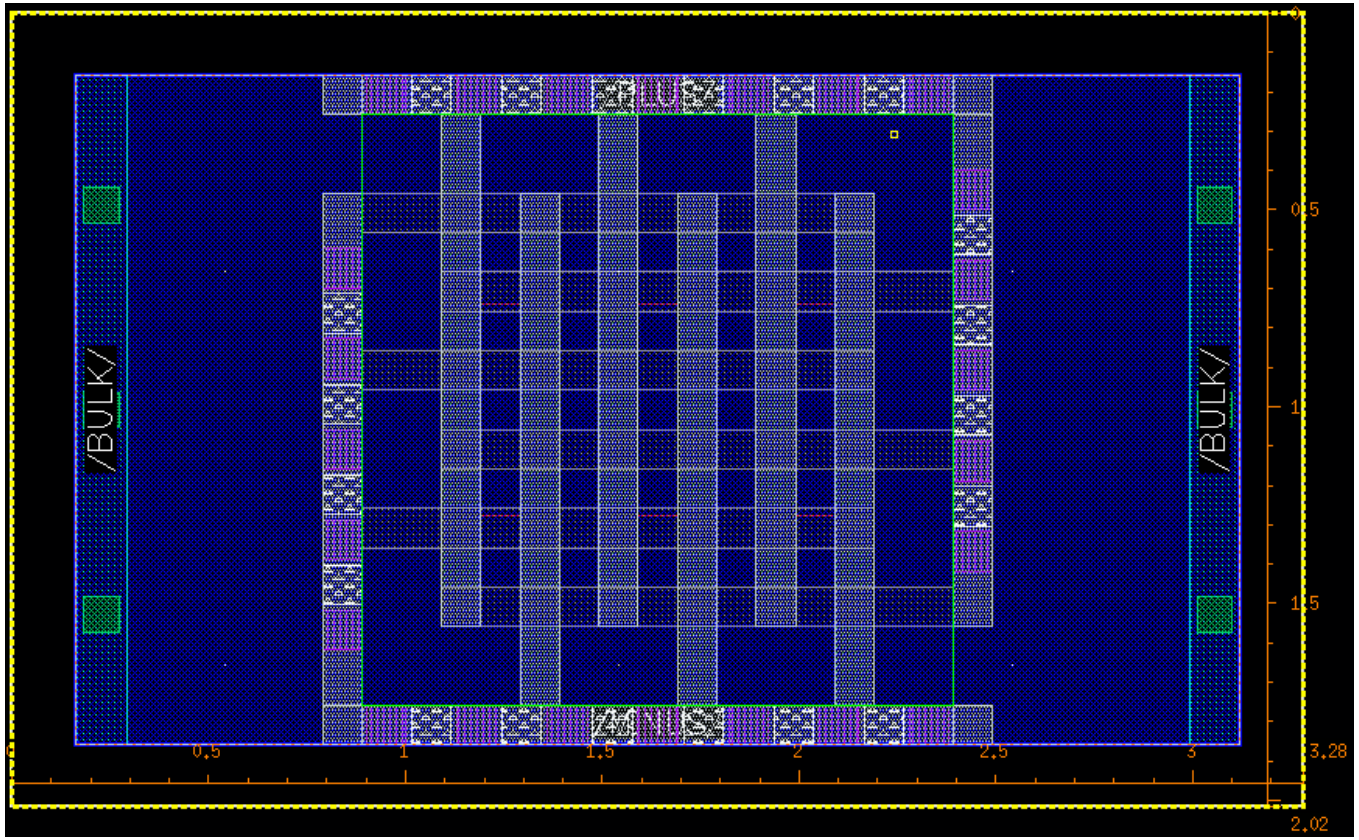
- 7-bit binary weighted SAR ADC with MOM-capacitor is shown.
- Requires large capacitance values with the highest capacitor = $64C_0$ = 152.96 fF.
- The effective capacitance of the CDAC is 128 C_0= 305.92 fF.
- Large capacitors require large switch sizes for connecting to V_{IN} or V_{REF}.

Split capacitor DAC

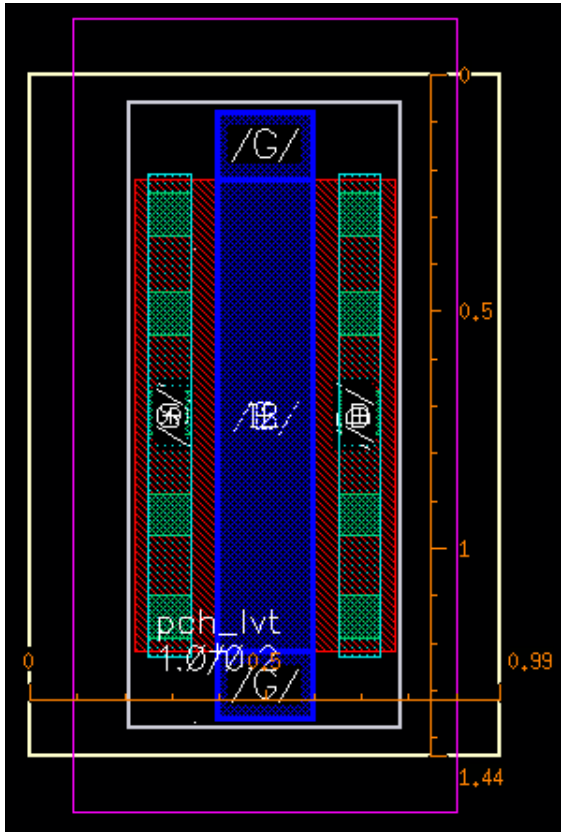


- 7-bit Split CDAC-based MOSCAP SAR ADC occupies a smaller area compared to binary-weighted SAR ADC with the effective capacitance of the CDAC being $8C_0$ = 20.72 fF.
- The downside of split CDAC is bottom plate parasitic capacitance of the bridge capacitor which can be ignored for a 7-bit ADC. Extracted simulations of a 7-bit ADC give an ENOB of 6.2 bits at a master clock of 500 MHz.
- Area can be further reduced by using a custom-designed metal capacitor for the bridge cap with capacitance of 3.44 fF and parasitic capacitances of 1.284 fF on either side.
- Using MOSCAP as a bridge capacitor increases area due to different body connections of the MOSFET. MOSFETs with different body connections must be spaced apart to meet design rule guidelines.
- Higher bridge capacitance value is considered to account for layout parasitics.

Layout of MOMCAP vs MOSCAP



Area of MOMCAP = 6.62 μm^2



Area of MOSCAP = 1.42 μm^2

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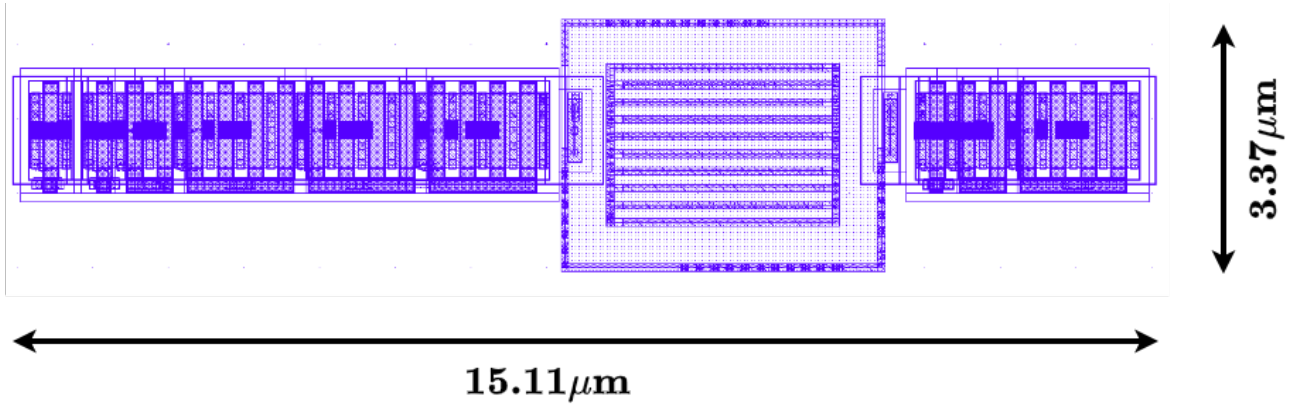
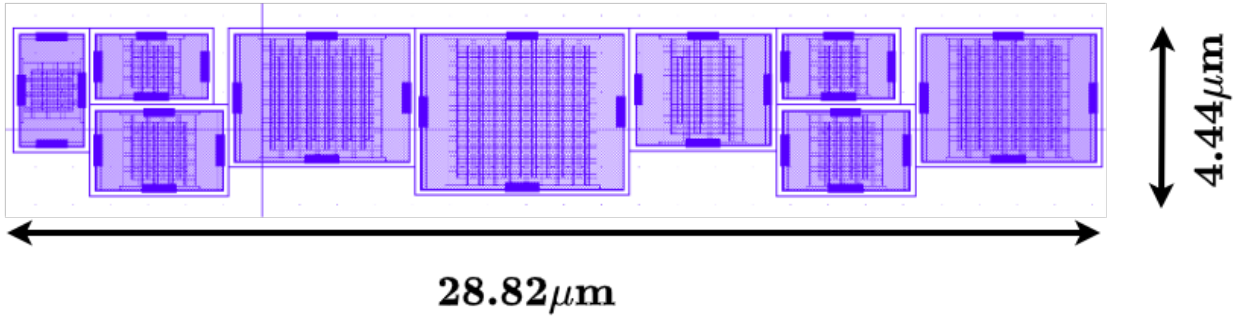
Layout of MOMCAP vs MOSCAP (2)

- The minimum capacitor provided by TSMC 65nm is a MOMCAP of area 6.62 μm^2.
- The MOSCAP used in the design is a PMOS with L= 200 nm and W = 1 μm occupying an area of 1.42 μm^2.
- The total area of a CDAC with a MOSCAP-based design is 83.5 μm^2 compared to $\approx$270 μm^2 with MOMCAPs.
- The area efficiency of MOSFET-based capacitive DAC is higher than capacitors provided by the foundry.

Layout of MOSCAP vs MOMCAP (3)





- The capacitor area in MOSCAP CDAC is 50.97 μm^2.
- The capacitor area in MOMCAP CDAC is 127.96 μm^2 which is 2.5 times larger than MOSCAP-based CDAC.

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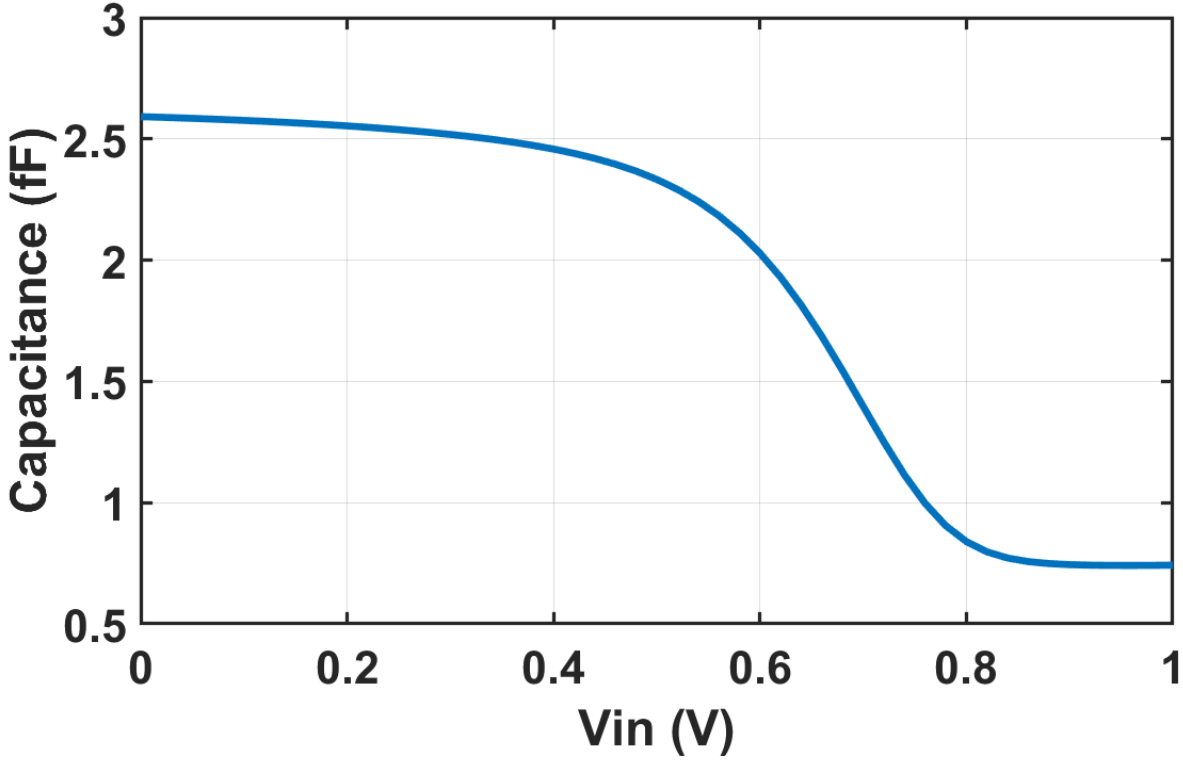
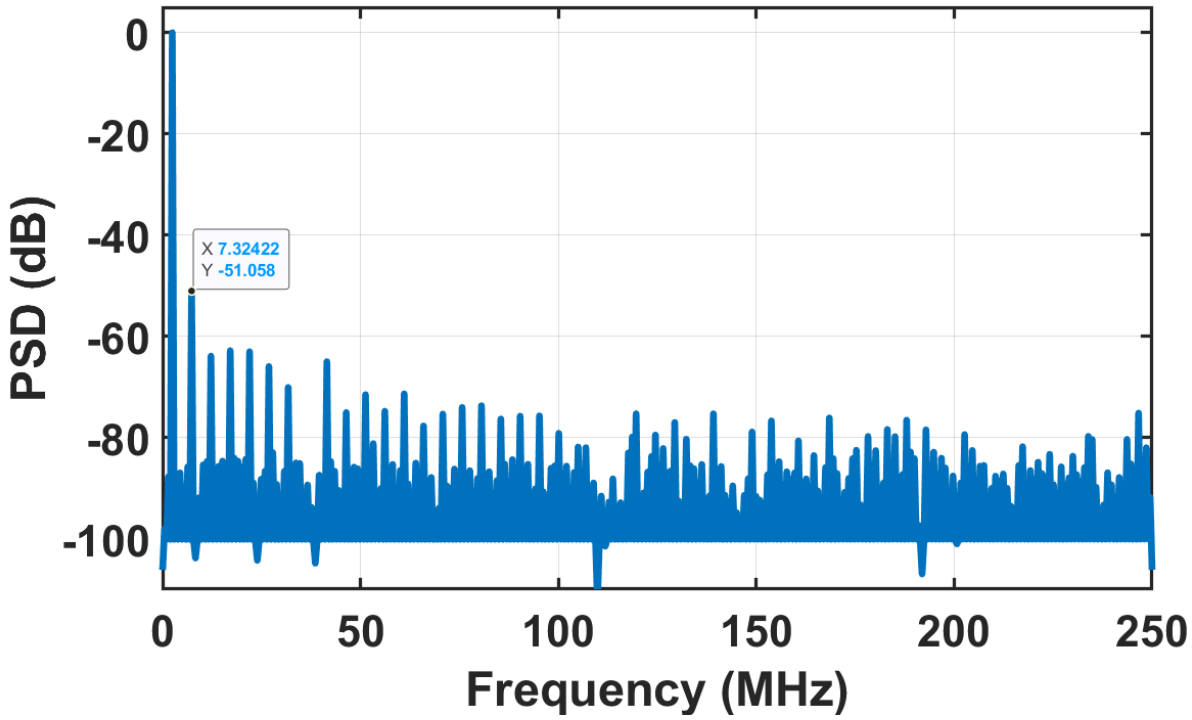
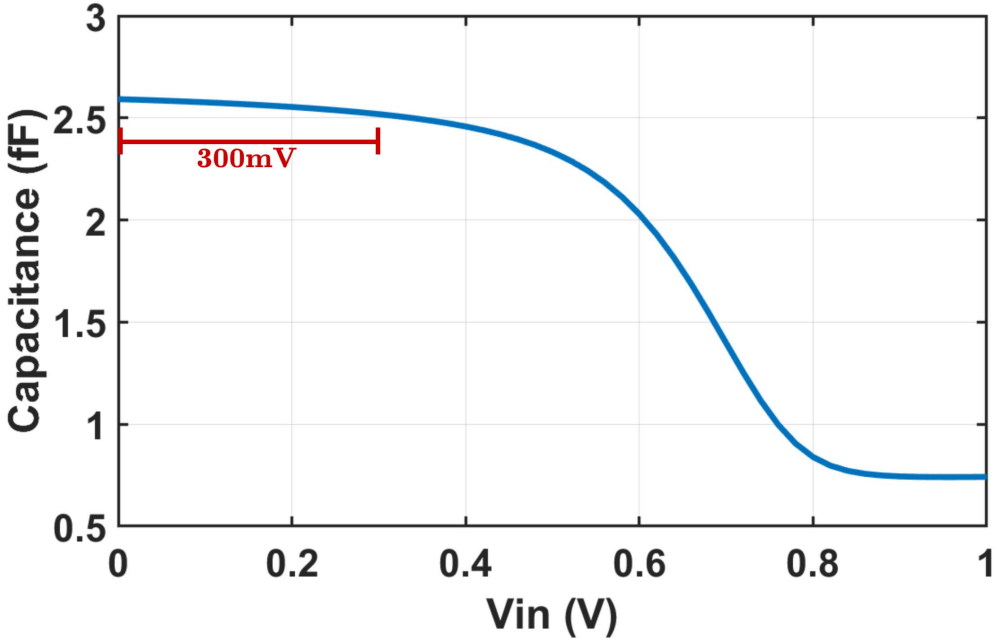
Linearity of MOSCAP

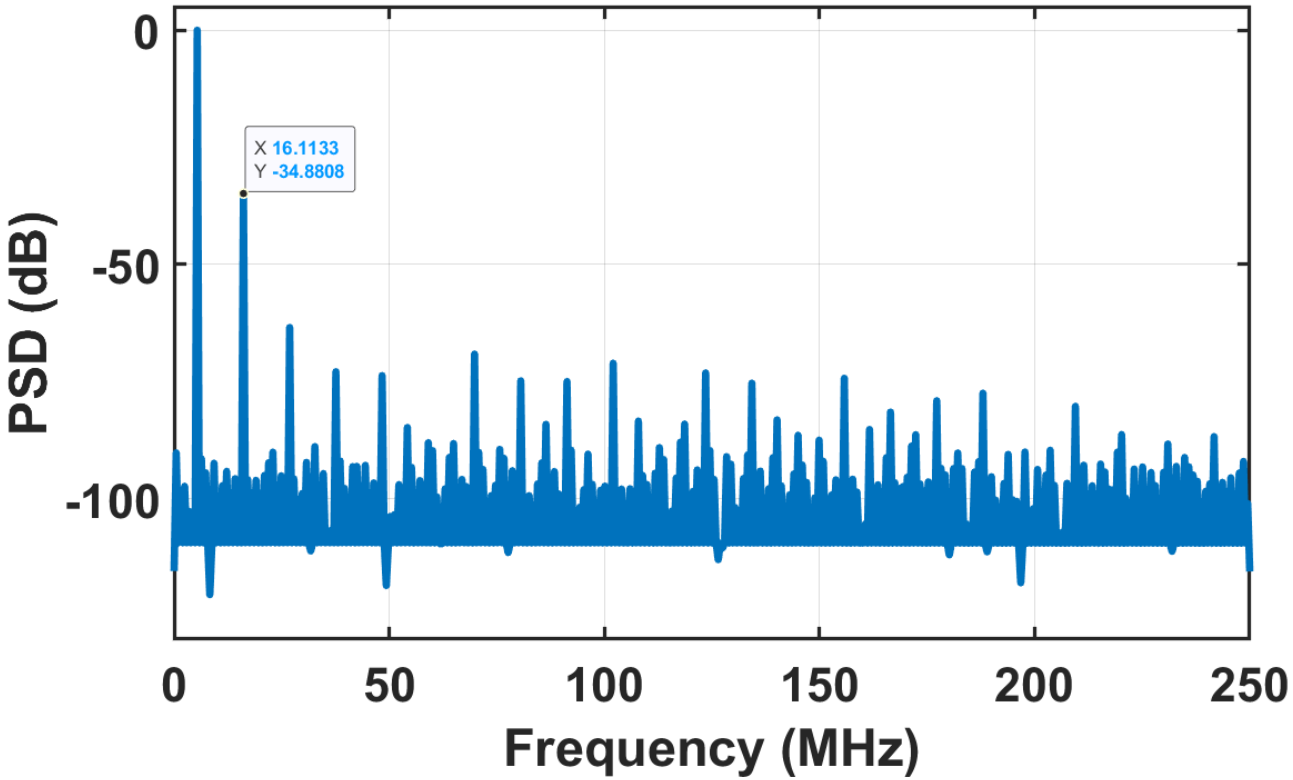




- The capacitance varies by 30 aF (approx. 1.2%) in the input voltage range of 0-0.2 V when V_{CM} = 1 V.
- The variation of the MOSCAP leads to a third harmonic which is 51 dB down during the sampling phase.

Linearity of MOSCAP with V_{in} of 300mVpp





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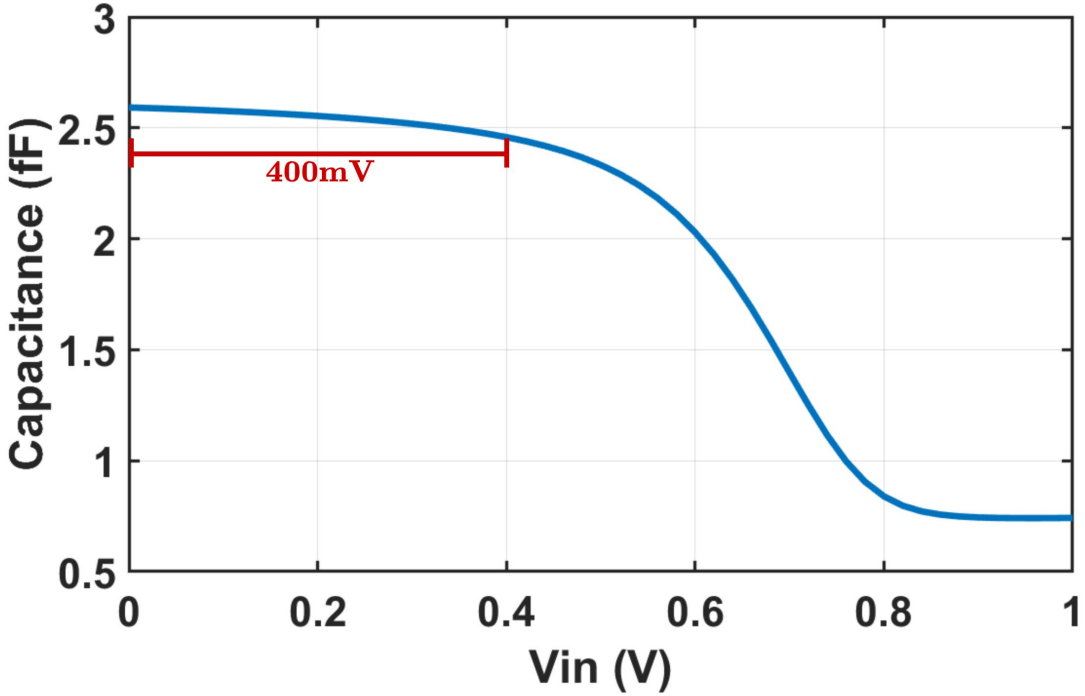
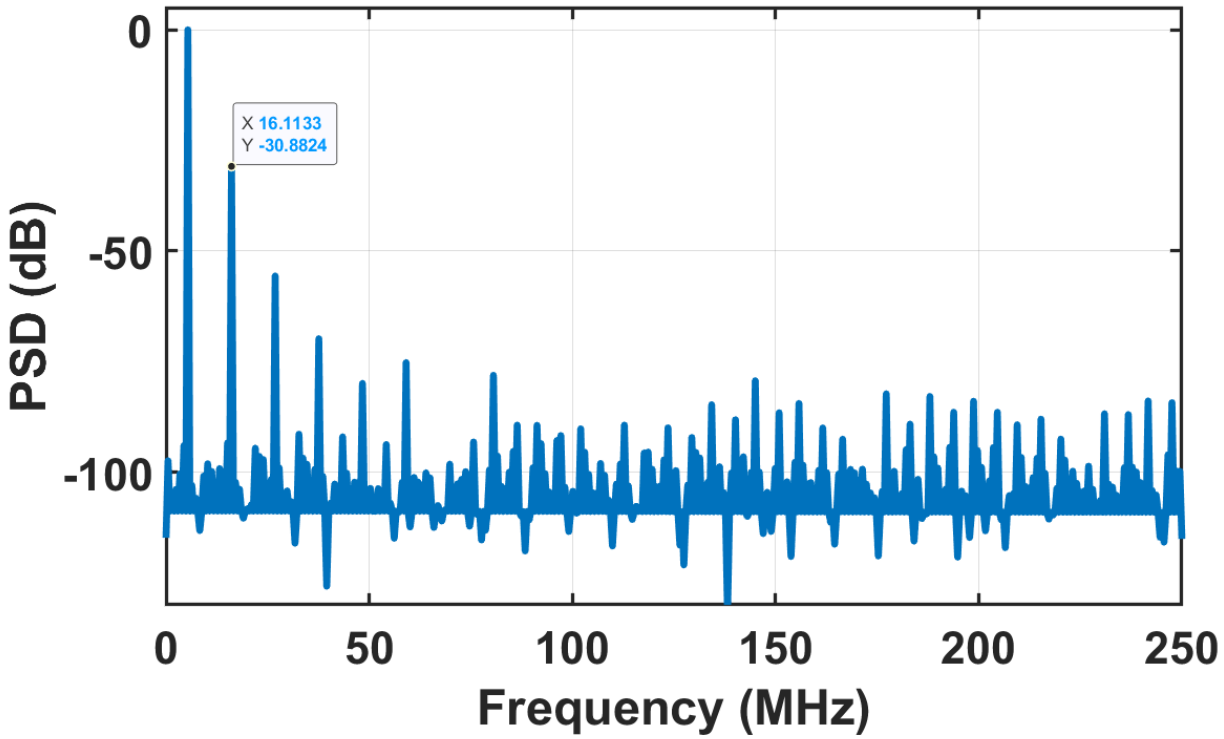
Linearity of MOSCAP with V_{in} of 400mVpp





- As the input voltage is increased, the capacitance works more in the non-linear region and hence a drop in SFDR is observed.

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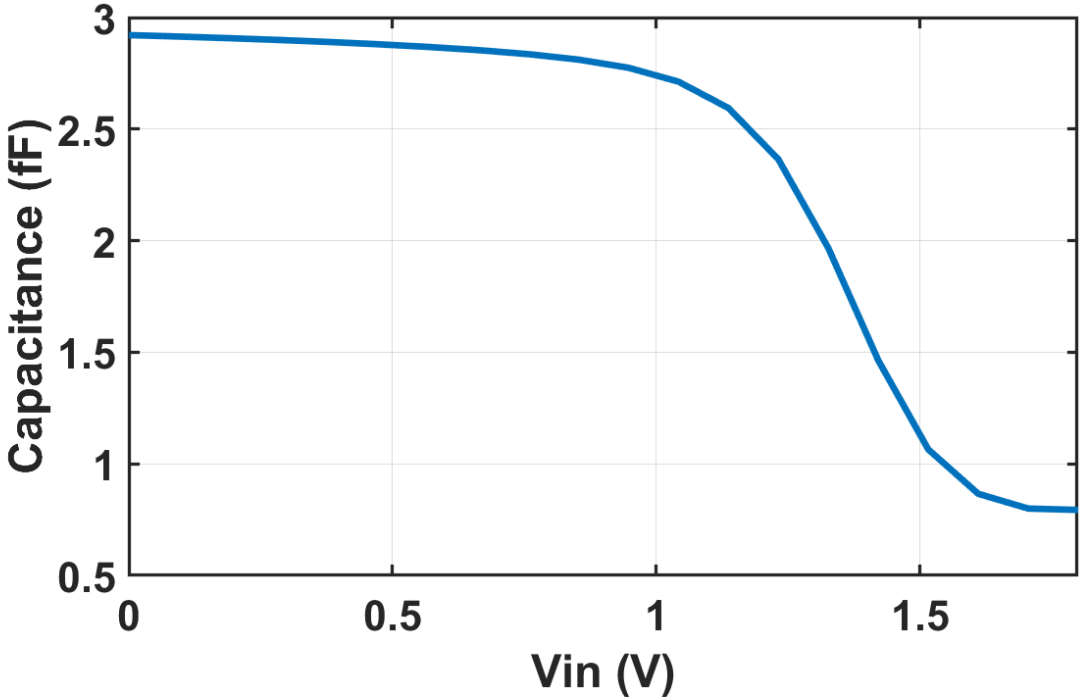
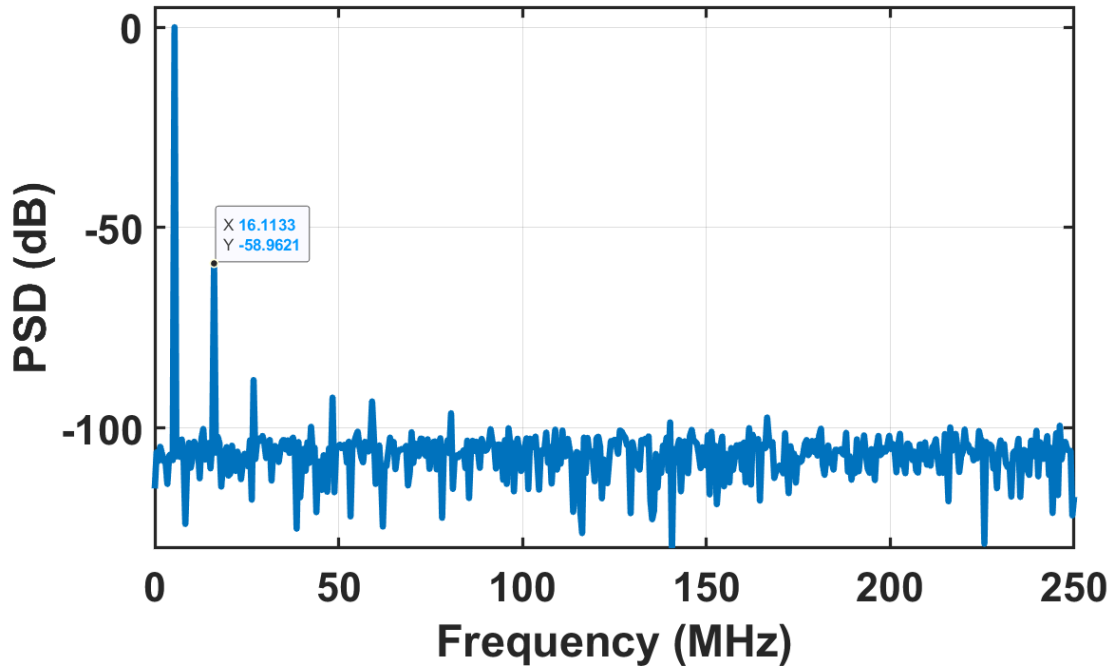
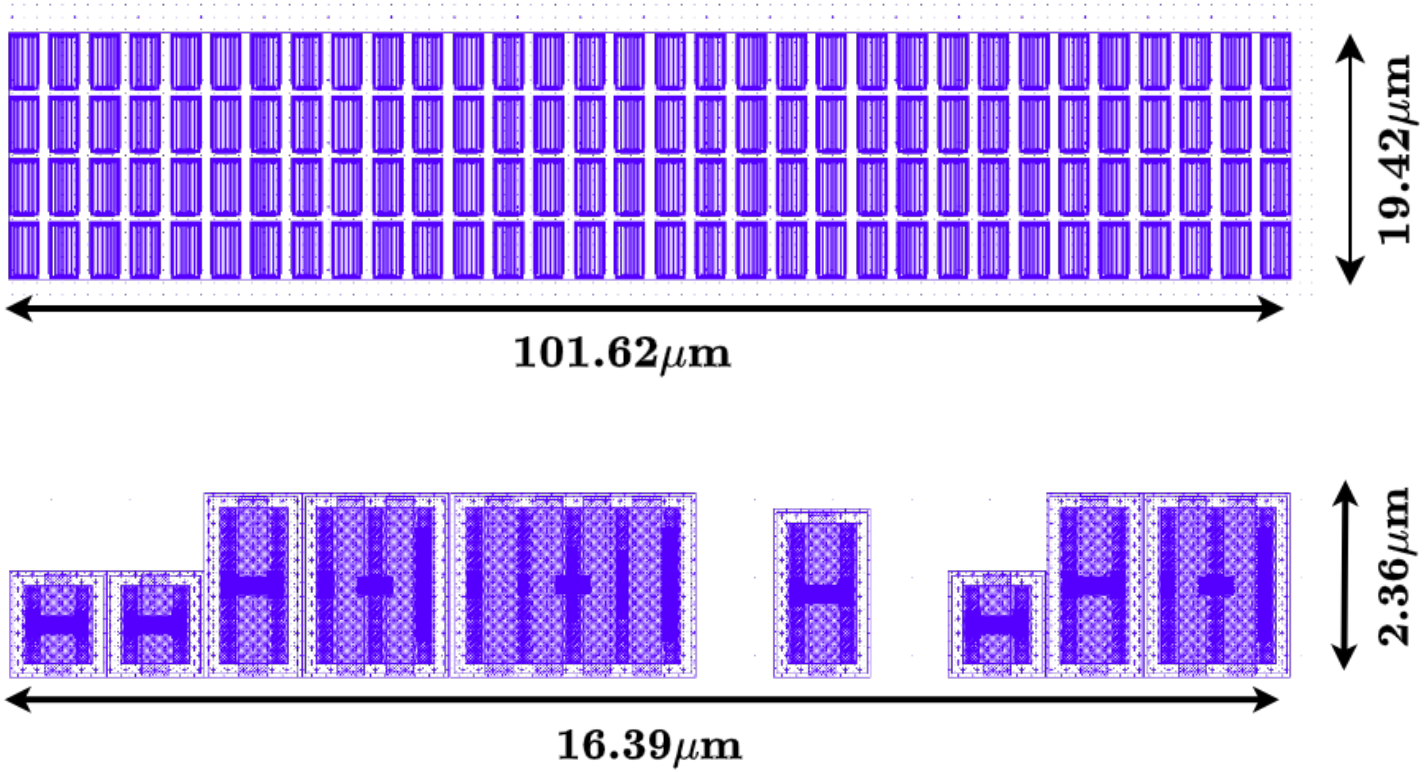
MOSCAP linearity in 130nm





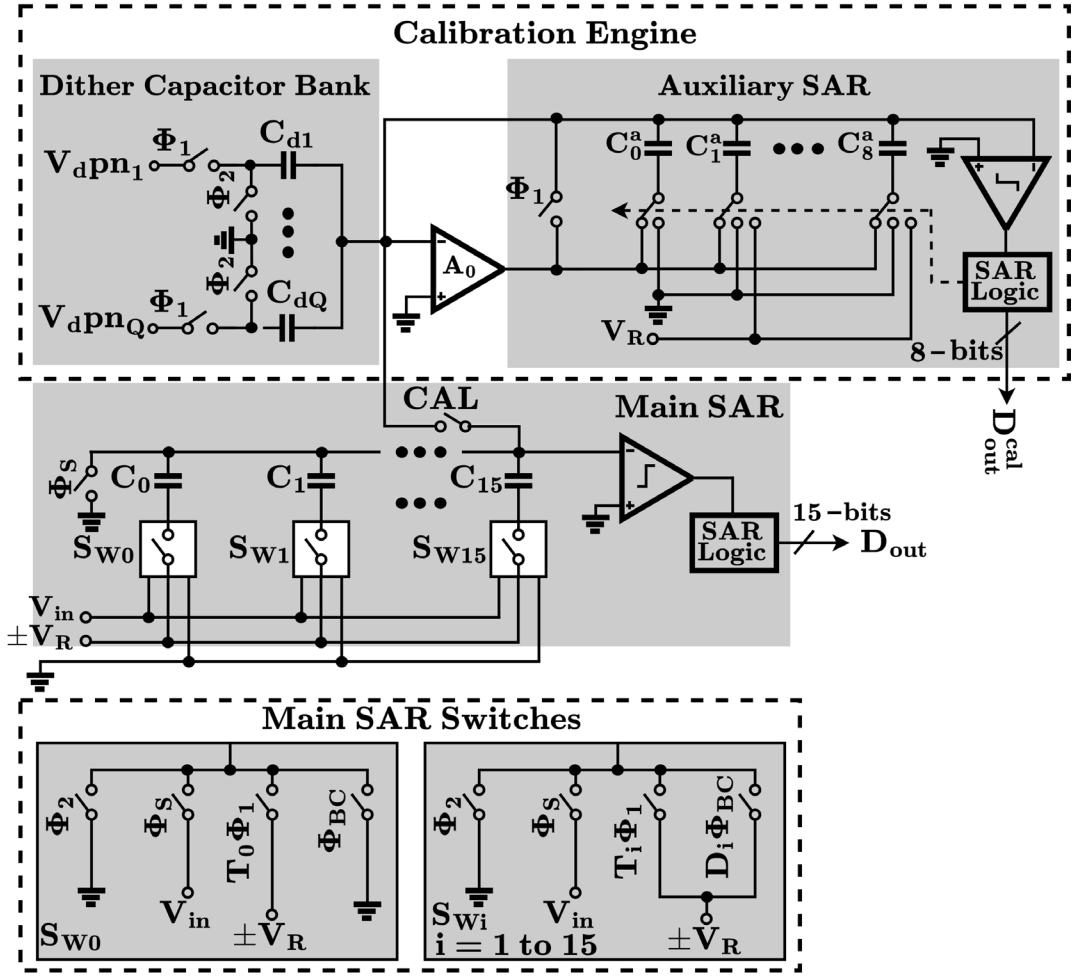
- The capacitance is linear for wider input voltage range.
- The MOSCAP variation leads to non-linearity resulting in a third harmonic of 58 dB down during the sampling phase.

MOMCAP and MOSCAP layout in 130nm



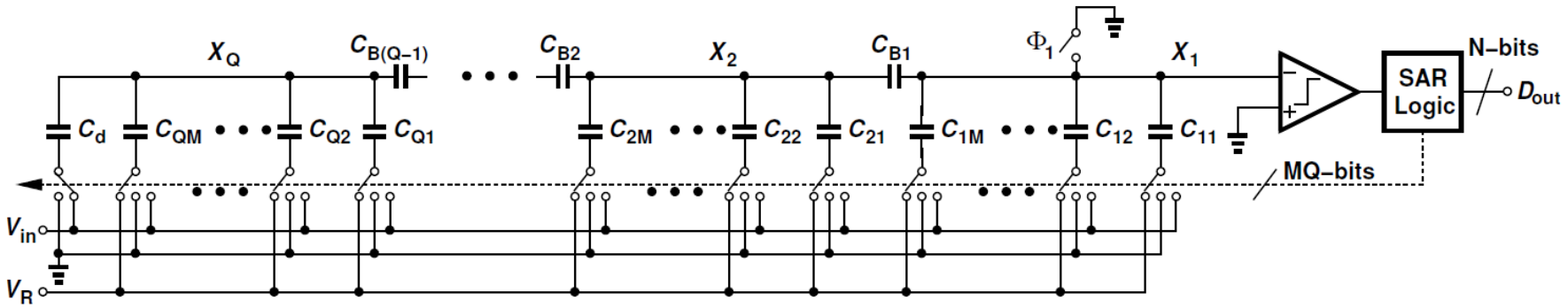
- The MOMCAP provided in 130nm have fixed capacitance values with the minimum capacitance being 4.37 fF.
- All the capacitors in the CDAC occupies an area of 1973 μm^2.

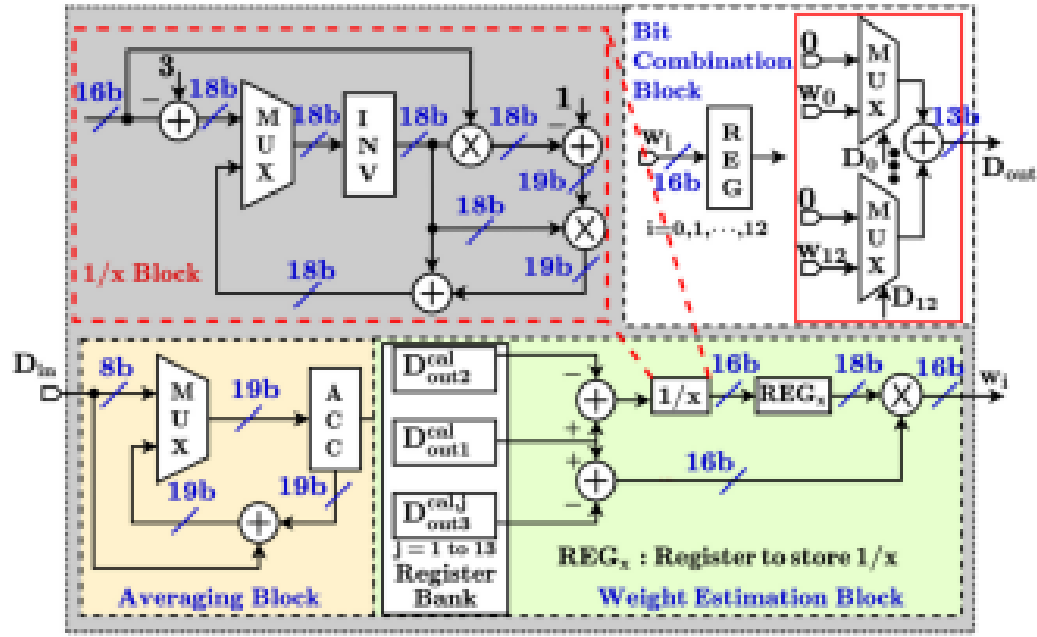
Higher resolution via deterministic dithering



S. Konwar, H. Roy, S. H. W. Chiang, and B. D. Sahoo, "Deterministic Dithering-Based 12-b 8-MS/s SAR ADC in 0.18-µm CMOS," *IEEE Solid-State Circuits Letters,* vol. 5, pp. 243-246, 2022.

Higher resolution via deterministic dithering





S. Konwar, H. Roy, S. H. W. Chiang, and B. D. Sahoo, "Deterministic Dithering-Based 12-b 8-MS/s SAR ADC in 0.18-µm CMOS," *IEEE Solid-State Circuits Letters,* vol. 5, pp. 243-246, 2022.

Higher resolution via noise shaping