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A Wide-Temperature-Range SAR ADC in Open-Source CMOS Technology

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Multi-channel analog-to-digital converters (ADCs) operating over a wide temperature range are required for data acquisition in high-energy physics experiments, space missions, medical imaging, astronomy, and quantum computing. For example, charge readout of the liquid argon (LAr) time projection chambers (TPCs) used by the DUNE far detectors relies on cooled ADCs operating at 89K. Successive approximation register (SAR) ADCs are suitable for such applications due to their highly-digital nature, low analog complexity, and power efficiency. Here we describe an 8-bit SAR ADC in open-source 130 nm CMOS technology designed to operate reliably from 4K-400K at sampling rates up to 10 MS/s.

Summary (500 words)

Typical SAR ADC designs require external reference voltages, bias voltages, and bias currents. Heat transfer through the wires used to provide these inputs can be a major issue for cryogenic experiments. This proposed ADC minimizes the number of external connections, thus making it suitable for operation within small cryogenic chambers. The design was realized in an open-source CMOS technology (Skywater S130) to facilitate sharing and dissemination within the community. Other advantages of the S130 process include rapid, low-cost prototyping (through eFabless) and publicly available cryogenic test data (measured at 4K) via a collaborative effort between Google and NIST.

Fig. 1 shows a top-level overview of the SAR ADC core. The design is fully differential and has a resolution of 8 bits. It uses a conventional capacitive charge-redistribution digital-to-analog converter (DAC), a discrete-time comparator, and SAR logic. A custom "pulse stretcher"circuit is used to generate the sampling clock signals required by the DAC. In addition, a time delay circuit (realized using a chain of inverters) is used to ensure that the voltage across the DAC has had enough time to settle before the comparator makes a decision. The SAR logic is simplified by designing it as a synchronous state machine. A total of 12 clock cycles are used per conversion cycle, resulting in an input clock frequency of 12fs where fs is the ADC sampling rate. The same clock reads out the digitized bits as a serial data stream. The SAR logic also generates an end of conversion (EOC) signal that can be used by an external controller as a frame indicator.

The proposed SAR ADC core was combined with auxiliary circuits to realize a complete and self-contained solution for cryogenic instrumentation. As shown in Fig. 2, the ADC core was aug- mented by 1) on-chip voltage and current references, 2) a sampling pulse generator, and 3) a digital interface for programming all system parameters. The design uses temperature- compensated all-MOS voltage and current references (denoted by VREF and IREF, respectively) to ensure operation over a broad temperature range. The full-scale and common-mode voltage sources used by the capacitive DAC (denoted by VF S and VCM, respectively) are generated on-chip by replica source-follower circuits. The maximum value of VF S is limited by the power supply voltage of VDD = 1.8 V.

Fig. 3 summarizes the simulated dynamic performance of the complete SAR ADC for VF S = 1.5 V, VCM = 0.75 V, and fs = 10 MS/s at 300K. The input was a sinusoid with a frequency of (3/160) x fs = 187.5 kHz and a nearly full-scale peak-to-peak swing of 1.3 Vpp. The output power spectrum was analyzed to extract key dynamic parameters such as 1) signal to noise-and-distortion ratio (SINAD), 2) spurious-free dynamic range (SFDR), and 3) the equivalent number of bits (ENOB). The results in the figure show that the ADC has nearly ideal performance, with an ENOB of 7.7 bits and an SFDR of 55.5 dB.

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