Contribution ID: **134** Type: **Oral**

SOCRATES: a Radiation-Tolerant SoC Generator Framework

Tuesday, 1 October 2024 11:20 (20 minutes)

As front-end ASIC complexity in HEP experiments grows, there is a shift towards more modular, programmable, and cost-effective designs. This work introduces the SOCRATES platform, a radiation-tolerant SoC generator toolset, centered on SoCMake, a hardware/software build system that automates SoC assembly and verification. Utilizing existing IP blocks, SoCMake generates the interconnects and the software framework to run application code. The platform includes radiation-tolerant IPs and supports fault-tolerant extensions for redundancy and error correction. A prototype ASIC based on the RISC-V Ibex processor, created using SOCRATES in a 28nm CMOS process, validates the toolset through SEE and TID testing.

Summary (500 words)

Integrating System-on-Chip (SoC) design techniques can help tame the complexity of ASICs by providing a structured approach to manage and optimize the integration of multiple functions onto a single chip. Such techniques include modular design, standardization of interconnects and IP reuse, hierarchical organization, system-level verification, and a platform-based methodology.

In the domain of High-Energy Physics (HEP) experiments, the complexity of on-detector ASICs is ever increasing to meet the requirements of modern detectors such as pixel detectors with advanced on-pixel functionalities, high pixel count, high data rate transmission and low power consumption.

A SoC design platform could greatly assist the design and support the verification of on-detector ASICs by automatizing the assembly of the components integrating the digital as well as the analog mixed-signal functions. SoCs could also include processing cores, memories, IO peripherals and interfaces to effectively replace state machines in many parts of the designs. Processors would allow for hardware resource sharing within and across applications as well as flexibility to match the need of the target application and programmability throughout the application's life cycle.

In this context, we introduce SOCRATES, a System-On-Chip RAdiation-Tolerant EcoSystem, which provides a complete toolset for the generation of radiation-tolerant System-on-Chip (SoC) designs. The project aims to enable design reusability and modularity by minimizing the amount of manually-written RTL code and promoting the reuse of qualified IP blocks, thus greatly reducing design and verification turnaround time and cost.

At the heart of the SOCRATES platform is SoCMake, a CMake-based build system with custom extensions targeted at hardware/software co-design. Starting from a SystemRDL description, along with the RTL of the CPU core, memories, peripherals, and any other custom logic, SoCMake calls different tools to generate the RTL of the whole SoC, the Hardware Abstraction Layer (HAL) for the peripherals, the linker script for application mapping and the documentation.

Radiation tolerance is provided by extensions that introduce TMR (Triple Modular Redundancy) and ECC (Error-Correcting Code). Each peripheral register block is generated with embedded TMR, the peripheral interconnect bus is automatically instantiated and consists of an AMBA APB protocol extended with ECC (APB-RT).

To validate this toolset and test the radiation performance of the resulting design, a demonstrator chip is being developed in a commercial 28nm bulk CMOS technology, whose architecture is also presented in this work.

This SoC is generated using the SOCRATES platform and it's based around Ibex, an open-source RISC-V processor core. A minimum set of peripherals is included, while maintaining a focus on introducing observability and testability features to evaluate the radiation tolerance of the design under irradiation testing.

Designs generated with the SOCRATES toolset could range from simple microcontrollers to complex many-core systems with dedicated hardware accelerators. Possible applications within the HEP community could range from simple control and monitoring tasks, like calibration and configuration, to performing on-chip complex data processing usually carried out on the back end, possibly providing a very significant speedup while retaining programmability.

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Session Classification: ASIC

Track Classification: ASIC