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Production Testing of the COLUTA ADC ASIC for the ATLAS HL-LHC Liquid Argon Calorimeter Readout

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The COLUTA ASIC is an 8-channel, 15-bit, 40 MSPS, analog-to-digital (ADC) converter designed for the high-luminosity LHC (HL-LHC) upgrade of the Liquid Argon calorimeter readout electronics. The production version of the ADC meets and exceeds the specifications for the analog performance and the HL-LHC radiation tolerance. The production testing will be performed by a custom-designed robotic test setup which will test 80,000 chips required for the upgrade. The chip performance results, and the chip quality information are stored in a local and centralized database. The robotic setup, chip-quality tests, data archival infrastructure, and the production yields will be presented.

Summary (500 words)

To meet new physics challenges and withstand the expected radiation doses at the high-luminosity LHC (HL-LHC), the ATLAS Liquid Argon (LAr) calorimeter readout electronics will be upgraded. The triangular calorimeter signals are amplified and shaped by analog electronics over a dynamic range of 16 bits, with low noise and excellent linearity.
The analog signals, after shaping, are digitized on two overlapping gain scales by a radiation-hard, low-power 40 MHz 15-bit “COLUTA” analog-to-digital converter (ADC).

The COLUTA ADC ASIC is a custom, 8-channel, 15-bit, 40 MSPS, ASIC fabricated in 65 nm CMOS. The ADC architecture couples a 3.5-bit Multiplying-DAC (MDAC) stage to a pipeline Successive Approximation Register (SAR) ADC with an on-chip Digital Data Processing Unit (DDPU) that determines and applies the MDAC and SAR calibration constants and formats the output data. The sample data and frame are continuously output via 640 Mbps serial LVDS to CERN Low Power Gigabit Transceiver (lpGBT) ASICs.

Measurements of the production version of the COLUTA ADC verify the sampling performance above specification of >11.5-bit ENOB at the characteristic frequencies of the LAr signals. The ADC also meets the radiation tolerance requirements for the operation of HL-LHC, as verified by tests conducted in a proton beam facility. A brief overview of the ADC performance and the radiation hardness of the ADC will be presented in this talk.

A robotic, multi-chip test setup has been prepared to test the required 80,000 chips for the LAr upgrade. The performance of each chip is measured using a custom-designed test board with identical analog inputs to measure uniformly the performance of each ADC channel. To ensure optimal performance for each chip, a collection of analog measurements is performed. The custom-designed robotic setup is designed to test 80,000 chips at an average rate of 5 min/chip. The chip performance results, and the chip quality information are stored in a local and centralized database. The robotic setup, chip-quality tests, and the data archival infrastructure will be presented in this talk. Besides chip-performance tests, radiation tolerance tests for randomly selected chips from various production lots will also be discussed. Results from robotic chip-testing of the production lots will be presented, along with the yields of the chips which meet the specifications for the upgrade.

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