Reusable Verification Components for High-Energy Physics readout ASICs

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Introduction

ASICs for detector readout developed by High-Energy Physics (HEP) community can be divided into two main categories: front-end (FE) readout and concentrator ASICs.
FE readout ASICs are responsible for receiving analog signals from a sensor, converting them into digital signals, and transmitting the resulting values outside of the ASIC. Typically, a FE readout ASIC includes multiple readout channels, as well as a data transport layer that combines the data from all active readout channels and sends it to the detector readout. Each readout channel is a mixed signal circuit. The digital module carries out functions such as filtering, data compression, and transmission of the resultant values. FE readout ASICs perform similar functions with minor variations to meet detector requirements.
Concentrator ASICs are responsible for receiving data from multiple FE readout ASICs, processing them, and sending them out on one or more high-speed serial interfaces. The data processing includes alignment, error detection, zero-suppression, data compression, and reordering.
Functional verification of these ASICs is fundamental to implement shift-left strategies to achieve first-time-silicon-success. Given the similarities between HEP ASICs, it can be beneficial to re-use verification components avoiding duplication of work. This contribution describes a set of re-usable verification components, developed at CERN under the CHIPS initiative, that allow bringing up a verification environment in hours instead of weeks.

Universal Verification Methodology

The Universal Verification Methodology (UVM) is, *de facto*, the industry standard for functional verification. Developed in the beginning of the 2010s, it is now an IEEE standard [1] since 2020.
UVM defines a set of base classes which allow building a comprehensive, re-usable, and scalable verification environment. It provides a standardised framework for developing a testbench which leverages advanced verification techniques.

- **Constrained-random stimuli generation:** the stimuli driving the design are not predetermined but they are instead randomised, inside a pool of valid stimuli.
- **Functional coverage analysis:** one of the big questions of verification is "When are we done verifying?". The answer to this question lies in the functional coverage. The designer of the testbench can define functional covergroups and coverpoints. The verification environment then allows gathering coverage from a set of tests to understand when all the predefined scenarios have been observed.
- **Reusable testbench components:** UVM encourages the design of hierarchical and reusable components. Reusability introduces overhead in early stages but saves time on the long run.

UVM is widely supported by the major EDA tools. In recent years, support is also being added to open source simulators.
In this contribution we focus on the description of reusable UVM verification components (UVCs).

UVM verification components

PIN UVC

- **Use cases:**
  - Control the reset of the DUT
  - Control and monitor GPIOs of DUT
- **User inputs (configuration):**
  - number of pins to control
  - start-up value of pin
  - synchronous or asynchronous assertion and de-assertion
- **Sequences:**
  - toggle the signal
  - generate a single pulse
- **Randomisable parameters:** duration, pulse high or low time

Clock UVC

- **Use cases:**
  - Generate clocks to DUTs or UVCs
- **User inputs (configuration):**
  - Period of fastest clock
  - Ratio between periods of slowest and fastest clock (integer)
- **Sequences:**
  - Generate any integer multiple of fastest clock period
  - Generate clock w/ and w/o jitter
- **Randomisable parameters:** ratio w.r.t. fastest clock, max jitter, phase

I2C UVC

- **Use cases:**
  - Configure the DUT in top- and system-level testbenches
  - Integrate with UVM Register Access Layer (RAL)
  - Provides an abstraction layer for the CERN VIP or Questa VIP (QVIP) ($\rightarrow$ license required)
- **User inputs (configuration):**
  - Simple or QVIP mode
  - Device ID for Design Under Test (DUT)
  - ADDRLEN/DATLEN
  - Repeated start or stop $\rightarrow$ start on read
- **Sequences:**
  - Run any I2C sequence on the I2C bus
  - Use the RAL to access the DUT via UVM FRONTDOOR
- **Randomisable parameters:** device ID, address, data, access

Wishbone UVC

- **Use cases:**
  - Configure the DUT in module-level test
  - Verify Wishbone master operations
  - Integrate with UVM RAL
- **User inputs (configuration):**
  - Master/slave behaviour
  - ADDRLEN/DATLEN
- **Sequences:**
  - Run any Wishbone sequence on the Wishbone bus
  - Use the RAL to access the DUT via UVM FRONTDOOR
- **Randomisable parameters:** address, data, access

Hit UVC

- **Use cases:**
  - Provide methodology for injection of particle hits in FE readout chips
  - Verify FE readout chip
- **User inputs:**
  - Integration effort
  - Matrix dimensions (x-size, y-size)
- **Sequences:**
  - Read from file
  - Random hits
- **Randomisable parameters:** location (x,y), charge, time to next hit

SEE UVC

- **Use cases:**
  - Provide methodology for injection of SEEs
  - Explore design susceptibility to SEEs
  - Verify design operation in SEE environment
- **User inputs:**
  - Integration scripts
  - List of fault-able nodes
  - Filtering strategy
- **Sequences:**
  - Start injection
  - Stop injection
  - Re-start injection
- **Randomisable parameters:** fault type (SET, SEU, SEE), node, duration

Example of testbench

In order to demostrate how to bring up a testbench using the CERN CHIPS UVCs, a sample DUT is introduced.

The DUT:

- Emulates a 4-channels FE ASIC with Time of Arrival (TOA) and Time over Threshold (TOT) measurement of the input signal *event_i*.
- Is clocked with a slow (40 MHz) and fast (320 MHz) clocks.
- Is reset by two signals: an asynchronous hard reset (resetting the whole DUT) and a 40 MHz-synchronous soft reset (not affecting the configuration registers).
- Is configured using the I2C protocol [2].
- The chip address is configured by four dedicated pins, that need to be stable over the operation of the DUT.

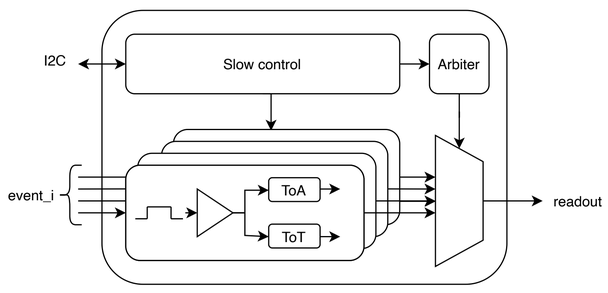

Figure 1: Example DUT: event recorder

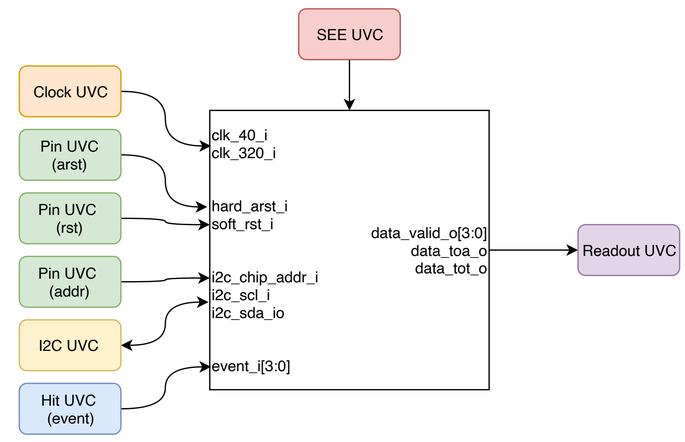

Figure 2: Example of testbench with the UVCs connected

HEP ASICs using the UVCs

The CHIPs UVCs have been successfully used in the verification of multiple ASICs:

- ATLAS HGTD ALTIROC
- ATLAS/CMS RD53
- CMS HGCAL ECOND and ECONT
- EXP28

Moreover the UVCs are currently being used in the verification of the following ASICs:

- ALICE ITS MOSAIX
- LHCb RICH Fastrich
- LHCb VELO Picopix

References

[1] IEEE Standard for Universal Verification Methodology Language Reference Manual. *IEEE Std 1800.2-2020 (Revision of IEEE Std 1800.2-2017)*, pages 1–458, 2020.
[2] I2C-bus specification and user manual, rev 7.0. http://www.nxp.com/docs/en/user-guide/UM10204.pdf. Accessed: 2024-09-23.

EP-ESE ELECTRONIC SYSTEMS FOR EXPERIMENTS

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