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Reusable Verification Components for High-Energy Physics readout ASICs

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Verification is a critical aspect of designing Front-end (FE) readout ASICs for High-Energy Physics (HEP) experiments. These ASICs share several similar functional features, resulting in similar verification objectives, which can be addressed using comparable verification strategies. This contribution presents a set of re-usable verification components for addressing common verification tasks, such as clock generation, reset handling, configuration, as well as hit and fault injections. The components were developed as part of the CHIPS initiative and they have been successfully used in the verification of multiple HEP ASICs.

Summary (500 words)

ASICs for detector readout developed by HEP community can be divided into two main categories: FE readout and concentrator ASICs.
FE readout ASICs are responsible for receiving analog signals from a sensor, converting them into digital signals, and transmitting the resulting values outside of the ASIC. Typically, a FE readout ASIC includes multiple readout channels, as well as a data transport layer that combines the data from all active readout channels and sends it to the detector readout. Each readout channel is a mixed signal circuit. The digital module carries out functions such as filtering, data compression, and transmission of the resultant values. FE readout ASICs perform similar functions with minor variations to meet detector requirements.
Concentrator ASICs are responsible for receiving data from multiple FE readout ASICs on high-speed interfaces, processing them and sending them out on one or more high-speed serial interfaces. The data processing includes alignment, error detection, zero-suppression, data compression, and re-ordering.

Universal Verification Methodology (UVM) is \emph{de facto} the industry standard for functional verification of complex ASICs. It allows implementation of coverage-driven constrained-random verification. UVM is leveraging object-oriented programming techniques to allow re-use of verification components.

In the framework of the CHIPS initiative multiple UVM Verification Components (UVCs) were developed. This contribution will present the functionalities of the different verification components and show how they can be used to bring-up a test bench in hours, instead of days. The components available are:
\begin{itemize}
\item Clock UVC: allows generating a set of synchronous clocks from a base (fast) clock through frequency division. The clocks have a randomizable period, phase and jitter.
\item Pin UVC: allows steering a Design Under Test (DUT) pin or General Purpose Input/Output (GPIO) bus, e.g. for controlling a reset or an I2C address bus. The sequences provided allow controlling the pins both asynchronously or synchronously to a given clock.
\item Wishbone UVC: allows controlling a Wishbone bus emulating a Wishbone master. It provided hooks to bind it to the UVM Register Access Layer (RAL) for controlling the DUT configuration.
\item I2C UVC: allows controlling an I2C bus emulating a controller on the interface. It provides hooks to bind it to the UVM RAL. The UVC also provides a level of encapsulation for a major EDA vendor I2C UVC making its use transparent to the user.
\item Hit UVC: allows controlling the injection of charges or hits into a matrix of readout channels emulating the effect of particles impinging into the detector sensitive area.
\item Single Event Effects (SEE) UVC: provides a framework for injecting Single Event Upsets (SEUs) and Single Event Transients (SET) into the DUT while operating it. The UVC sequences are designed to be randomly

stable.
\end{itemize}

The UVCs have been successfully used in multiple ASICs verification such as: lpGBT, ALTIROC, ECON-D, ECON-T, Medipix4, MOSS, and RD53.
The UVCs described are available on the CERN CHIPS GitLab page.

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