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High-Speed Data Transmission IP's in 65nm CMOS Image Sensor Process at the Electron Ion Collider

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Next generation particle physics experiments like Electron Ion Collider (EIC) demand high-speed data communication and lower mass designs for its detectors.
This poster presents initial test results for circuits designed to meet the EIC high-speed data requirements. These include a dual-frequency Phase Locked Loop (PLL) that supports two frequency modes of operation, a 5 GHz Pseudo-Random Bit Sequence (PRBS) Generator for system testing, an I2C block and a high speed CML receiver.

Summary (500 words)

Next generation particle physics experiments like Electron Ion Collider (EIC) demand high-speed data communication and lower mass designs for its detectors. Thanks to the availability of smaller technologies and innovative designs techniques, novel scientific detectors will be based on high speed and energy efficient sensor systems.
This poster presents initial test results for circuits designed to meet the EIC high-speed data requirements. These include a dual-frequency Phase Locked Loop (PLL) that supports two frequency modes of operation, a 5 GHz Pseudo-Random Bit Sequence (PRBS) Generator for system testing, an I2C block and a high speed CML receiver.
The PLL has two frequency ranges, 800 MHz to 2 GHz and 5.5 to 7 GHz. The output of the PLL can be used to clock a PRBS generator. The PRBS generator uses a 16-bit Galois linear feedback shift register, set up for maximal length before it repeats. The register is tapped two places, the two taps are passed through a buffer which aligns them to be 180 degrees out of phase, and then they are combined in a XOR gate which doubles the data rate of each stream. This allows the PRBS generator to produce a 10 Gbit/s output with the PLL and shift register clocking at 5 GHz.
The Common-mode Logic (CML) receiver consists of a Continuous Time Linear Equaliser (CTLE, filter) followed by a CML to CMOS converter and then a CML output driver. This allows the block to be tested regenerating CML signals. The CTLE attenuates low-frequency signal components, amplifies components around the Nyquist frequency and filters off higher frequencies to compensate for transmission path loss without boosting noise.
The I2C block is a test instance of a soft macro which provides a configurable number of 8-bit registers which can be programmed and read back over the I2C bus. Each I2C address provides one inbound register which can be written to over the I2C bus. Each inbound register is triplicated, with triple-majority voting and data scrubbing so that single bit flips in one voter are corrected so errors do not accumulate. Each address can also allow 8 bits of on-chip signals to be read out over I2C.
In this test chip the I2C block was configured to provide 3 inbound and 3 outbound registers. Two of the 3 connect the inbound register to the outbound register to allow the software to read back the data to check that it has been written and stored correctly.
This paper will present initial test results for each block of the test chip before irradiation and after 10 MRads of irradiation.
The PLL has been tested in both speed modes over a range of input clock frequencies, with varying power

supply voltages. Similarly, the CTLE receiver has been tested with clock and PRBS data patterns at a range of bit rates, again with varying power supply voltages. The write and read back of data over the I2C bus has been tested.

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