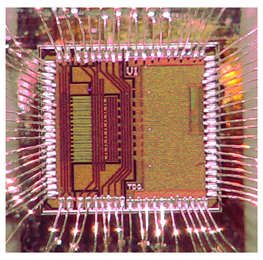
Development of the Time-to-Digital Converter in 130 nm CMOS technology

Mirosław Firlej (firlej@agh.edu.pl), Tomasz Fiutowski, Marek Idzik, Aleksandra Molenda, Jakub Moroń, Krzysztof Świentek

AGH University of Krakow, Faculty of Physics and Applied Computer Science, Krakow, Poland

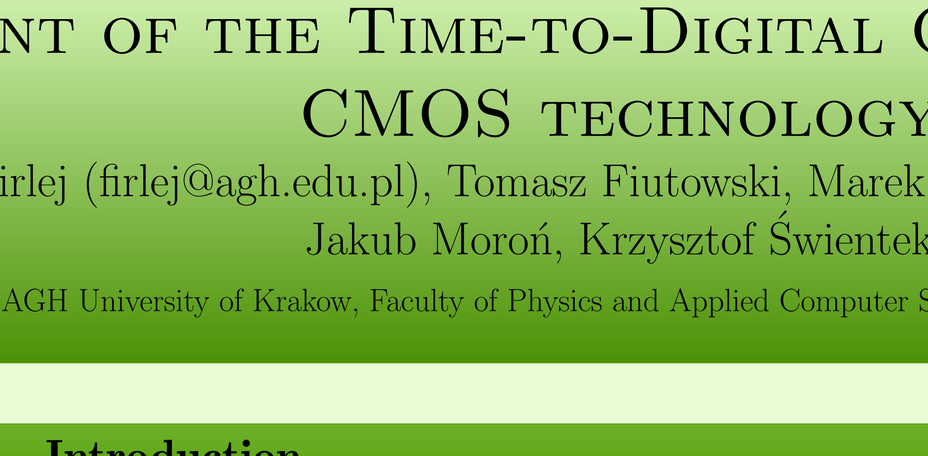
Introduction

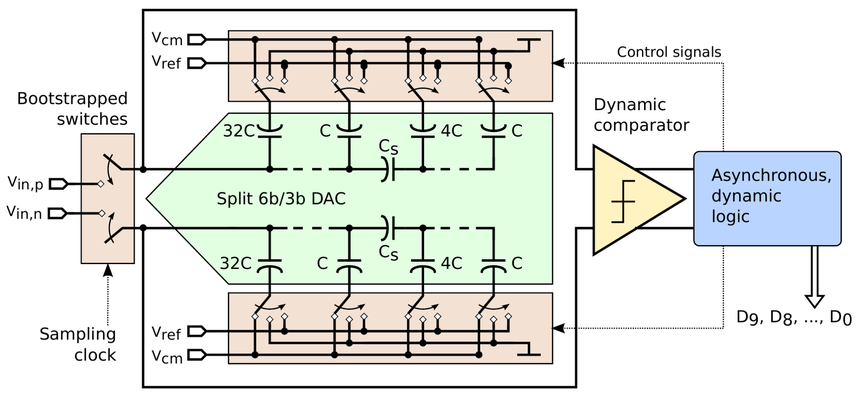


A TDC prototype was designed and fabricated in CMOS 130 nm technology. The architecture with analog interpolators was chosen, which was motivated by previous experience in SAR ADC design in 130nm CMOS technology[1]. The measured time difference between the event and the trigger signal is converted to the amplitude and then digitised by a 10-bit ADC. The circuit has configurable time resolution from 15 ps to 140 ps, which gives the total possible time measure range from ±9.5 ns to ±70 ns.

Architecture

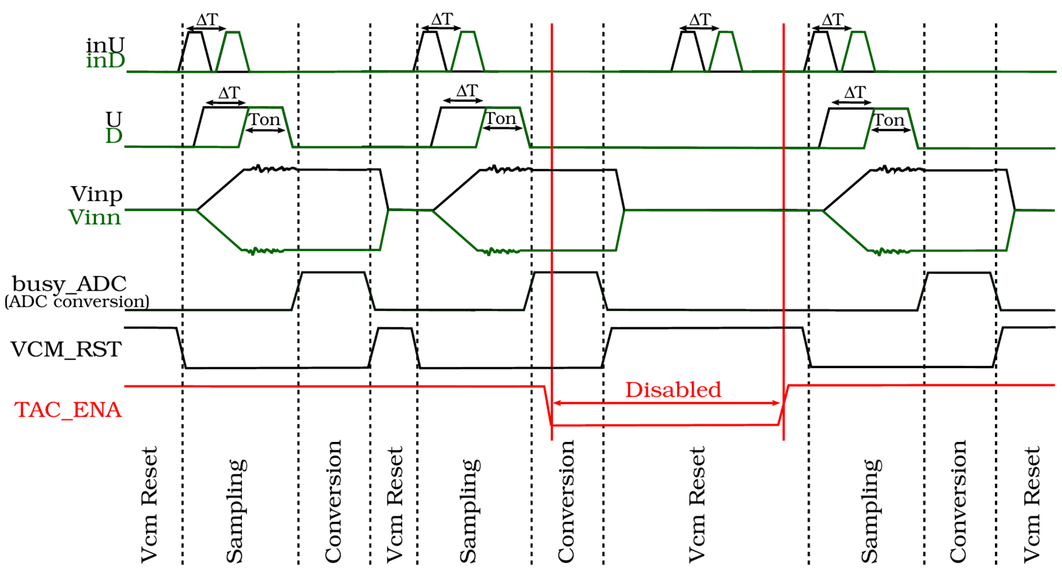
The TDC contains a Time to Analog Converter (TAC) with two current mirror branches, digitally controlled by Phase and Frequency Detector (PFD). The PFD detects the time difference between the input signals InU and InD, no matter which comes first, which allows to measure positive and negative (before trigger) time values. Thanks to internal current DACs, the bias of the Charge Pump (CP) can be digitally configured, changing the time resolution from 15 ps to 140 ps (LSB). As the last stage a fully differential SAR ADC is used to digitise analogue value.





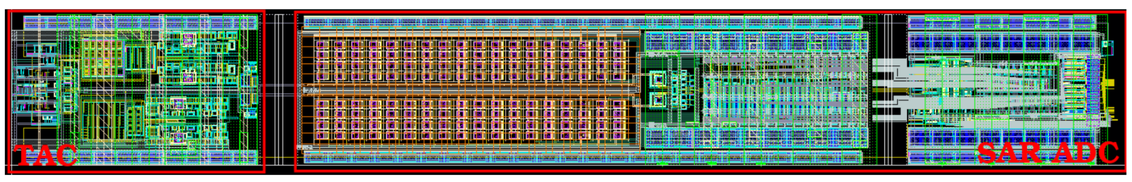
For the 10-bit SAR ADC implementation a differential capacitive DAC, a dynamic comparator, and an asynchronous dynamic control logic were chosen. The asynchronous ADC logic eliminates a fast bit-cycling clock distribution during conversion and a fully dynamic logic is used to eliminate the static power consumption. To reduce total ADC capacitance the minimal capacitor size together with a split DAC architecture were chosen.

The rising edges of the inU (start) and inD (stop) signals generate the U and D signals. The time difference between them is proportional to the voltage build the internal ADC capacitance (Vinp and Vinn). When the ADC input voltage becomes stable the conversion starts. When the ADC conversion finishes, it is reset to be ready for the next conversion.

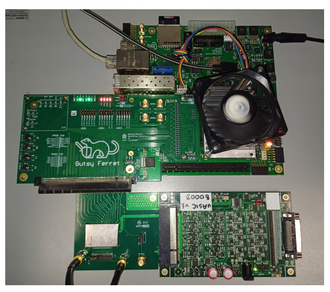


Layout

The layout of TDC was drawn in 100 um pitch and the length of around 740 um. This was done for future implementation of TDC in a multi-channel ASIC.



Measurements Setup



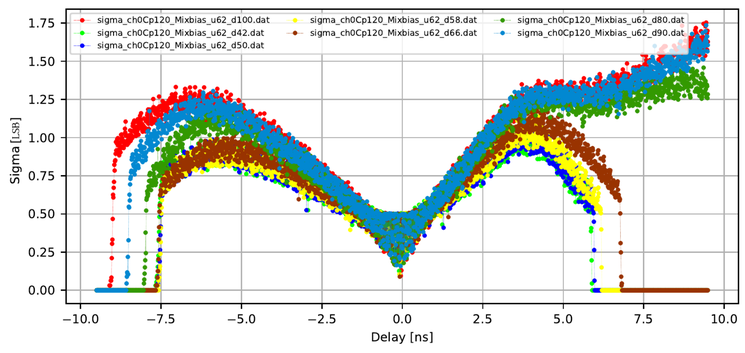
A dedicated setup was developed to measure main TDC parameters. It comprises following components:

- Function Generator Agilent 81160A for input signals,
- Trenz FPGA Board as DAQ system,
- Dedicated test boards: Gutsy Ferret Board (Gutsy Ferret) and uASIC Board,
- Dedicated TDC Board with ASIC,
- Client PC for data collecting and analysing.

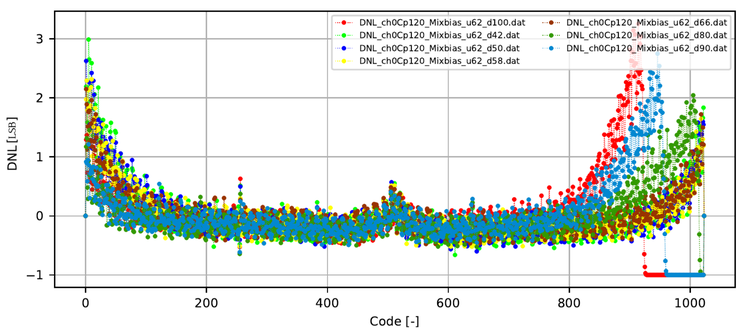
References

[1] M. Firlej, T. Fiutowski, M. Idzik, S. Kulis, J. Moroń, K. Świentek, *An ultra-low power 10-bit, 50 MSps SAR ADC for multi-channel readout ASICs*, Journal of Instrumentation, Vol.18, Num.11, P11013, Nov 2023

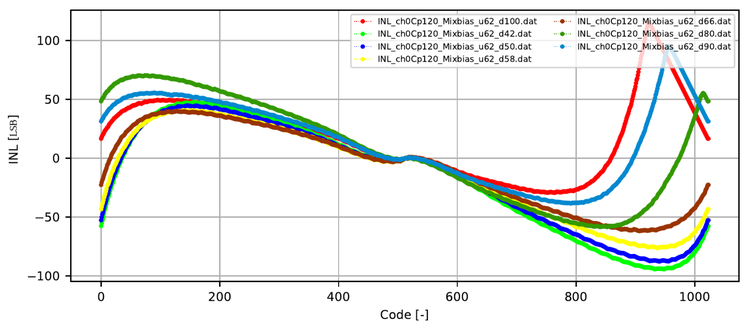
Preliminary Results



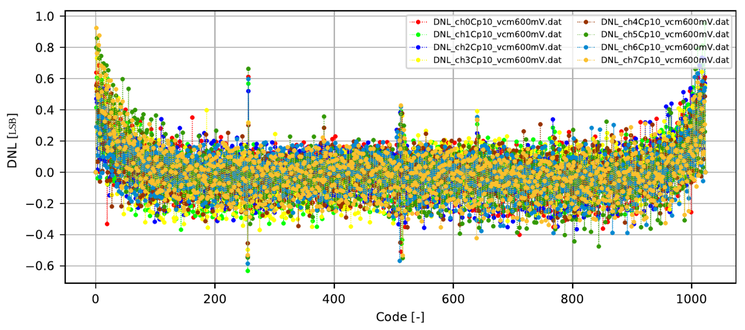
The Jitter (sigma) at best resolution (15 ps) is around 1 LSB and depends on the measured time



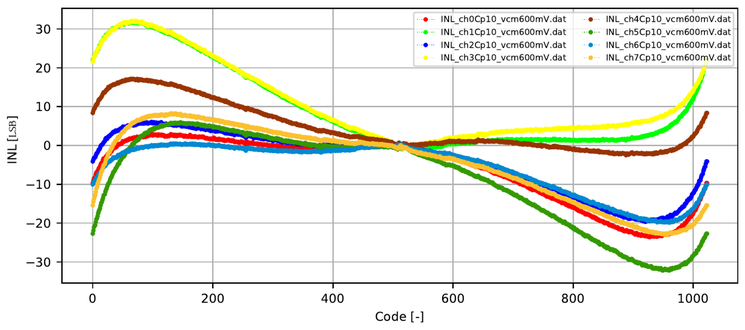
The DNL at best resolution (15 ps) is below 1 LSB in most of the measured range



The INL to be studied - results much worse than simulated



The DNLs for all channels in prototype ASIC look very similar



The INLs for all channels show slightly different behaviour

Summary

The architecture and preliminary results of prototype TDC, comprising a TAC and 10-bit ADC were shown.

- First tests confirm expected TDC functionality,
- The configurable time resolution from 15 ps to 140 ps gives the total possible time measure range from ±9.5 ns to ±70 ns,
- The prototype TDC achieves a good DNL around 1 LSB,
- The INL is significantly worse than simulated of the order of 10-15 LSB (need further studies),
- The measured jitter is below 1 LSB,

Acknowledgments

This work has received funding from the Polish Ministry of Science and Higher Education under contract No 5179/H2020/2021/2, and from the European Union's Horizon 2020 Research and Innovation programme under grant agreement No 101004761 (AIDAinnova).