Contribution ID: **40** Type: **Poster**

Development of the Time-to-Digital Converter in 130 nm CMOS technology

Tuesday 1 October 2024 17:40 (20 minutes)

The design and measurement results of a prototype TDC fabricated in CMOS 130nm technology are presented. The TDC architecture with analog interpolators was chosen, which was motivated by previous experience in ADC design. The measured time difference between the event and the trigger signal is converted to the amplitude and then digitised by a 10-bit ADC. The TDC prototype is functional nad achieve good DNL and jitter (below 1LSB), slightly dependent of the selected time precision. The circuit has configurable time resolution from 15ps to 140ps, which gives the total possible time measure range from ±9.5ns to ±70ns.

Summary (500 words)

Nowadays in the field of detectors for particle physics experiments, in addition to information about a particle's passage and the amplitude of its signal (measured by ADC), precise time information provided by Time-to-Digital Converter (TDC) is very often required. Both amplitude and time measurements are needed to build complex multi-channel readout ASIC. This work presents the development of the TDC using Time-to-Analog Converter (TAC) and 10-bit Successive Approximation Register(SAR) ADC for digitization. In such a solution one readout channel can be equipped with amplitude and time information, meeting the requirements of modern multi-channel readout ASICs.

The TDC consists of TAC with two current mirror branches, digitally enabled/disabled by Phase and Frequency Detector (PFD), and a fully differential 10-bit SAR ADC. It allows to measure possitive and negative (before trigger) time values. The time resolution can be digitally configured from 15˜ps to 140˜ps (LSB) thanks to internal configurable current DACs. For the ADC implementation a differential capacitive DAC, a dynamic comparator, and an asynchronous dynamic control logic was chosen. The asynchronous ADC logic eliminates a fast bit-cycling clock distribution during conversion and a fully dynamic logic (also in PFD) is used to eliminate the static power consumption. To reduce total ADC capacitance the minimal capacitor size together with a split DAC architecture was chosen.
The layout of TDC was drawn in 100˜um pitch and the length was around 740˜um. This was done for future implementation of TDC in a multi-channel readout ASIC.

The prototype TDC was fabricated in CMOS 130˜nm technology. A dedicated setup was developed to measure important TDC parameters. First tests confirm expected TDC functionality. Detailed parameter's tests are in progress. First results show that the prototype TDC achieves a good DNL around 1˜LSB, while the INL is significantly worse than simulated of the order of 10-15˜LSB (need further studies). The measured jitter is below 1˜LSB. Power consumption still needs to be measured, but post layout simulations give around 1.2˜mW at 20˜MHz rate.

In this presentation the architecture of the developed TDC will be described, comprising the implementation of the TAC and 10-bit ADC. The complete set of measurements of the prototype TDC, showing its linearity and timing resolution will be also presented.

Authors: MORON, Jakub (AGH University of Krakow (PL)); SWIENTEK, Krzysztof Piotr (AGH University of Krakow (PL)); IDZIK, Marek (AGH University of Krakow (PL)); FIRLEJ, Miroslaw (AGH University of Krakow

(PL)); FIUTOWSKI, Tomasz Andrzej (AGH University of Krakow (PL))

Presenters: IDZIK, Marek (AGH University of Krakow (PL)); FIRLEJ, Miroslaw (AGH University of Krakow (PL))

Session Classification: Tuesday posters session

Track Classification: ASIC