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PLL and TDC in TSMC 65nm for FastIC+ Chip

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A phase locked loop (PLL) and a time to digital converter (TDC) have been developed for the FastIC+ chip, an 8-channel ASIC to readout fast timing detectors. The chip is designed to work with sensors such as multi-anode photo multipliers (MAPMTs), microchannel plates (MCPs), silicon photomultipliers (SiPMs), among others. The PLL generates the clock reference for the whole chip, including a high-speed serializer and the TDC. The voltage controlled oscillator (VCO) provides 16 phases at 1.28 GHz . The TDC channels sample the phases of the VCO to obtain their LSBs, while their MSBs are obtained from the frequency divider.

Summary (500 words)

The analog front-end of the FastIC corresponds exactly to FastIC chip [1]. This front-end was conceived to readout sensors with intrinsic gain, like MAPMTs, MCPs, SiPMs, and provide digitized time information. The chip is designed in TSMC 65nm technology and has 8 channels with positive or negative polarity front-ends, including a leading edge discriminator (LED); a radiation-hard PLL and a TDC to digitize the time-of-arrival (TOA) and time-over-threshold (TOT) of the detected particles. This general purpose readout chip is attractive for fast timing and time of flight applications, such as positron emission tomography and high energy physics, mass spectrometry imaging, to name a few. This work presents the PLL and TDC architectures, experimental results will be presented.

The PLL is composed of a phase and frequency detector (PFD), a charge pump, a VCO and a synchronous frequency divider. The VCO is made of 16 Meander differential cells [2] oscillating at 1.28 GHz , providing a 24ps time bin for the TDC. From these phases, the 5LSBs for the TDC are derived, while the frequency divider provides the remaining 5MSBs. The PFD and frequency divider have been hardened against single event upset (SEU) using triple modular redundancy generator (TMRG) tool [3]. However, the charge pump and the VCO remain unhardened, therefore, in case of a single event transient in these blocks, the PLL will undergo unlocked for some microseconds and a flag will be raised. PSS+Pnoise simulation results shows a $\sigma_{\text{PLL}} < 5\text{ ps}$ when the phase noise is integrated from 10kHz to 20MHz. The total power consumption of the PLL, including triplicated logic, is 16.2mW, which yields $\sim 1.8\text{ mW}$ per channel.

The TDC consists of 8 independent channels, which includes a front-end readout (FERO) and the sampling registers. An additional channel for calibration purposes is included as well. The FERO samples the hit signal coming from the analog front-end and generates the control signals that trigger the capture of the VCO phases. Afterwards, the data is debubbled, encoded, processed and sent to the serializer. The nominal TOA resolution is 24ps, while the nominal TOT resolution is $< 500\text{ ps}$. The nominal sampling frequency is 40 MHz (reference clock frequency), but can be increased up to 160MHz by configuration, if the dead time of the sensor and the analog front-end is small enough. The sampling registers are full custom master-slave clocked-CMOS flip-flops [4]. Most of the power consumption of the TDC comes from the 16 sampling register, the input of which switches at 1.28 GHz . The power consumption, including the PLL, is $\sim 2.8\text{ mW}$ per channel, with a sampling rate of 40MHz. For applications where the time resolution can be relaxed, a lower power consumption mode has been implemented. This mode disables half of the buffers that drive the VCO phases to the TDC, reducing the switching activity. This mode achieves a time resolution of $< 50\text{ ps}$ with a power consumption, including the PLL, of 2.3 mW per channel, with a sampling rate of 40MHz.

Authors: PATERNO, Andrea (CERN); GASCON, David (ICCUB); BANDI, Franco Nahuel (CERN); MAURICIO, Joan (ICCUB); FERNÁNDEZ-TENLLADO, Jose Maria; MANERA, Rafel (ICCUB); GOMEZ, Sergio (ICCUB)

Presenter: MAURICIO, Joan (ICCUB)

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