Contribution ID: **154** Type: **Poster**

Design of the OBELIX monolithic CMOS pixel sensor for an upgrade of the Belle II vertex detector

A monolithic CMOS pixel sensor named OBELIX is beeing designed to equip new detection layers proposed as an upgrade of the current vertex detector of the Belle II detector. Based on the TJ-Monopix2 sensor, OBELIX integrates an extended matrix with 33 micrometers pixel pitch. The chip includes a unique combination of features for this granularity: low-dropout regulators, hit logic to match the Belle II trigger at 120 MHz/cm2 hit rates and a fast hitOR signal used to both time-stamp hits with a few ns precision and to provide fast information for track triggering.

Summary (500 words)

The Belle II experiment is running at the SuperKEK collider, aiming at a luminosity of 6e35 cm-2.s-1. Beam conditions required at such luminosities generate a large and continuous rate of background particles impinging the vertex detector, for which Belle II has initiated an upgrade program. The VTX project proposes a depleted monolithic pixel sensor for this upgrade, the OBELIX chip, in order to improve the granularity in space and time over the current system. The sensor occupies an area of about 19x30 mm? and includes a 464x896 pixel array with 33.04x33.04 um pixel pitch, as well as peripheral circuitry for power regulation, bias generation, digital control and data processing.

The OBELIX-1 chip has been designed in a CMOS 180 nm process as its predecessor TJ-Monopix2, issued from the ATLAS-ITK R&D , from which it inherits the pixel matrix scheme whith a detection performance already assessed. Besides the fired pixel address, the column-drain readout provides 50 ns timing precision (relaxed from the original 25 ns) with 7 bits of arrival time and 7 bits of ToT. OBELIX-1 integrates only two out of four TJ-Monopix2 variants of pixel front-end: a DC and AC coupled diode with a cascode amplifier. This choice results from the tests of TJ-Monopix2 and their careful comparison with the circuit post-layout simulations.

To facilitate system integration, distributed low-dropout regulators are implemented on the matrix side following a previous design from the RD53 project. From input voltage from 2V to 3V, they generate output voltage of 1.8 V (+ 10%, -20%) with a maximum load current of 500mA.
Three new digital processing parts included in the periphery provides critical functionalities for Belle II operation.
- The trigger logic unit allows to transmit efficiently a maximum hit rate of 120MHz/cm2 with a 30 kHz average trigger rate and 10 us trigger latency.
- The peripheral time-to-digital converter samples the hitOR signal combining all pixel outputs in a column at both edges of a 170 MHz clock, providing time stamping of hits at the few nanoseconds level after corrections and as expected from measurements on TJ-Monopix2. According to simulations, the matching with hit addresses works below a hit rate of 60 Mhz/cm2.
- The track trigger transmission unit also makes use of the same hitOR signal to generate a low granularity occupancy map over an integrated time window of 30 ns. The chip sensitive area is divided in 8 macropixels and 8 bits indicating whether each of them have a received a hit or not is transmitted on a specific output line with a 100 ns delay.

The overall chip is designed so that the power consumption is less than 200 mW/cm2 at an average 60 MHz hit rate and with 50 ns time-stamping, as verified in the post-layour simulation.

This presentation will review the overall design of the OBELIX sensor and discuss the quantitative verification of the chip main functionalities used to sign off the submission.

Primary author: BOUDAGGA, Roua

Presenter: BOUDAGGA, Roua

Track Classification: ASIC