Development of Low Temperature Electronics for LAr-TPC

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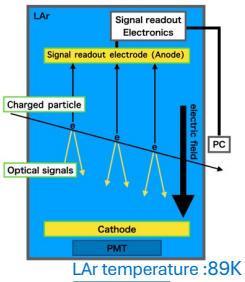
Background

- Liquid argon TPC (LAr-TPC)
  - A 3D imaging detector with massive target.
  - Good particle identification and energy resolution.
- A multi-kton LAr-TPC has been developed for neutrino oscillation and nucleon decay search experiments.

Requirements of signal readout electronics for a large LAr-TPC

- High integration
- Low power consumption
- Large enough gain and dynamic range for the expected physics events
- Low noise
  The front-end electronics is mounted just above the anode to reduce the detector capacitance.



LAr temperature :89K

Our goal

Realizing the readout electronics which can be operated stably at cryogenic environment.

LTARS (Low Temperature Analog Readout System)

LTARS design specification

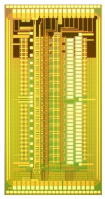
Parameter	High Gain (HG)	Low Gain (LG)
Peaking Time	1 us, 4us	
Conversion Gain	10 mV/fC	0.5 mV/fC
Dynamic Range	±80 fC	±1600 fC
ENC	<3000 e⁻	<62500 e⁻

Unique functions of LTARS

- Two gain modes
  Ensure proper dynamic range
- Enable to switch the shaping time.

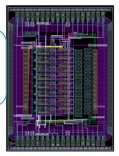
History of our R&D

LTARS2018
- 😊 The characteristics satisfied the requirements at room temperature.
- 😟 The performance was degraded at low temperature.
  - Due to increase of the threshold voltage of the transistor.



implemented the temperature compensation circuit

LTARS2020
- 😊 Satisfied the requirements at both room and low temperature.



Higher functionality and versatility

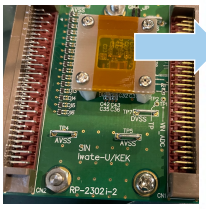
LTARS16A

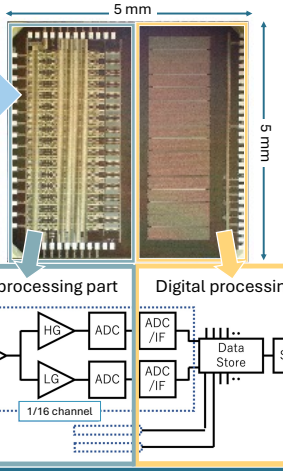
LTARS16A

ASIC chip based on TSMC 180nm CMOS

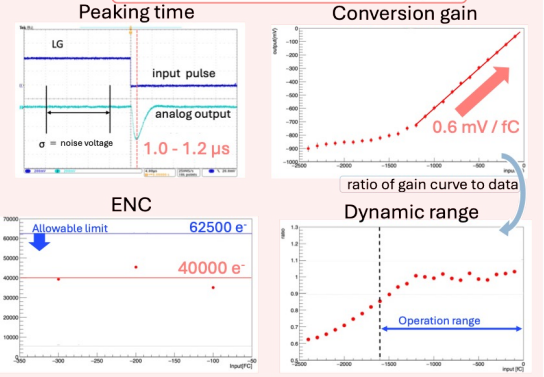
Specifications

- A/D convertor is implemented in the ASIC.
- Two trigger modes : external / internal
- Two processing modes : trigger / continuous
- Simultaneous outputs of HG and LG signals.



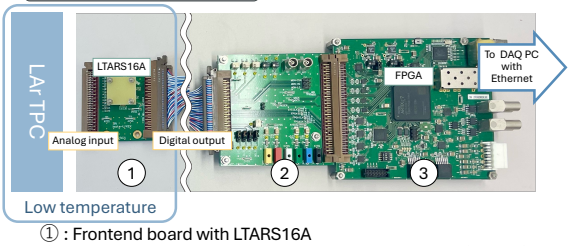


Characteristics of LTARS16A (LG)

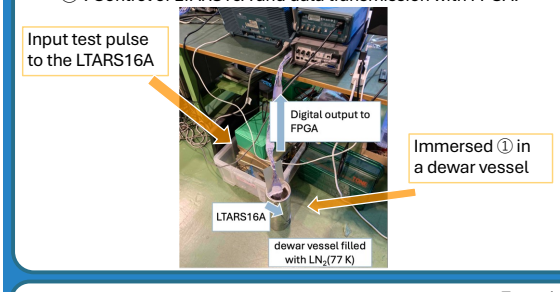


The performance of LTARS16A at room temperature satisfies the requirements.

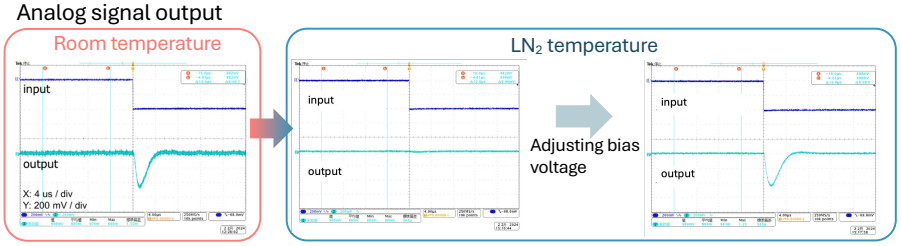
Cryogenic test



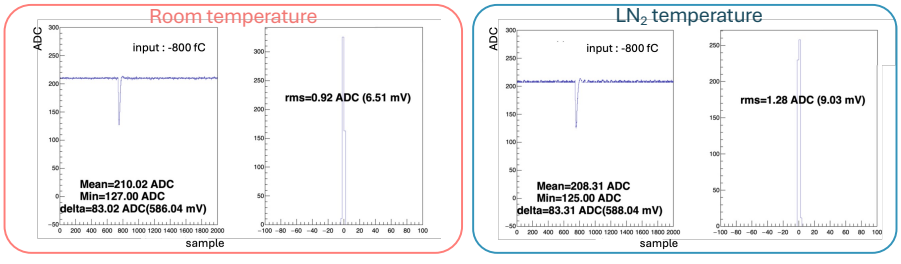
① : Frontend board with LTARS16A
② : Power supply to LTARS16A and interface between ① and ③.
③ : Control of LTARS16A and data transmission with FPGA.



Analog signal output



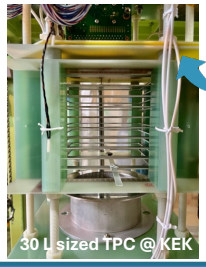
Digital signal output



Even at LN_2 temperature the performance satisfies the requirements !

Test with TPC

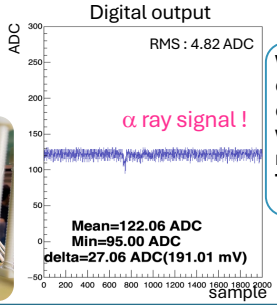
LTARS16A is mounted on the 30 L sized TPC



2 ASIC boards for X Y directions are mounted just above the anode.

Test with α source in gas Ar

Digital output



We successfully observed digital output **for α rays with the LTARS16A mounted on the TPC.**

Summary

- We have developed the electronics for LAr-TPC (LTARS) which can be operated stably at cryogenic environment.
- In the current study, a new ASIC (LTARS16A) with higher functionality and versatility has been developed.
- We have confirmed the performance as expected for a test pulse and α rays.
- We are now planning to test it with the TPC in LAr.

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