## **TWEPP 2024 Topical Workshop on Electronics for Particle Physics**



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## Development of Low Temperature Electronics for LAr-TPC

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We developed signal readout electronics for a liquid argon time projection chamber detector, envisioned for use in neutrino oscillation and nucleon decay search experiments. The front-end electronics are based on the ASIC technology, which consists of a 16 channels analog processor, an analog-to-digital converter, and a signal transmitter for digital processing. We demonstrated that the electronics possess a dynamic range for input charge up to 1400 fC and output signal with an appropriate time constant, which meet the requirements of the experiments. We also tested the electronics at cryogenic temperature and confirmed the same performance as at room temperature.

## Summary (500 words)

In the field of particle physics, a large (multi-kton) liquid argon time projection chamber (LAr-TPC) has been primarily developed for neutrino oscillation and nucleon decay search experiments. The LAr-TPC can reconstruct a charged particle in 3D and identify particles by measuring the energy loss according to the ionization along the track. These unique features enable a clear and comprehensive picture of the particle reactions in the detector, which makes it possible to distinguish the physics of interest with high accuracy.

To realize a large LAr-TPC, it is necessary to develop electronics which meet the requirements such as high sensitivity to target physics events, stable operation in cryogenic environments, and multi-channel signal readout, which can cover a large effective area of the detector. Therefore, we developed dedicated signal readout electronics for use in the LAr-TPC.

The front-end electronics developed in this study, referred to as LTARS16A, are based on the ASIC technology and implemented in the TSMC 180 nm CMOS. The chip size is 5 mm x 5 mm and it possess 16 identical signal processing channels. A simplified block diagram a channel is shown in Fig. 1. The detector readout channel is connected to a charge-sensitive-amplifier (CSA). The CSA output is then divided into two parts, and each signal is fed to individual amplifiers with different gains, high gain (HG) and low gain (LG), to ensure a wide dynamic range. After amplifying and shaping the signal in the HG/LG amplifiers, the signal is converted to 8-bit digital data using an analog-to-digital converter (ADC). The digital data of all the channels (16 channels x two types of amplifiers: HG/LG) are stored in the digital signal processing parts, followed by serialization and transmission to the digital processing circuit.

We tested the LTARS16A at room temperature and cryogenic temperature immersing the circuit in liquid nitrogen (T  $\sim$  77 K). Table 1 lists the characteristics of LTARS16A obtained from the room temperature test. The measured values are almost identical to the design values based on requirements of the experiment. Figure 2 shows the analog output signals for an input charge of -800 fC at room temperature and cryogenic temperature. We observed almost the same output pulse. Note that the feedback resistance was adjusted in the cryogenic temperature test. Figure 3 shows the output from the ADC for an input charge of -800 fC at room temperature and cryogenic temperature. There were no significant differences in the ADC values at these different temperatures. We conclude that the performance of LTARS16A is the same at cryogenic temperature and at room temperature environments. In this paper, we also discuss the results of a cosmic ray test wherein these electronics were implemented in a small LAr-TPC. Primary author: MORITA, Ayumi (Iwate University)

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