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HPSoC: A very high Channel Density Waveform Digitizer with sub-10ps resolution - front end design and measurements

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Abstract: We present the architectural design, prototype fabrication and first measurements for the second revision of the High Pitch digitizer System-on-Chip (HPSoC) prototype. The HPSoC concept is that of a high channel density and scalable waveform digitization ASIC with an embedded interface to advanced high-speed sensor arrays such as e.g. AC-LGADs. The chip was fabricated in 65nm technology and targets picosecond-level timing resolution via high speed waveform sampling (10 Gsps) and autonomous chip triggering. Details on the front end Transimpedance amplifier design and measurements without and with LGAD sensors will be presented.

Summary (500 words)

In recent years, the introduction of very fast optical sensors with extremely low pitches (e.g. Low Gain Avalanche detectors -LGADs) has enabled high-density designs for high energy and nuclear physics detectors offering excellent spatial and timing precision; the performance of detector systems composed of large arrays of such components is currently limited mostly by the readout capabilities of the existing readout electronics. To address these issues, we studied and designed the architecture of the HPSoC, a customized multi-channel waveform digitizing readout that is capable of directly interfacing with state-of-the-art sensor arrays, can extract relevant information from each pixel's interaction and internally combine such information in a compact digital format, with timing precision at the picoseconds level and capable of sub-pixel spatial precisions at a few tens of micrometers or less. The design has been described in a previous contribution. In this work we concentrate on the design and characterization of the front end amplifier.

In order to demonstrate the feasibility of the design and test some of its critical components, a prototype chip containing most of the parts of the design and with 4 fully functional channels was designed. A fully functional digitizer and a preliminary mechanism for self-triggering and autonomous operation was incorporated as well. The part has been fabricated in 65nm CMOS technology. The TIA is an evolution of a previous design that was tested in the first generation of the chip, that proved adequate but suffered from a few limitations - mostly in terms of high input resistance and lower than expected gain. The new revision uses an improved topology, consisting in a regulated cascode stage to reduce the input impedance, and a wide band gain stage. Simulations show reduction of more than a factor of 5 in input impedance, thus making the part more robust to input capacitance increase. It also shows a moderate but significant increase (factor of 1.7) in gain. A small level of control over the gain and bias level of the TIA stages is possible via internal digital switches.
The fabricated dies have been direct-bonded to a test board that permits testing of a test structure using calibration capacitive inputs, as well as connection to various types of sensors. Furthermore, the board does allow interfacing with a flexible readout controlled via an external FPGA for configuration of the internal parameters and testing of full mixed signal setup (TIA + digitizer) as well as the external and self-triggering capabilities.

We will report on the performance of the TIA using calibration input signals, and signals generated using AC-LGAD strip and pixel sensors using a laser Transient Current Technique (TCT) system. Sensors with varying strip lengths and thus different input capacitance for the HPSoC will be shown.

The digital front end and back ends have also been designed for future integration. Upon satisfactory test completion, we will proceed designing, fabricating and testing a fully functional revision with a larger number of integrated channels incorporating front end and back end digital partitions.

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