Contribution ID: **104** Type: **Poster**

An ASIC for ToF-PET application with MCP-PMTs

We present the R&D of FPMROC, an ASIC for ToF-PET with a fast MCP-PMT (FPMT). The design architecture includes a preamplifier, a discriminator with programmable threshold, a time- to-digital converter, an event builder with a serializer, a clock unit, and a SPI. We aim for a time resolution below 10 ps, matching the targeted FPMT parameters. We are designing the first prototype using a 55 nm CMOS technology. Although the development is for a ToF-PET, the design may find applications in time measurements in future physics experiments. The prototype submission is in July.

Summary (500 words)

The MCP-PMT exhibits excellent response to single photoelectrons, with a rising time of less than 100ps. The transit time spread (TTS) is exceptionally small, around 10 ps for multi-photoelectrons and less than 50 ps for single photoelectrons. This capability offers the potential to enhance coincidence timing, thereby improving the image quality of positron emission tomography (PET) and next-generation physics experiments.

Given the need for fine time resolution measurements in the picosecond domain, we have developed a prototype frond-end circuit named FPMROC, to measure the time of arrival from the FPMT with a gain of 1E5. The FPMROC is designed in a 55 nm CMOS process and incorporates a full readout chain, including a low-noise preamplifier, discriminator, time-to-digital converter (TDC) for time of arrival (TOA) and time-over-threshold (TOT) measurements, as well as fast data serialization and data driver for output.

Two amplifier schemes have been implemented. The first scheme uses multi-stage amplifiers to saturate the signal, with each stage characterized by a high bandwidth but low gain. The second scheme employs a classic trans-impedance amplifier, where a common-source is provided with feedback by a resistor. While the preamplifier in the second scheme offers higher gain than the saturated scheme, it operates at a slower speed. The input impedance is designed to be approximately 50 Ω for impedance match. The hit pulse is generated by a discriminator, which operates above a threshold set by an internal digital-to-analog converter (DAC).

The TDC consists of two stages. Firstly, a differential ring oscillator with 11 delay cells generates a cell delay of about 78 ps. Then, a passive interpolator divides this delay to around 13 ps by a factor of 6. The hit signal is captured by a register array at rising edges of a latch signal. The propagation delay of each delay cell is sensitive to process variation, temperature, and power supply. To mitigate these variations, a system clock self-calibration approach is used to record the timestamp twice. Additional measurements for each hit signal calibrate the differential delay cells, thereby improving measurement precision.

An event builder is devised to cache data from 8 TDC channels, whereupon it frames and encodes the data before outputting it as 64-bit, 160M/s data to a serializer. Two-level FIFOs are used for data storage and aggregation. A framer retrieves and assembles data, which is then passes to a 64B66B encoder incorporating scrambling algorithms from 10G Ethernet to maintain the DC balance of data. Finally, a gear boxer is used to align with the data rate and width requirements of a high-speed serializer.

The serializer transmits serial data at a rate of 10.24 Gbps, using a high-quality differential clock generated by an LC-based phase-locked loop (PLL). Additionally, the PLL provides a 40 MHz CMOS clock for the TDC.

An 8-channel prototype ASIC will be submitted in July. The simulation results indicates an RMS resolution of 10 ps could be realized with a power consumption of 40 mW per channel.

Primary author: YAN, Xiongbo (Institute of High Energy Physics, CAS)

Co-authors: DENG, Binwei (Hubei Polytechnic university); XIA, Chuan (Central China Normal University); WANG, Chuanye (Nanjing University (CN)); Prof. GUO, Di (Central China Normal University); ZHANG, Guoxiang (Central China Normal University); HUANG, Jiaoyang (Central China Normal University); YE, Jingbo (Chinese Academy of Sciences (CN)); WANG, Jun (Wuhan Textile University); XIAO, Le (Central China Normal University CCNU (CN)); ZHANG, Wei (Wuhan Textile University); DAI, Wenjie (Central China Normal University); LI, Xiaoting (IHEP); YUAN, Yuan (Chinese Academy of Sciences (CN)); ZHOU, Zijie (Central China Normal University)

Presenter: YAN, Xiongbo (Institute of High Energy Physics, CAS)

Track Classification: ASIC