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A Monolithic Active Pixel Sensor with a Novel Readout Architecture for Vertex Detector in particle physics Experiments

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We present the design and preliminary test results of a MAPS sensor prototype MIC6_V1 based on a 55nm Quad-well CMOS Image Sensor process for the vertex detector application. In order to achieve high-spatial resolution, fast readout, and low power consumption, MIC6_V1 has implemented a new node-based, data-driven parallel readout architecture. The integration time is 5us, and by sharing VCO in the pixel group, the hit arrival time resolution can reach 10ns. The pixel size of MIC6_V1 is 23.6 μm × 20 μm. The pixel matrix is 64 rows by 64 columns, and the size of MIC6_V1 is 2.8mm × 2.8mm.

Summary (500 words)

The vertex detector in high energy physics experiment requires high spatial resolution, fast readout, and low power consumption. The Monolithic Active Pixel Sensor (MAPS) is the most promising candidate technology to satisfy all those requirements. We have developed the MAPS sensor MIC6_V1 in a 55 nm quad-well CMOS image sensor process with a node-based data-driven readout scheme.

MIC6_V1 contains a pixel matrix of 64 rows by 64 columns with a pixel size of 23.6 μm 20 μm. Each pixel contains a sensing diode, an amplification, a discriminator, and a hit storage register connected to a node-based sparse readout circuitry. Every double-column of pixels share a readout circuit, and 4x2 pixels form a super pixel group. The 8 pixels in each super pixel share a VCO for hit arrival time measurement. The VCO oscillates only when the super pixel group is hit to reduce power consumption. The oscillation frequency of VCO can be configured between 100 ˜ 200 MHz. Each super pixel also includes a node of sparse readout logic circuit, and the hit information will be asynchronously transmitted to the bottom of the double-column through the readout nodes. Readout nodes transmit data based on request-acknowledge handshake protocol. When a super pixel group is hit, 20 bit data will be generated, including 4-bit super pixel group address, 8-bit time counter and 8-bit hit shape.

In the bottom of MIC6_V1, a periphery readout module also based on asynchronous readout node has been implemented to readout 20-bit data and 5-bit column address from each double-column. Then, a synchronizer module is connected to the peripheral readout module, which is responsible for processing handshake, data synchronization, data bit-width conversion, and finally outputting the data. In addition, an asynchronous handshake multiplexer module is implemented, through which any double-column can be tested independently.

We first individually tested each double-column readout link. The data port at the top of each double-column readout link was configured with a test pattern. By sending a request signal to the top of the double-column, the chip would output the correct response signal at the top, completing the handshake and writing the test pattern data into the double-column. After transmission through 16 nodes within the double-column, a request signal was output at the bottom, and the test pattern was observed at the data port at the bottom. The entire process took approximately 25ns, indicating that the hit information of a super pixel group could be output every 1.56 ns. In addition to testing the double-column readout link through the top, we further evaluated the functionality of the double-column readout link by using test signals within the pixels. By activating test pulse enable switches inside certain pixels and combining them with the test Pulse signal and Strobe

signal, we simulated situations where pixels are hit. As a result, we observed the expected 20-bit data and request signal at the bottom of the double-column. Based on this, we tested the readout of the entire chip array through the peripheral asynchronous readout module and synchronizer module.

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