Development of a 10–bit ultra-low power SAR ADC with internal threshold in 130 nm CMOS technology

Patryk Prus, Miroslaw Firlej, Tomasz Fiutowski,
Marek Idzik, Jakub Moron, Krzysztof Swientek
Faculty of Physics and Applied Computer Science
AGH University of Krakow

April 26, 2024

Abstract

The design and simulation results of an ultra-low power fast 10-bit SAR ADC in CMOS 130 nm technology, are presented. This ADC is an extension of experimentally verified (INL,DNL $<$ 0.5 LSB, ENOB$>$9.5) 10-bit SAR ADC working up to 50 MSps and consuming 680 uW@40 MSps. The goal of the new design was to add an internal threshold for the processed input signal, so as to stop the conversion and thus greatly reduce power consumption in case the signal is below the threshold. The designed ADC will soon be submitted for fabrication.

Summary

In modern and future detectors for particle physics experiments a fast, ultra-low power, area-efficient ADC is an indispensable component for complex multi-channel readout ASIC. This work presents the development of a 10-bit SAR ADC, with an implemented internal threshold for input signal, operating up to ∼40 MSps and consuming ∼250 uW@40 MSps, at low particle occupancy. The ADC was verified in post-layout simulations and will soon be submitted for fabrication.

The new ADC is an extension of existing and experimentally verified, radiation-hard, 10-bit SAR ADC [1], so the architecture and main blocks are similar or sometimes even the same. A fully differential ADC architecture was chosen, comprising a pair of bootstrapped switches, a differential capacitive Digital-to-Analog Converter (DAC), a dynamic comparator, and an asynchronous dynamic control logic. A fully dynamic architecture is used to eliminate the static power while asynchronous logic eliminates a fast bit-cycling clock distribution. The Merge Capacitor Switching scheme is implemented in the capacitive DAC.

The main difference between the new and existing ADC is in the operating algorithm, governed by asynchronous control logic. In the new design, an additional functionality for comparing input signal with the internal ADC threshold was implemented. The main goal was to stop the conversion and thus greatly reduce power consumption when the signal is below the threshold. To do this, an additional conversion cycle was added to compare the input signal with the threshold. If the signal is above the threshold the ADC conversion consists of 11 conversion cycles (instead of 10 cycles). As a result, for signals above the threshold the ADC is slightly slower and consumes more power than the existing version, but for signals below the threshold it is much faster and consumes much less than the existing ADC.

To obtain a realistic performance estimation, post-layout simulations of the new ADC were performed and compared with post-layout simulations of the existing ADC [1]. For an input signal above the threshold, the new ADC was found to be ∼10% slower and consume ∼15% more power than the existing ADC. On the other hand, when the signal is below the threshold, the conversion is much faster and the power consumption is less than one-third of the existing ADC. From these results, it was calculated that for low particle occupancy of about 1% the power consumption would be about one-third (∼250 uW@40 MSps) while for 10% occupancy about 40% of the power of the existing ADC.

In this presentation, the design of the new ADC will be presented along with the post-layout simulation results and comparison with the existing ADC.

References

[1] M. Firlej, T. Fiutowski, M. Idzik, S. Kulis, J. Moron, K. Swientek, *An Ultra-Low Power 10-bit, 50 MSps SAR ADC for Multi-Channel Readout ASICs*, *Journal of Instrumentation*, JINST 18 (2023) P11013.