Development of a 10–bit ultra-low power SAR ADC with internal threshold in 130 nm CMOS technology

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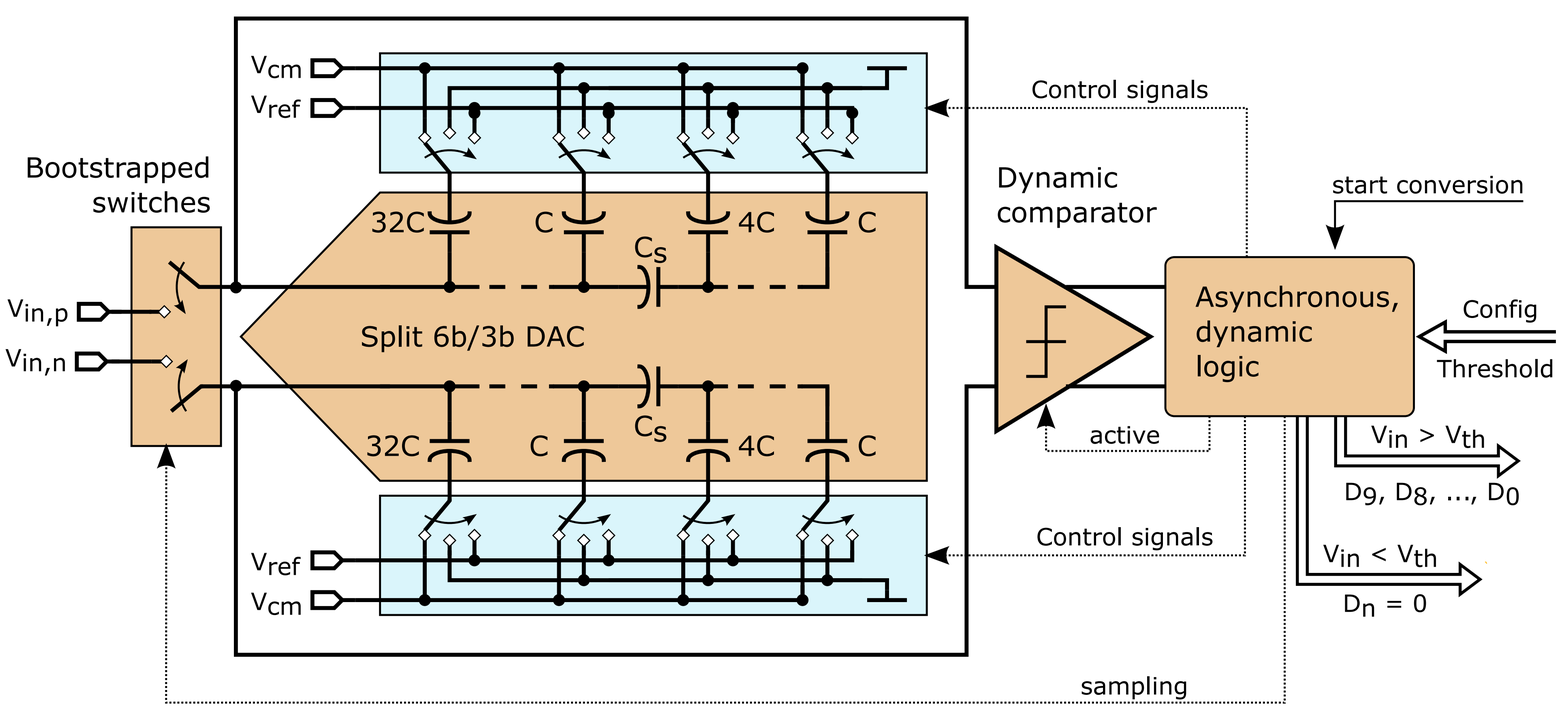
Introduction

The design and simulation results of an ultra-low power fast 10-bit SAR ADC with an internal threshold, developed for multi-channel readout systems, in particular for applications in particle physics experiments, are presented. The ADC was designed in 130 nm CMOS technology, it works up to $\sim$ 40 MSps and consumes $\sim$ 350 μW@40 MSps, at low particle occupancy. The new ADC is an extension of the existing 10-bit SAR ADC[1] with the difference in the operating algorithm, governed by an asynchronous control logic. An additional functionality for comparing input signal with an internal ADC threshold was implemented. If the signal is above the threshold the ADC conversion consists of 11 conversion cycles, instead of 10 cycles. As a result, for signals above the threshold the ADC is slightly slower and consumes more power than the existing version, but for signals below the threshold it is much faster and consumes significantly less than the existing ADC.

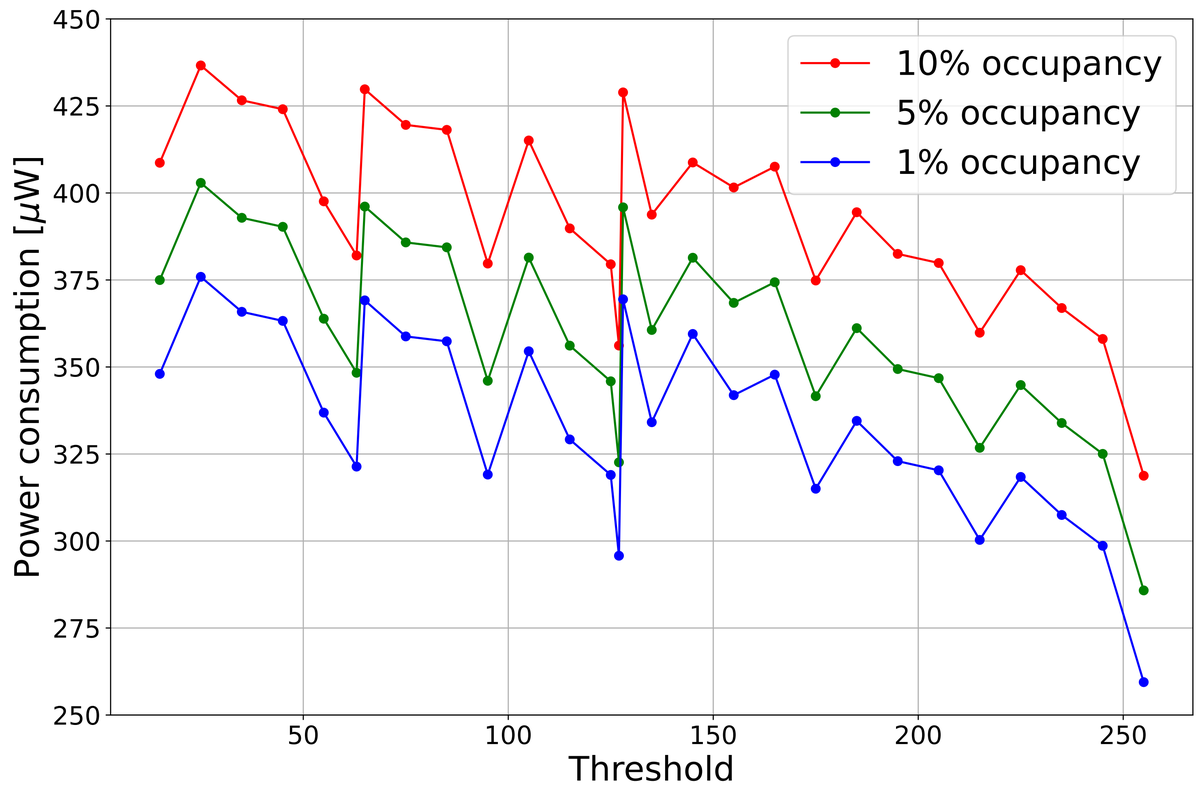
Design



An additional conversion cycle was added to compare the input signal with the user-defined 8-bit threshold. The comparison is performed after determining the Most Significant Bit (MSB). If the threshold voltage (Vth) is higher than the remaining signal and MSB=0, the conversion is terminated, and all bits are set to 0. However, if Vth is lower, the conversion proceeds in the standard manner. The comparison with the internal threshold can be disabled, allowing the ADC to operate as the existing one.

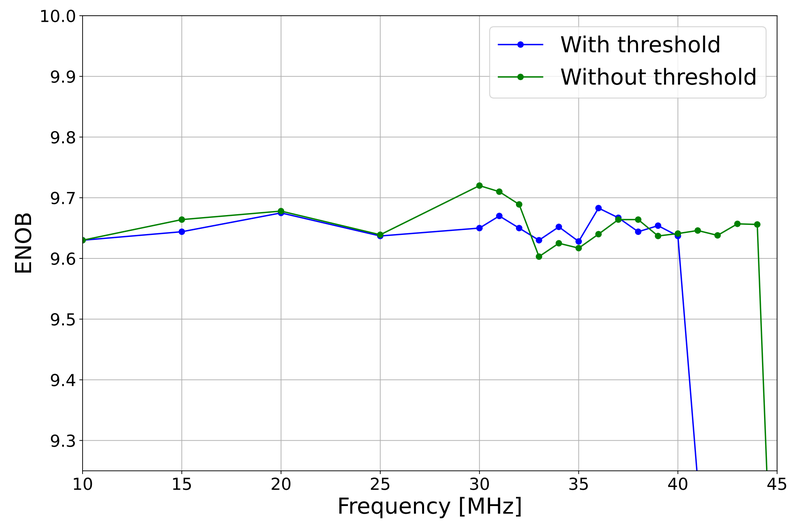
Power vs Occupancy

Power consumption versus threshold for different occupancies @40 MSps



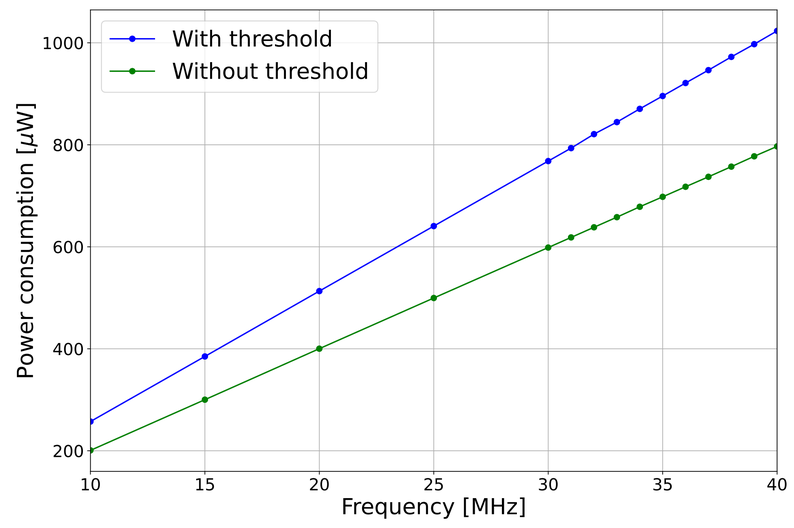
Performance

Effective number of bits versus sampling rate with and without threshold



Power Consumption

Power consumption versus sampling rate with and without threshold



Summary

- The design and simulations of a novel ultra-low power SAR ADC with an internal threshold have been completed.
- Post-layout simulations show that the ADC works up to 40 MSps with ENOB above 9.6 and at low occupancy consumes about 350 μW@40 MSps.
- A prototype ASIC with few ADC channels is under preparation and should be submitted to production in close future.

Acknowledgements

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Reference

[1] M. Firlej, T. Fiutowski, M. Idzik, S. Kulis, J. Moron, K. Swientek, *An Ultra-Low Power 10-bit, 50 MSps SAR ADC for Multi-Channel Readout ASICs*, *Journal of Instrumentation*, JINST 18 (2023) P11013.