A 14bit 100 MS/s Two-Step Split SAR ADC using low-power high-linearity RA without any internal phase compensation and in-stage redundancy technology

Abstracts

Since full waveform sampling can provide more accurate signal information which is important for particle detectors. So high-speed, high precision and low power consumption Analog to Digital Converter is needed. A two-step sub-SAR ADC is used to achieve low power consumption and using pipeline principle to improve the speed. In-stage and between-stage redundancy technologies are used to improve the SNDR. A three stages amplifier without any internal phase compensation are used as the residue amplifier to decrease the power consumption. The simulation results show that the SNDR can be up to 84.2dB, and the power consumption is less than 25mW.

Summary

The energy of the particle beam of the Heavy Ion Research Facility-Cooling Storage Ring (HIRFL-CSR) in Lanzhou, China, can be as high as several GeV/u, and the heavy ion collision experiment in this energy region is of great significance for understanding the properties of QCD species in the low-temperature and high-density region. In order to solve this scientific problem, researchers propose to build a universal low-temperature and high-density nuclear material measurement spectrometer (CEE) on the CSR platform, which can realize the full-space measurement of secondary particles in heavy ion collisions in the GeV energy region, and provide experimental data for the study of QCD and other nuclear reaction kinetics. Topmetal-CEE is a detection chip with anti-irradiation ability used in CEE projects, which is located at the front end of the incident beam of CEE, and is mainly used to detect the position, time and energy information of the incident beam current. In order to further ensure that the analog information at the front-end of the Topmetal-CEE chip can be quantified and read out fast and accurately, an on-chip

ADC is required to complete the data transmission, while also meeting the overall low power consumption requirements of the detector.

To meet the energy resolution and speed of the experiment, the resolution of the ADC is 14 bits and the sampling rate of the ADC should reach 100MS/s. Successive approximation (SAR) ADC has low power consumption and high compatibility while pipeline ADC has high speed. In this work, to combine the performance advantages of these two ADCs, a two-step split SAR ADC using 55nm process has been designed.

We have studied that the overall power consumption is the lowest when the first-stage SAR ADC is 9 bits, and the second-stage SAR ADC is 7 bits which include two bits between-stage redundancy. To add an additional in-stage redundancy to improve the SNDR, so the convert number of the two stage SAR ADCs are 10 bits and 8 bits actually. A switching strategy based on monotonic switching is adopted, which can greatly reduce the power consumption and the number of unit capacitors. In addition, an offset self-calibration technology based on charge pump is designed to further reduce the influence of the offset of the comparator. The Residue Amplifier (RA) between the two stages is based on closed-loop operational amplifier. While to reduce the power consumption and increase the bandwidth, the amplifier is using three stages amplifier without any internal phase compensation. The pre-simulation results show that the effective bit of the whole ADC can reach 13.69 bits at a sampling rate of 100 MS/s. The spurious-free dynamic range SFDR is 92.3dB. The signal-to-noise distortion ratio SNDR is 84.2dB. The total power consumption of the overall ADC is less than 25mW.

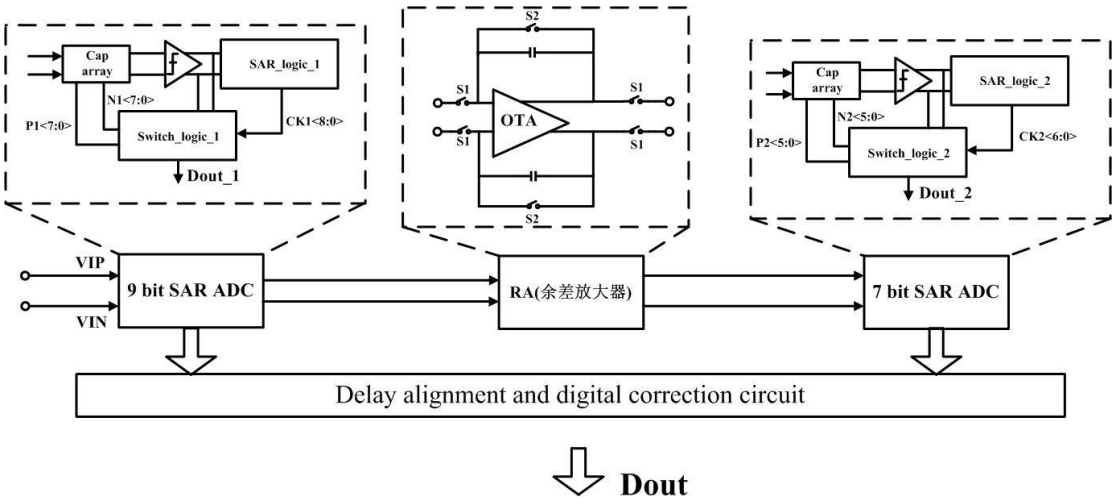

Figure 1. The proposed two-step split SAR ADC structural diagram of the ADC in this work

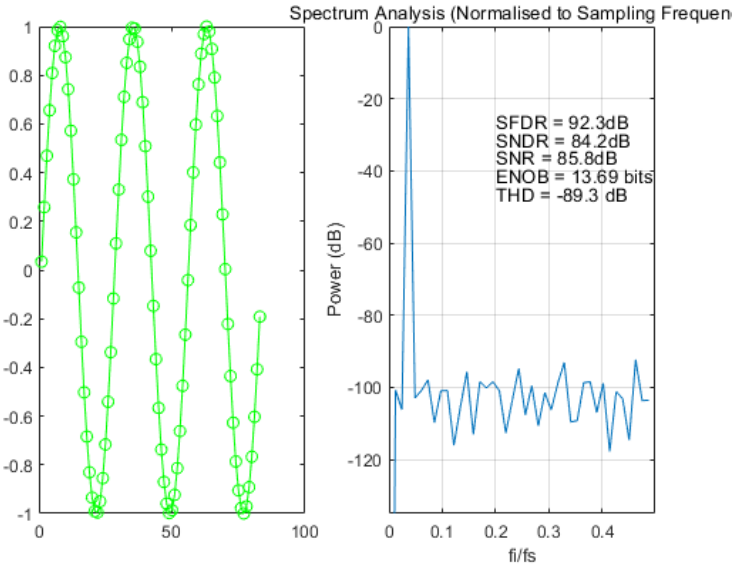

Figure 2 pre-simulation results of the ADC FFT analysis with an input signal frequence of 10M at 100M Sampling rate