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Evaluation of efficiency, radiation hardness, and timing performance of the Analogue Pixel Test Structure for ALICE ITS3

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During the upcoming Long Shutdown (LS3) of the LHC, the three innermost layers of the ALICE Inner Tracking System (ITS2) will be replaced by ITS3, a new vertex detector utilizing curved, stitched wafer-scale monolithic silicon sensors, fabricated using 65 nm CMOS technology and thinned to 50 µm. The feasibility of this technology for ITS3 was examined in the initial test production run (MLR1). This contribution will provide a brief overview of the MLR1 submission and discuss the latest sensor characterization results of the Analogue Pixel Test Structure, focusing on the detection efficiency, timing response and radiation hardness.

Summary (500 words)

The upgraded Inner Tracking System (ITS2) of the ALICE experiment at the LHC, featuring CMOS monolithic active pixel sensors, known as ALPIDE, is currently operational and showcasing excellent performance in LHC Run 3. The forthcoming ITS3, scheduled for installation during the LHC Long Shutdown 3 (2026-2028), aims to enhance tracking precision and efficiency, particularly for particles with transverse momentum as low as 0.1 GeV/c. ITS3 is a cylindrically bent silicon vertex detector designed with stitched wafer-scale monolithic active pixel sensors employing the Tower Partners Semiconductor Co. (TPSCo) 65 nm technology.

The initial assessment of this technology, through the first submission (MLR1: Multi-Layer Reticle 1), including test structures like the Analogue Pixel Test Structure (APTS), has been conducted since 2021. The APTS, featuring a 6×6 pixel matrix with a direct analogue readout for the central 4×4 pixels, was designed in two output buffer variants: a source-follower (APTS-SF) and a fast operational amplifier (APTS-OA). Sensor variants included different pixel pitches from 10 µm to 25 µm, with alterations in the geometry and size of p-well and n-well collection electrodes, fabricated in various processes. Initial results of detection efficiency from non-irradiated APTS-SF chips and the timing performance of APTS-OA were presented at TWEPP 2023. Subsequent laboratory measurements and beam tests, along with comprehensive analysis, were performed in 2023 and 2024.

The APTS-SF not only achieved an energy resolution of 4% at the Mn-Kα peak from 55Fe source measurements but also maintained a detection efficiency of 99% or higher for all pitches at a temperature of approximately 15℃, even up to a non-ionizing energy loss (NIEL) of 10ˆ14 1 MeV neq cmˆ−2, well above the requirements set for ALICE ITS3. Notably, this efficiency persisted up to a NIEL of 1 × 10ˆ15 1 MeV neq cmˆ−2 for a 15 µm pitch and 2 × 10ˆ15 1 MeV neq cmˆ−2 for a 10 µm pitch. Even after exposure to 3 × 10ˆ6 Gy, the detection efficiency remained at 99%, meeting the total ionizing dose (TID) requirements for both ALICE ITS3 and the future ALICE 3 vertex detector. An in-pixel efficiency study showed the dependence of the efficiency on the position inside the pixel cell. It revealed the efficiency losses predominantly at pixel edges and corners at high thresholds. Charge distributions and detection efficiency, tested with an alternative readout (Caribou) system for the chip with 25 µm pitch, aligned well across setups, confirming the results.

The APTS-OA, equipped with fast individual operational amplifier-based buffering, exhibited a time resolution as low as 63 ps in the latest beam tests, significantly surpassing performance achieved with the previous 180 nm CMOS process, and opening avenues for broader applications beyond high energy physics.

This presentation will detail the latest APTS characterization results from laboratory 55Fe source measurements and beam tests, considering different reverse substrate biases and varying NIEL and TID irradiation levels.

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