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Development of high-speed serializer transmitters in 180 nm technology for CEPC vertex detector readout electronics

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Introduction

- The Monolithic CMOS Pixel Sensor is a promising candidate for the Vertex Detector of the Circular Electron Positron Collider due to its favorable performance and balanced trade-offs among granularity, readout speed, material budget, and power consumption. We have developed a dedicated full-scale TaichuPix chip, which features a matrix of 512 × 1024 pixels, each measuring 25 × 25 μm², resulting in a total chip area of approximately 4.06 cm². This chip aims to achieve a spatial resolution better than 5 μm and is currently developed using a 180-nm CMOS Image Sensor technology.
- To maintain a high-speed readout and a low material budget, the TaichuPix chip demands a raw data rate up to 3.84 Gbps and power consumption of less than 25 mA/Gbps for the serializer circuit. The TaichuPix1 achieved a maximum data rate of 3.36 Gbps with large jitter and current. Subsequently, two 4Gbps serializers (20:1 and 40:1) were developed and optimized to meet the requirements, using the same 180-nm process node as the TaichuPix, while considering funding and time constraints.
- The preliminary tests showed low jitter characteristics of the RO-PLL, and the LC-PLL featured better jitter performance despite this version's biasing problem, and both serializer circuits functioned correctly.
- A revision has been implemented to address the biasing issue. Preliminary tests showed a clear eye diagram at 4 Gbps, with a total jitter of 85 ps.

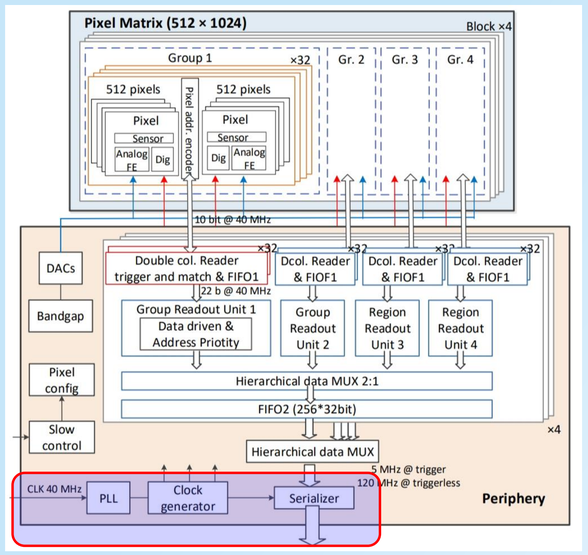

Fig.1. The block diagram of the full-scale TaichuPix chip

Design and performance of circuits

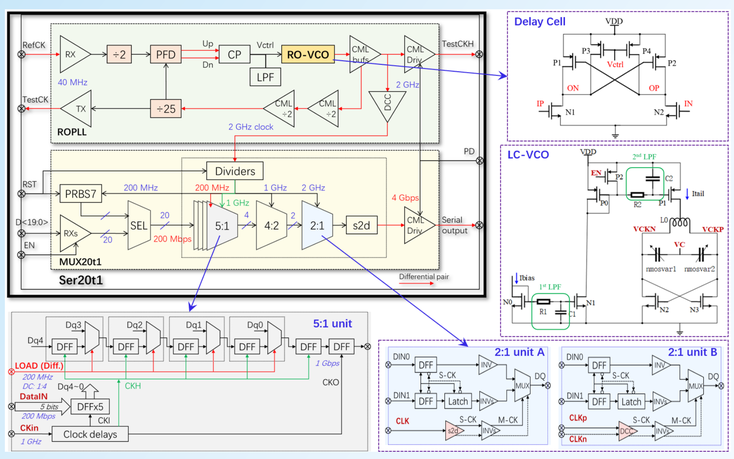

Fig.2. Schemes of the serializer designs

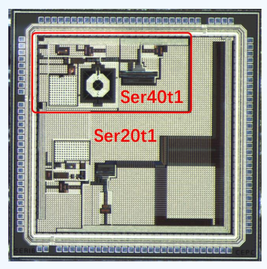

Fig.3a. Microphotograph of the prototype design（3 ×3 mm² ）

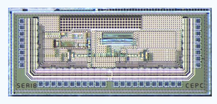

Fig.3b. Microphotograph of the revision design（1 ×2.45 mm² ）

The prototype designs

- *The serializer (Ser20t1 or Ser40t1) is mainly composed of a phase locked loop (ROPLL or LCPLL), a multiplexer (MUX20t1 or MUX40t1), a CML driver and other test circuits, as shown in Fig.2. The multiplexer consists of several 5:1 sub-units based on a shift-register chain and a 4:1 or 8:1 sub-multiplexer based on a binary-tree structure (2:1 unit A and B). The simulated current at 4 Gbps of the Ser20t1 and Ser40t1 is about 75 mA and 84 mA, respectively.*
- *The performance of the three PLLs is summarized in the table below.*

Performance	RO-PLL	LC-PLL*	PLL in TaiChuPix
Simulated Frequency range (FTR) (GHz)	0.34 ~ 3.12	1.8 ~ 2.3	0.32 ~ 3.4
Phase Noise @1MHz (PN-1M) (dBc/Hz)	-103	-118	-100 @ 2.24 GHz
Loop Bandwidth (LBW) (MHz)	0.5 ~ 2.9	0.22 ~ 1.3	0.53 ~ 4.8
Current (mA)	~ 27.63	~ 34	~ 40
Area (including test modules) (mm²)	0.35	0.68	0.24
Inputs and outputs of clocks	Differential	Differential	Single-end
***Measured** FTR (GHz)*	***0.32 ~ 2.95***	***1.81 ~ 2.45@2.6V****	***0.32 ~ 2.91***
***Measured** RMS jitter (Rj) (ps)*	***<1.8***	***<1***	***~5***

The revision design

- **We identified a problem during tests within the biasing circuit which was used in the LCVCO and CML drivers (refer to Fig.4 a).*
- *The simulation results, as presented in Fig.5, indicate that the start-up function operated correctly with a 1.8-V power supply, and the VBN stabilized after approximately 10 μs. Nevertheless, the chip did not function as expected during the preceding laboratory measurements.*
- *To address this, we revised the design and implemented a simpler diode-biasing circuit instead (refer to Fig.4 b). The new design used the ROPLL and MUX40t1 without parallel inputs, allowing for a rapid verification of the issue. And the simulated total current at 4 Gbps is about 78 mA.*
- *Comparison simulations of the driver with two biasing schemes are shown in Fig.6.*
- *Debugging efforts will continue to verify the star-up circuit and the transistor sizes in order to resolve the issue.*

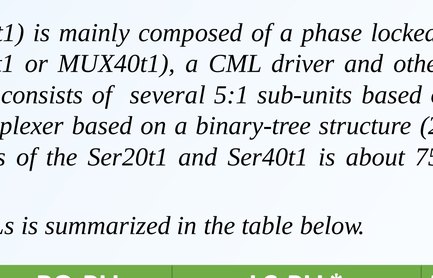

Fig.4 (a) Schematic of the bias generator (b) Biasing of the revision

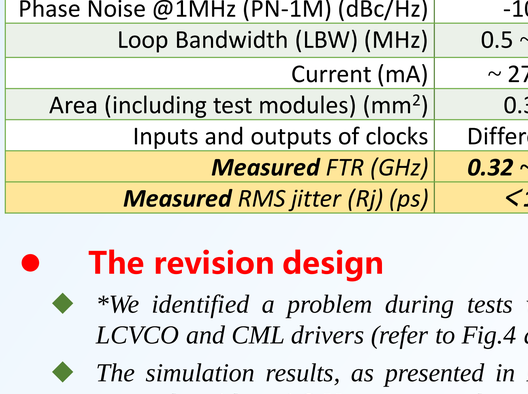

Fig.5. Transient waveforms of the start-up simulations

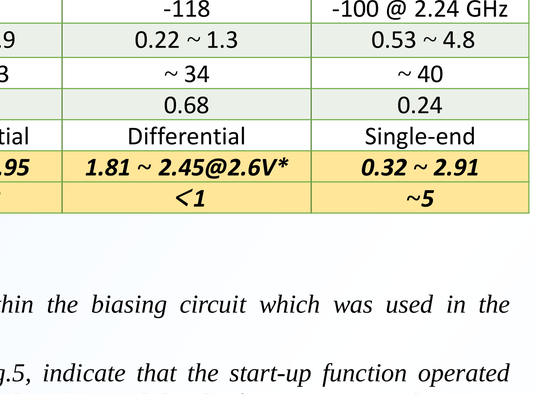

Fig.6. Transient-waveform comparisons of the two versions

Preliminary tests and results

The clock and serial data are tested by a 16-GHz wide-band oscilloscope (LeCroy SDA 816Zi-A) through SMA connectors and coaxial cables. The 1.8-V power supply is provided by a TLV1117 chip on the PCB board.

Tests of the RO-PLL

- *Frequency tuning range:* *0.33~3 GHz*
- *RMS jitter of the 20-MHz clock:* *~2.1 ps (SDAii), ~1.5 ps (TIE)*
- *RMS jitter of the 2-GHz clock:* *~1.33 ps (SDAii), ~2.3 ps (TIE)*

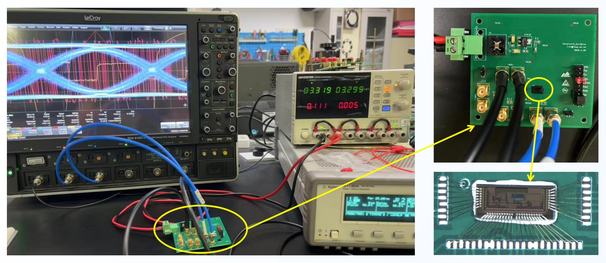

Fig.7. The test setup

Tests of the serial output

- *The measured eye-diagrams at 4 Gbps and 4.8 Gbps are very clear (refer to Fig.9).*
- *The total current of the die is 84 mA, which is 6 mA higher than the post-simulation value, attributed to the driver.*
- *The comprehensive results indicate that the architectures have been confirmed, and the designs satisfy the data rate and power consumption requirements of the CEPC vertex detector readout R&D project.*

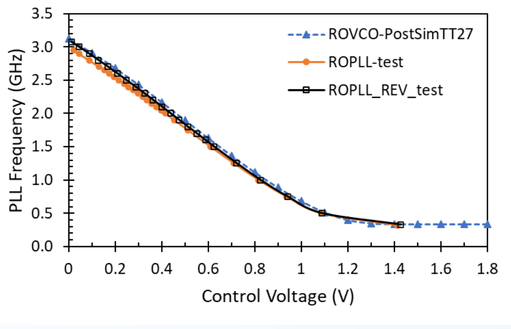

Fig.8. Tests of the frequency locking range of the RO-PLL @1.8V

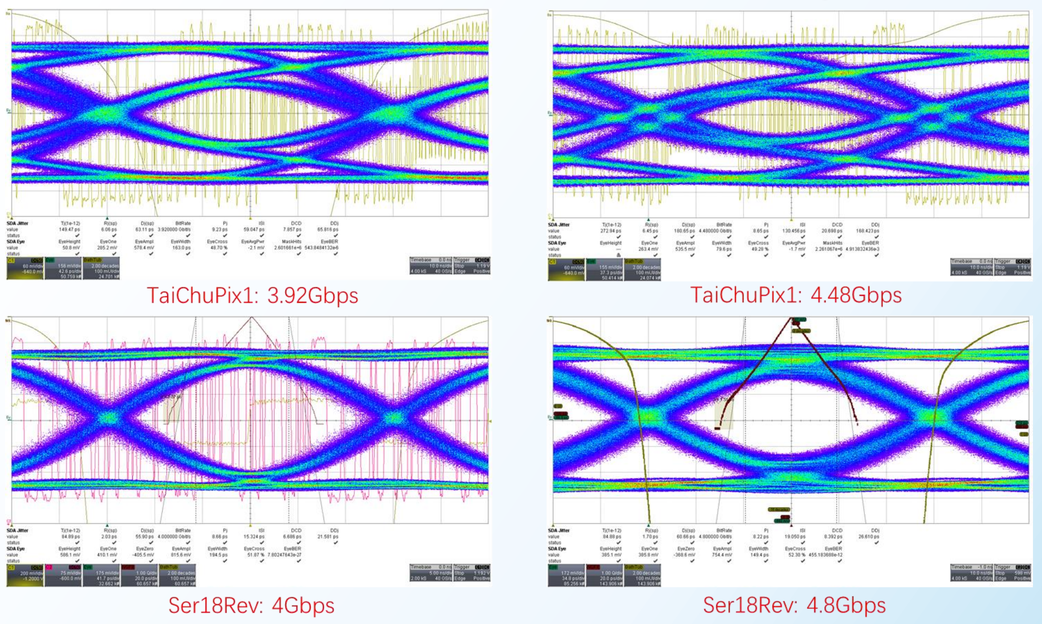

Fig.9. Eye-diagram comparisons of the TaiChuPix (top) and the revision (bottom)

Conclusion and outlook

The prototype and revision designs confirmed that the seria data transmission rate can exceed 4 Gbps in a 180 nm process node. The internal CMOS transmission timing sequence supports data rates up to 4.8 Gbps at least; however, the driving capability probably requires enhancement. Additionally, we are continuing our efforts to correct the prototype chip using FIB to facilitate further debugging and measurements, despite the yield of the FIB approach being only 50%. Next, the CEPC vertex detector R&D for the readout electronics will transition to a 65 nm technology, aiming for a spatial resolution better than 3 μm and lower power consumption. Our current design schemes and experiences will serve as valuable references.

Acknowledgements

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