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Development of high-speed serializer transmitters in 180 nm technology for CEPC vertex detector readout electronics

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he TaichuPix chip, a dedicated monolithic pixel sensor for the CEPC vertex detector R&D, demands a raw data rate up to 3.84Gbps and power consumption of less than 25mA/Gbps for the serializer circuit. The TaichuPix1 achieved a maximum data rate of 3.36Gbps with large jitter and current. Subsequently, two 4Gbps serializers were developed and optimized to meet the requirements. Despite encountering a biasing issue, test results indicate that the RMS jitter of both PLL clocks is less than 1.2ps. A revision has been implemented to address the biasing issue and is ready for testing. Updated test results will be presented.

Summary (500 words)

Monolithic Active Pixel Sensor is one of the promising candidates for the Circular Electron Positron Collider Vertex detector, due to its good performance and trade-off of granularity, readout speed, material budgets and power consumption. A full-scale TaichuPix chip, including a matrix of 512 × 1024 pixels with a size of 25 × 25 μm2 is developed to provide a spatial resolution better than 5 μm. It requires a raw data rate up to 3.84 Gbps and power consumption less than 100 mA for the serializer circuit. Based on one of the small-scale prototypes, the highest serial data rate is tested to be 3.36 Gbps with a peak-to-peak jitter of about 150 ps and large current consumption. Moreover, the 32-bit parallel data width of the serializer isn't suitable for the 8B10B encoder. Therefore, two 4-Gbps serializers have been designed and optimized to meet these requirements based on the same process node of 180 nm as the TaichuPix, considering the funding and time costs. The serializer consists of a phase locked loop (PLL), several 5:1 sub-multiplexers based on a shift-register chain, a 4:1 or 8:1 sub-multiplexer based on the binary-tree structure, a clock distributor and a high-speed driver. Both ring-oscillating PLL and LC-tank PLL were integrated for performance evaluation.

The preliminary tests showed that the RO-PLL exhibited low jitter characteristics, while the LC-PLL showed better jitter performance despite encountering a biasing issue. With the power supply set to 2.6 V, the total current of the high-speed driver increased to about 27 mA (compared to the design value of about 31 mA). This produced a distinguishable 200 mV differential serial signal, and both serializer circuits operated correctly at a data rate of 4 Gbps. The measured eye height and width are about 150 mV and 0.7288 UI (unit interval), respectively. The total jitter measured 145.2 ps, consisting of approximately 8.8 ps of random jitter and 21 ps of deterministic jitter.

The discovery of unusually low measured current, coupled with issues related to the LC-VCO and other random phenomena, allowed us to identify the problem within the biasing circuit which was used in the LC-VCO and CML drivers. Subsequent simulations successfully reproduced start-up anomalies. A revision has rectified the issue and will be tested very soon. Based on the current-stage measurements and analysis, the target of 4 Gbps data rate with 85 ps total jitter looks highly achievable. Further detailed testing and analysis will be presented.

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