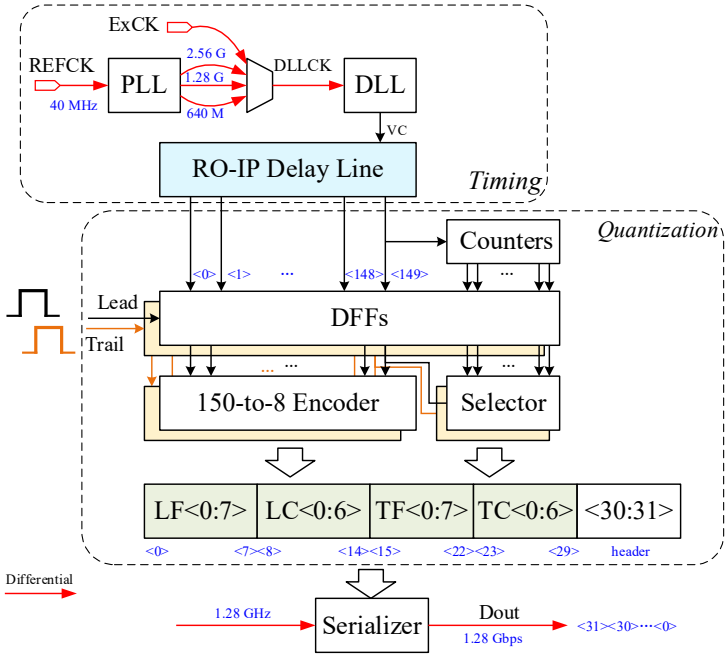

Figure 1. Prototype architecture of the timing block and its digitized readout

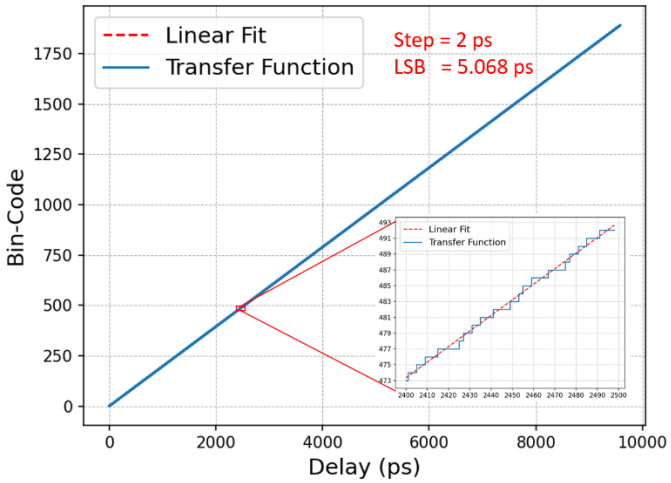

Figure 2. Simulated transfer function of the timing circuit (partial range: 0~9.6 ns)