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A ring-oscillator-based 5.2 ps bin-size timing circuit for time measurement applications in high-energy physics experiments

Accurate time measurement is essential for future high-energy physics experiments, such as Calorimeters and Time of Flight detectors of the Circular Electron Positron Collider (CEPC). The advancement of detector performance necessitates the need of high-resolution timing circuits. We introduce a ring-oscillator based timing block controlled by a delay locked loop, employing passive interpolation techniques, achieving an average bin-size as low as 5.2 ps in a 55 nm process. The core power consumption is estimated to be less than 30 mW. The prototype design will be submitted soon, and the architecture, key circuits and simulation results will be presented.

Summary (500 words)

The high-resolution timing circuit serves as a critical component in time measurement electronics. The prototype timing circuit uses a ring-oscillator-based (RO) delay line and passive interpolation to achieve picosecond time resolution. Fig.1 shows the overall architecture. To ensure high resolution, a combination of techniques is employed, including the use of differential delay cells and clock transmission for improved noise resistance, a low-jitter phase-locked loop (PLL) to generate high-quality clocks, and a delay locked loop (DLL) to mitigate the effects of process voltage and temperature variations (PVT). Both the DLL and RO delay line incorporate a similar voltage-controlled delay line (VCDL) comprising 15 delay cells, and the latter controlled by a VC signal should exhibit the same unit delays. Consequently, the oscillating frequency is approximately half of the DLL clock. The PLL provides three selectable differential clocks to the DLL, with an external clock option also available. Operating at 2.56 GHz, the DLL theoretically generates time intervals of approximately 26 ps, assuming the static phase error is zero. Subsequently, the interpolator subdivides the 26 ps interval into smaller bin-sizes of about 5.2 ps.

In order to characterize the timing performance, a digitized circuit is designed to realize a quantitative function and serial readout. In the quantization stage, two groups of d-flip-flop registers are connected to 150 fine-time phases and coarse counters, triggered by an event pulse which is split into Lead and Trail signals. The difference in delay between two rising edges represents the pulse width. By tuning the delay with a step smaller than a bin-size, an input-output transfer function can be obtained (see Fig. 2). Additionally, calibrations can be achieved by setting the Lead or Trail to a fixed cycle. To address the metastability issue caused by asynchronous event signals, two 7-bit synchronous counters (1.28 GHz) with a nominal range of 100 ns are used. Subsequently, parallel data is serialized and output at a nominal data rate of 1.28 Gbps. The functionality of the serializer can be verified using an integrated pseudo-random binary sequence (PRBS7) generator.

The PLL has previously undergone submission, with a measured RMS jitter of less than 460 fs. The overall circuit will be submitted soon with detailed design and analysis to be presented.

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