FLAXE, a SoC readout ASIC for electromagnetic calorimeter at LUXE experiment

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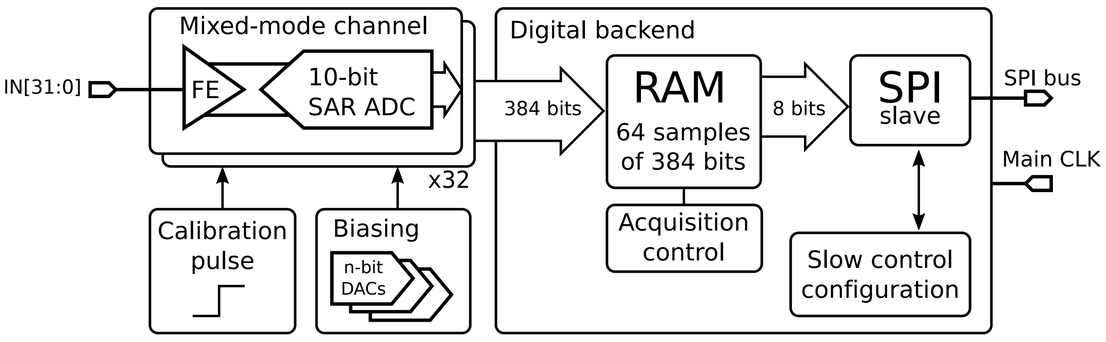
FLAXE design

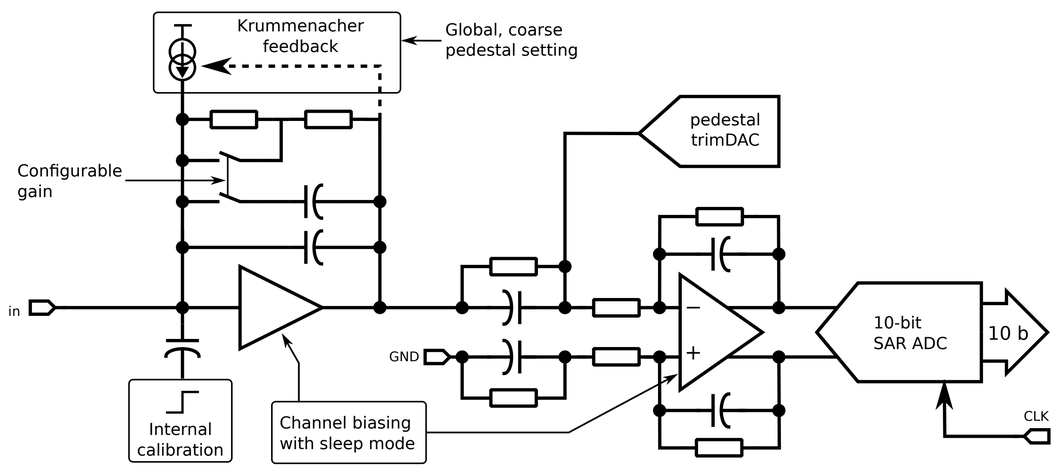


Main features:

- 130 nm CMOS technology
- 32 readout channels
- Internal DAQ RAM
- Complete SoC with biasing and calibration circuitry
- $\leq$ 50 Mbps SPI bus for data and configuration

- LUXE experiment will have a very low bunch crossing rate of 10 BX/s due to the laser charging time
- 64 consecutive data samples from all channels collected in internal memory for each bunch crossing and are read out via SPI protocol between bunch crossings
- Analogue and mixed-mode domain put in sleep mode between bunch crossings to save power

Mixed mode channel

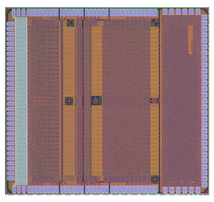


Channel components:

- Preamplifier with two configurable gains
- Fully differential CR-RC shaper, 50 ns peaking time
- 10-bit SAR ADC working nominally at 20 MSps
- Internal calibration
- Sleep mode for power saving
- Coarse (global) and fine (per channel) pedestal settings

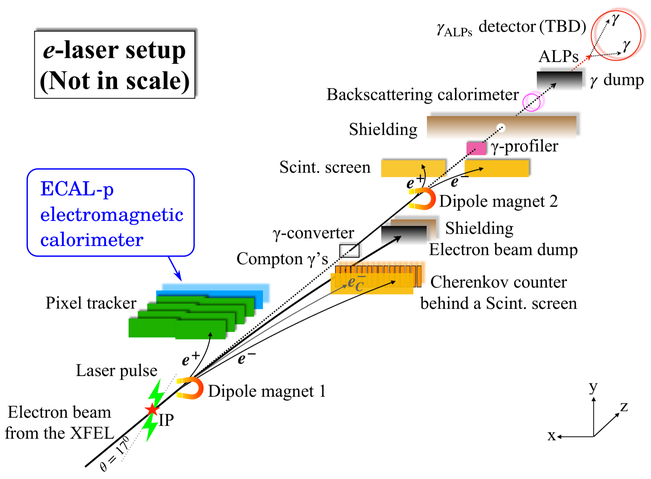
Production and yield

- Design sent for engineering run last year. First batch of 142 ASICs packaged and tested mid-2024
- Fabrication failed with catastrophic yield of 5%, most likely due to the manufacturing problems
- 35% of the ASICs have shorts in at least one power supply domain
- 54% of the ASICs have extremely large (>10x) power consumption affecting blocks performance

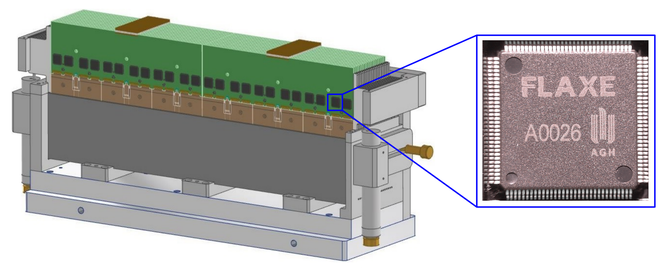


LUXE experiment

The LUXE experiment is proposed at DESY and the European XFEL in Hamburg and Schenefeld, Germany. It is designed to explore the strong-field QED regime in collisions of high-intensity optical laser with either the 16.5 GeV electron beam of the XFEL directly (e-laser setup), or the high-energy secondary photons produced from it (γ-laser setup).



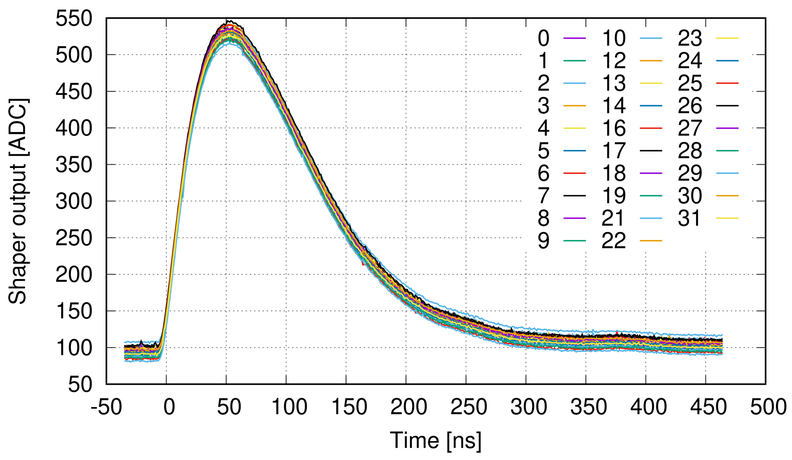
ECALp calorimeter



- Compact sampling ("sandwich") calorimeter
- 16-20 layers of 3.5 mm (1 X_0) tungsten plates with only 1 mm gap for silicon sensors
- Small Molière radius thanks to compact design
- 6 sensors per layer, 256 pads per sensor, each pad 5x5 mm^2
- 1536 channels (48 ASICs) per layer
- 24.5k-30k channels (768-960 ASICs) in total

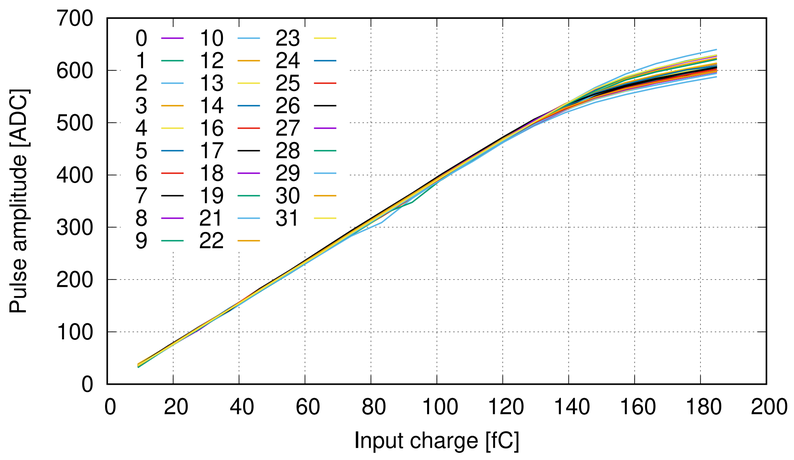
Single ASIC measurement results for C_{in} = 30pF

Pulse shape



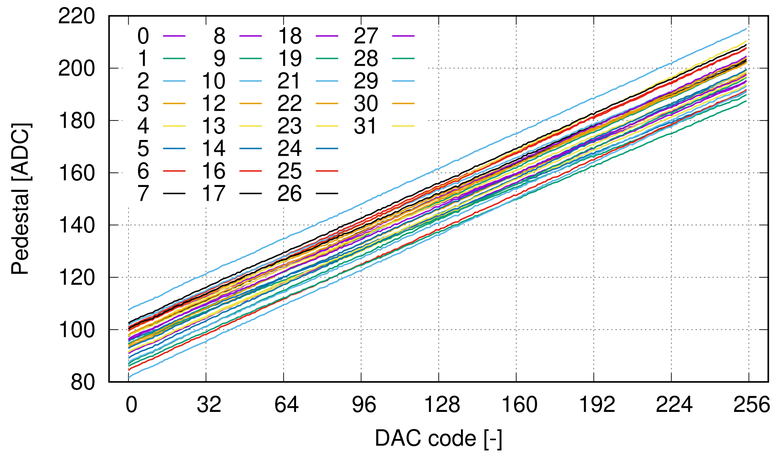
Pulse shape as expected with <5% DNL to ideal CR-RC

Linearity – high gain mode



Linear dynamic range in high gain up to 150 fC

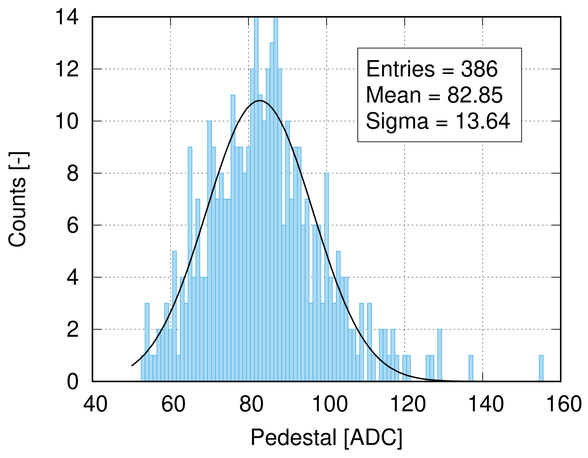
Channel trimDACs



TrimDAC range sufficient to cover the pedestal spread

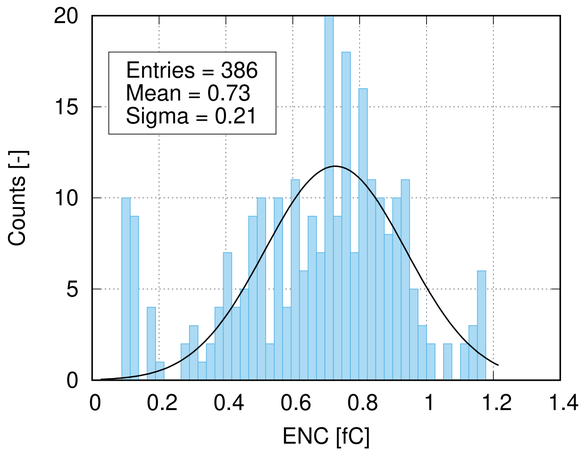
Statistical spread of FLAXE parameters (preliminary) for C_{in} = 30pF

Pedestal spread



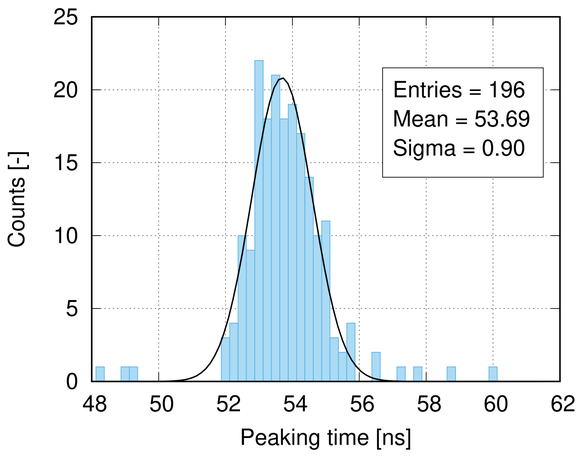
Nominal value and spread as expected

Channel noise



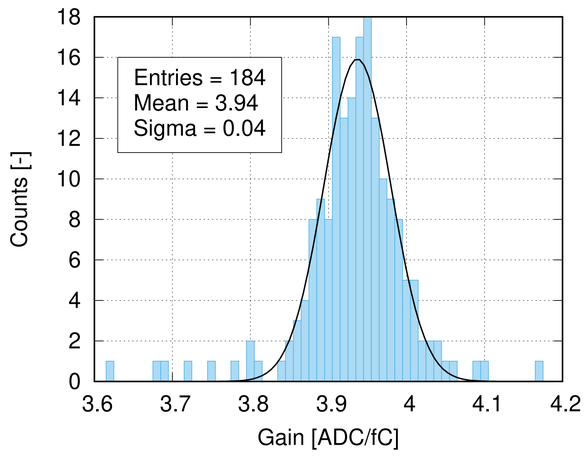
Setup not optimized for noise measurement

Peaking time



Peaking time 7% larger than designed 50 ns

Front-end gain



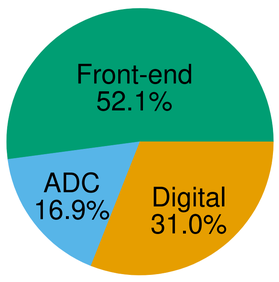
Gain as expected from design (4 ADC/fC)

Power consumption

Total: **71 mW (2.2 mW/channel)**

- Front-end: 37 mW (1.2 mW/channel)
- ADC: 12 mW (375 μW/channel)
- Digital: 22 mW (690 μW/channel)

Sleep mode disabled. Only ASICs without extreme over-current taken into account.



Summary

- SoC readout ASIC for ECALp calorimeter at LUXE experiment designed, fabricated and tested
- Fabrication problem resulted in catastrophic yield of 5% leaving only 7 working ASICs, with only 20–30 functional analogue channels in each
- Characterization of the working ASICs shows that all results are well within specifications
- Design should be sent once again for engineering run at the end of this year

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