CPROC: A RISC-V processor demonstrator for monitoring and data processing in HEP

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Abstract

In High Energy Physics, ASICs are becoming more and more complex with the integration of many digital processing and monitoring structures. The next generation of System-On-Chips will require reprogrammable logic to let the user change the ASIC behavior after its fabrication.
CPROC (Central Processing ReadOut Chip) is a processor demonstrator based on the RISC-V Instruction Set Architecture. It will open the era of FPGASIC with a user-defined program executed by the embedded processor. The CPROC chip was received in May 2024: an introduction to RISC-V, architectural choice and capabilities will be presented.
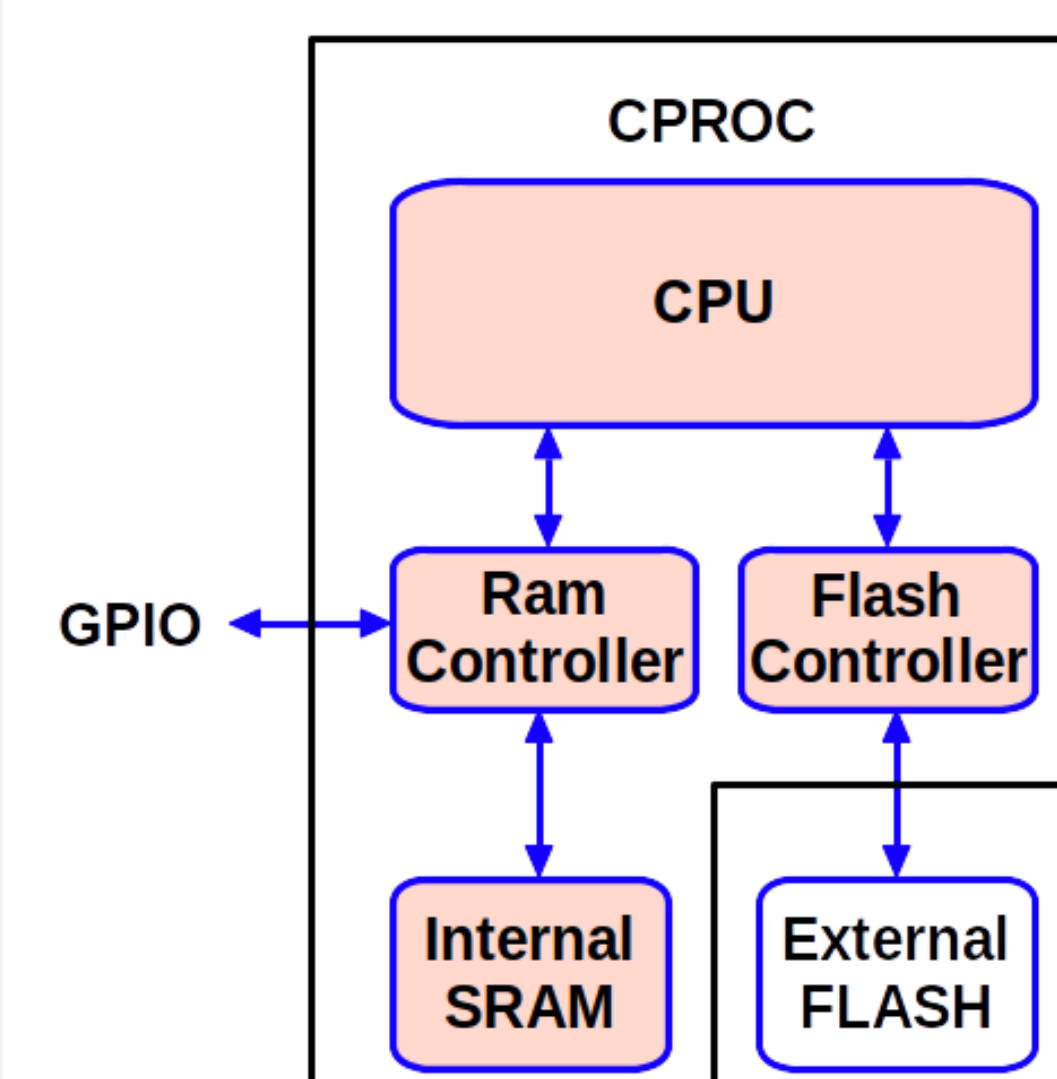
CPROC Layout
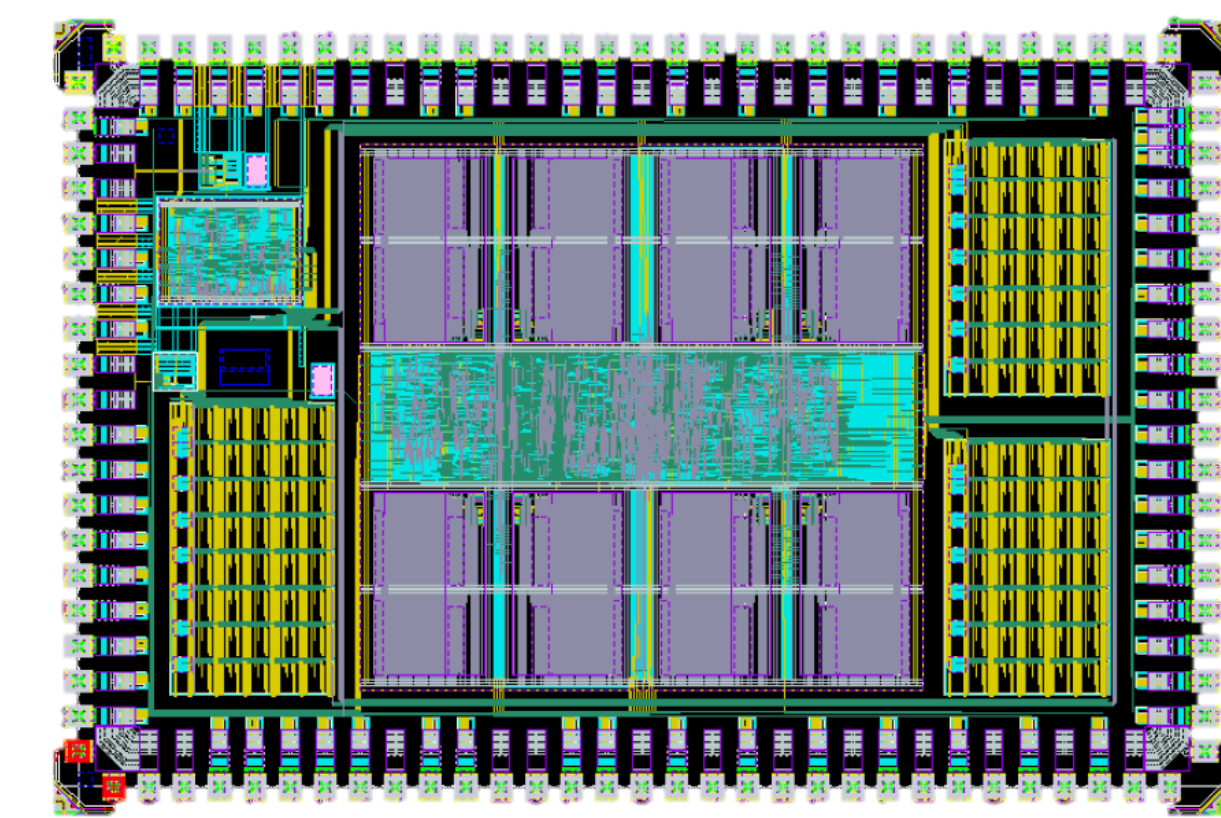
CPROC Architecture
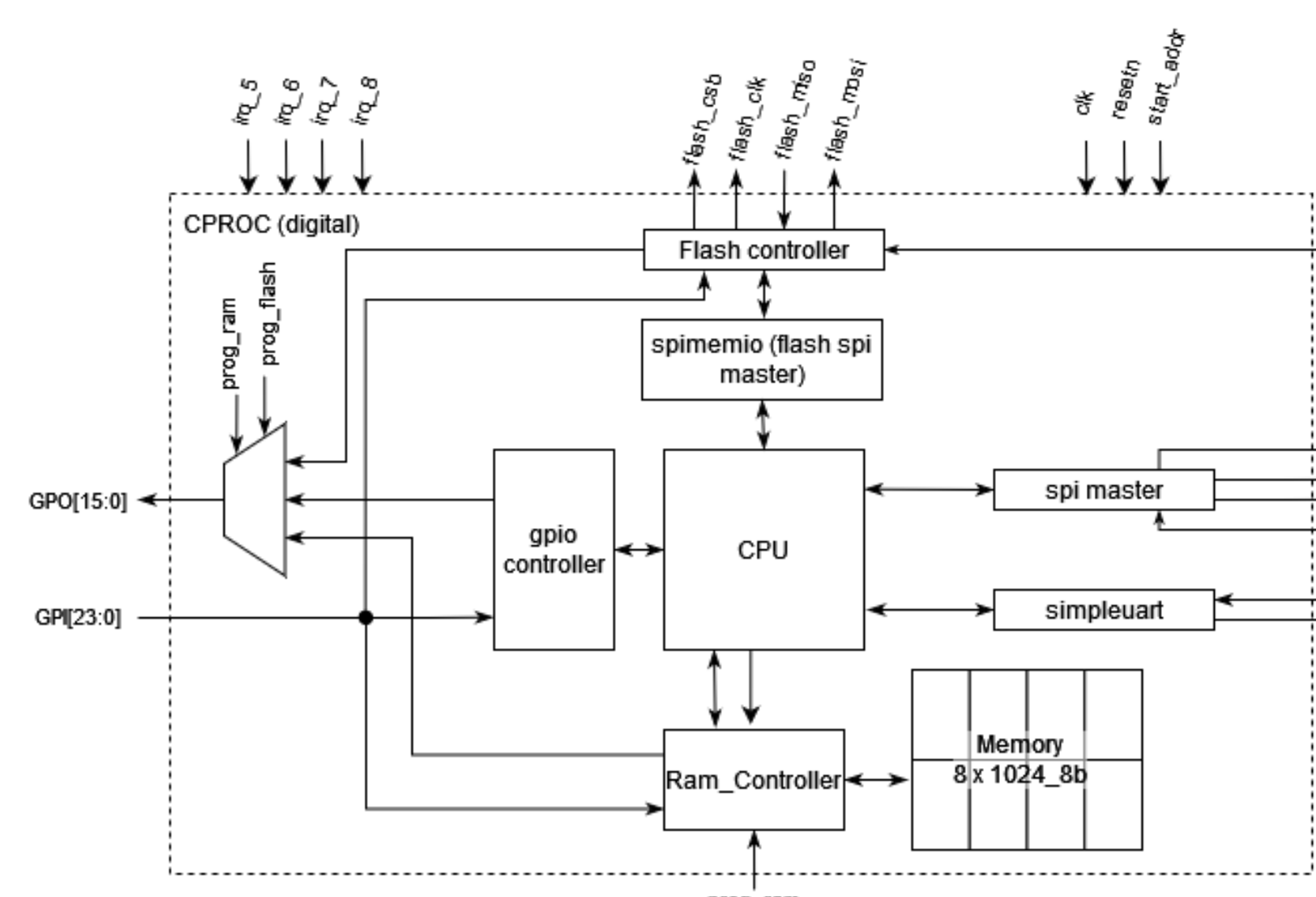
- ASIC designed in 130nm CMOS technology (1.2V)
- Packaged in a BGA 196 pins with pitch 0.8mm
- Single core CPU (PicoRV32), RV32EC ISA, 40MHz
- Internal 8 Kb SRAM (2048 words x 32 bits)
- External flash support
- General Purpose Inputs (24) / Outputs (16)
- I2C, SPI and UART connection
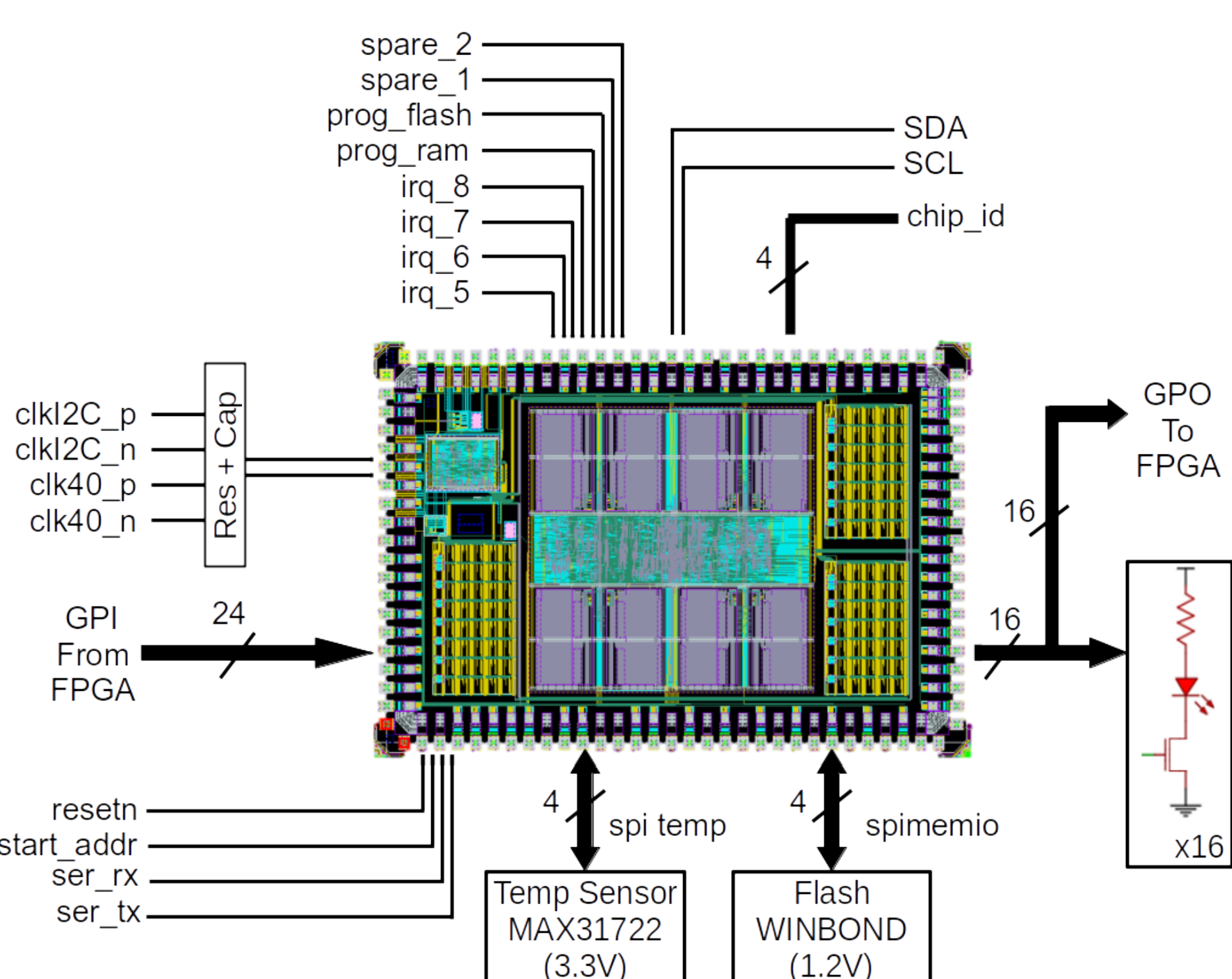- 4 programmable IRQs

CPROC Memory Management

- Internal SRAM is a radiation hardened memory
- 2 starting address choice:
  - SRAM or External FLASH
- Programming through GPIO
- 3 programming modes available:
  - RAM programming
  - FLASH programming
  - Start pointer

Test Board

- CPROC motherboard detail:

- Connection to a Xilinx FPGA board KCU105
- Temperature sensor for CPROC SPI master tests
- Winbond 64Mb 1.2V serial flash (external memory)
- 40 GPIO connected to KCU105
- Led chaser to validate tests on CPROC modules
- One IRQ can be tested as a GPIO
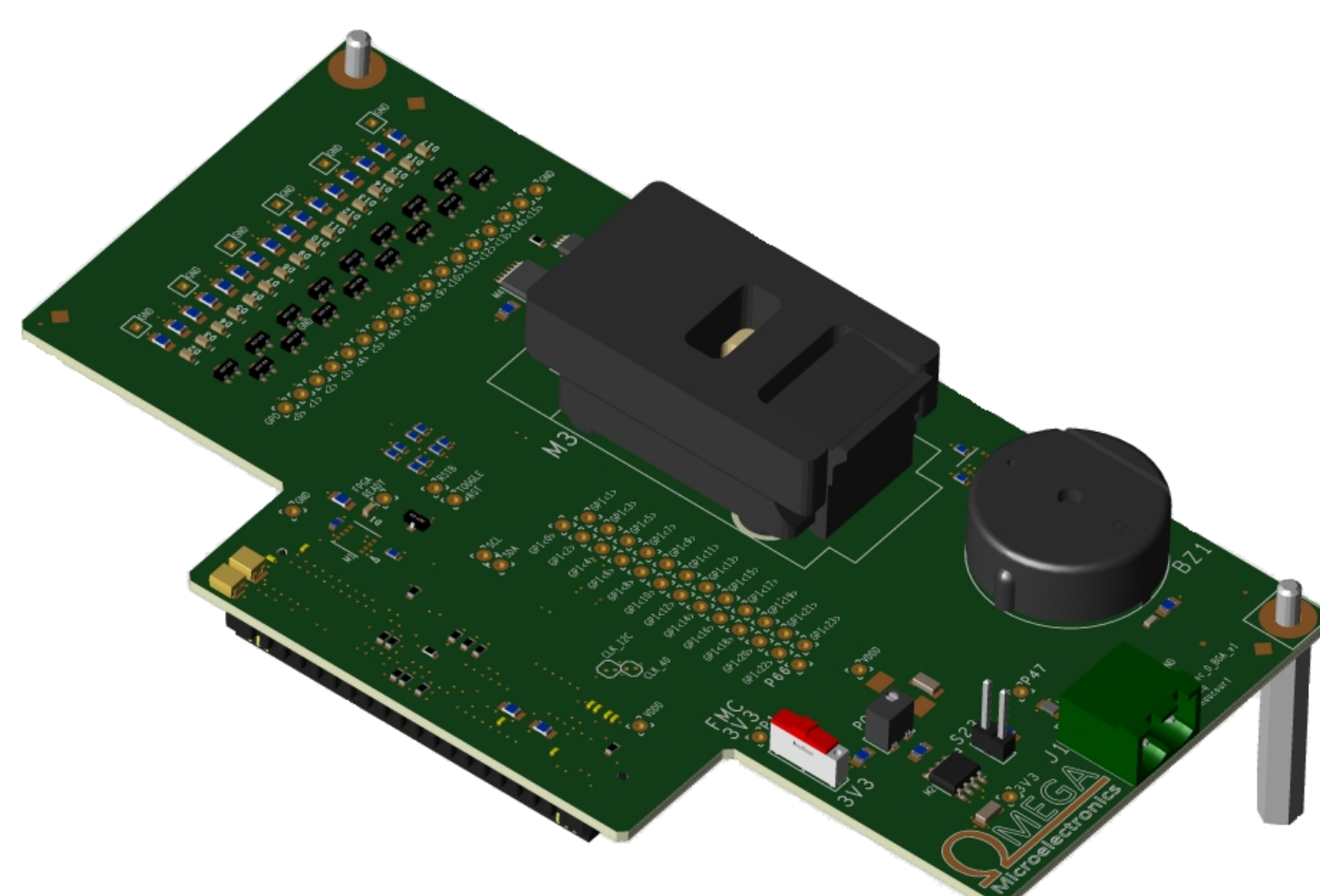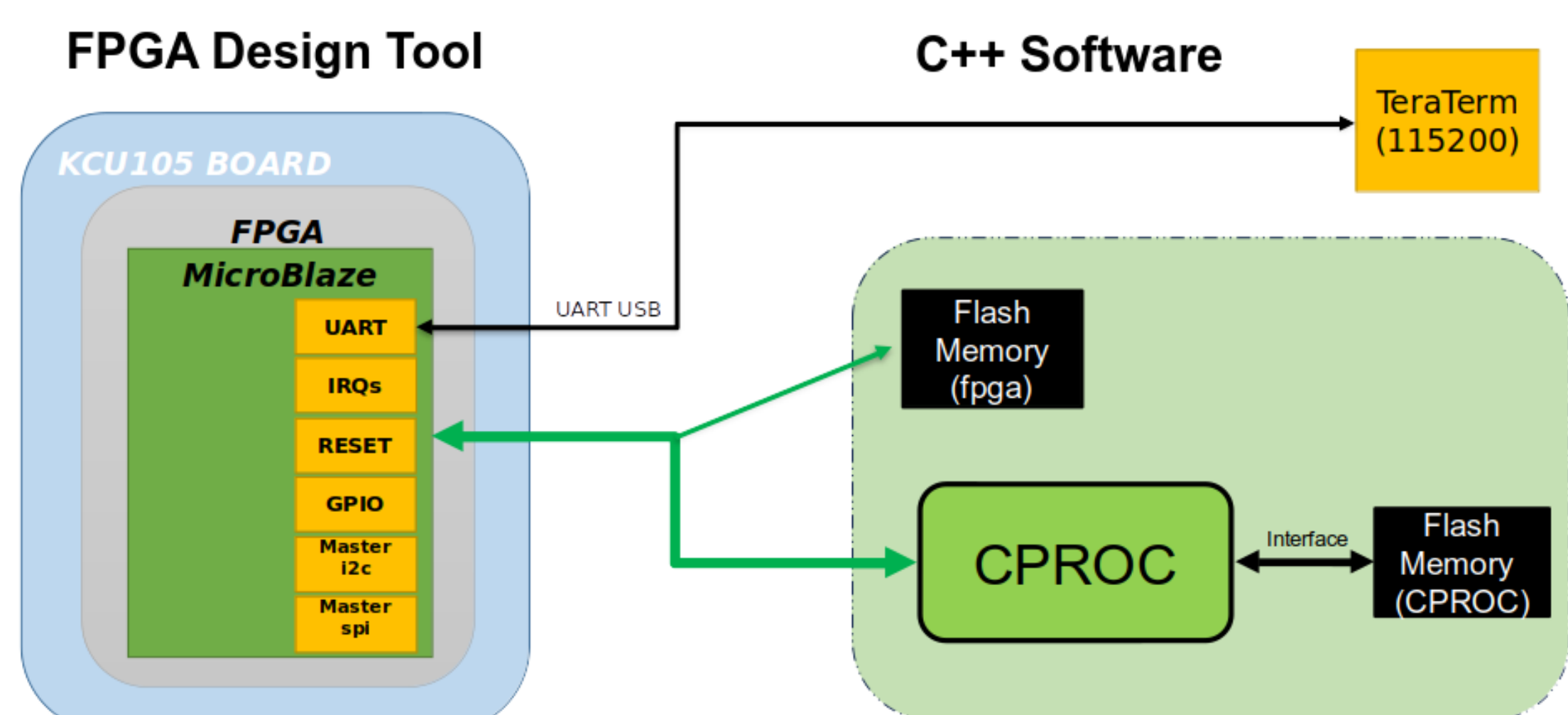
CPROC test board

CPROC Tests

- Examples of tests used to validate CPROC functions and configuration:
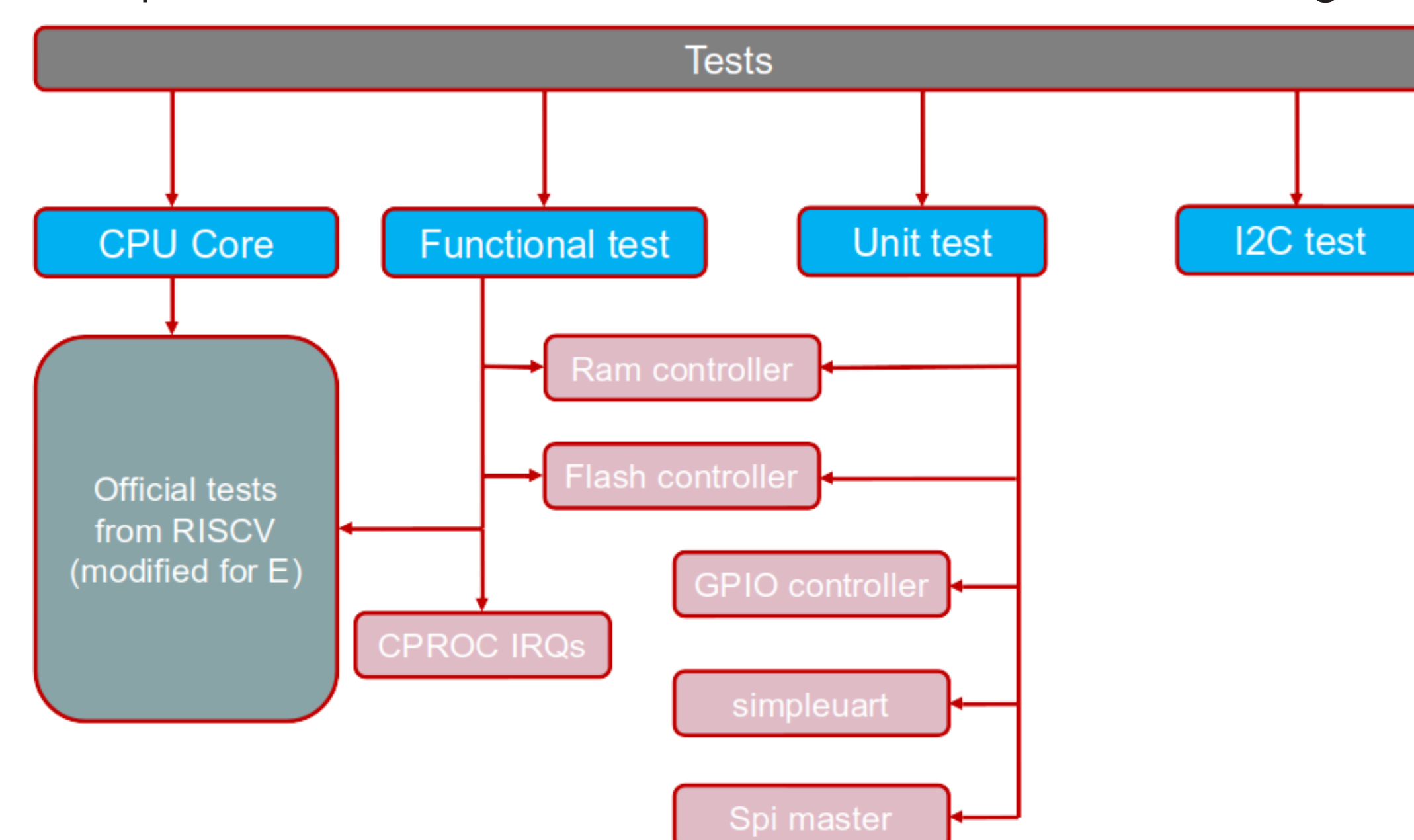
- Firmware tests:
  - Demonstrator
  - GPIO
  - Flash control test
- CPROC RISC-V tests:
  - Program/Verify Ram
  - Program/Verify Flash
  - Enable IRQ
- I2C tests:
  - Read/Write
  - Multi-byte R/W
  - Broadcast tests

Firmware / Software Tests

Firmware schematic tests principle

- Access to SRAM through:
  PC→UART→FPGA board→CPROC→SRAM
- CPU-FPGA connection check led
- Manual testing: starting address choice, write, read, program, verify memories
- Auto test:
  - FLASH: erase all, write all, verify all
  - I2C: write, read from all registers, verify all
  - SRAM: write, read, verify all

CPROC testbench

Measurements / Next Steps

- Power measurements:
  - CPROC idle with clock: 59 mW
  - CPROC normal running: 74 mW
- Working features:
  - All communications protocol (I2C, SPI, UART)
  - All test firmwares (e.g., IRQ, GPIO, Demonstrator)
  - Running program from internal SRAM or external FLASH

- Technology node:
  Transition to a smaller process node (e.g., from 130nm to 65nm) will reduce design size, leading to lower consumption and higher performance. This will also improve SRAM performances.
- Memory improvement:
  - Improve current boot loading via GPIO, in next version the loading will be done via an UART connection to save input/output resources.
  - Embedded flash in the technology node that support integrated non-volatile memory flash, for firmware updates and the needs to store calibration data for physics measurements.