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CPROC, a RISC-V processor demonstrator for monitoring and data processing in HEP

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In High Energy Physics, ASICs are becoming more and more complex with the integration of many digital processing and monitoring structures. The next generation of System-On-Chips will require reprogrammable logic to let the user change the ASIC behavior after its fabrication. CPROC (Central Processing ReadOut Chip) is a processor demonstrator based on the RISC-V Instruction Set Architecture. It will open the era of FPGASIC with a user-defined program executed by the embedded processor. The CPROC chip was received in May 2024: an introduction to RISC-V, architectural choice and capabilities will be presented.

Summary (500 words)

In High Energy Physics, Front-end ASICs are designed to be as versatile as possible. Thus, many parameters are embedded (up to tens of thousand) to tune each internal stage. For the next generation of ASICs, this solution appears to still be relevant for analog and mixed-signal parts but will be insufficient for integrated digital processing or monitoring systems. An embedded processor could be part of the solution if integrated within the ASIC. By loading a specific program, it could change the behavior of some digital parts after the ASIC fabrication: it allows more flexibility in reconfiguring specific tasks.

As we are targeting a processor for mixed-signal ASIC, we have to minimize the impact of adding such new digital component. CPROC is a microcontroller, which embeds a RISC-V processor with its peripherals and general-purpose inputs and outputs. It is designed to have a small area footprint with the capability to run a light embedded program. CPROC is made around an open-source RISC-V 32-bit processor; it integrates an 8 kBytes memory for data and program storage (also known as von Neumann architecture). Its inputs and outputs are used to interact with the testboard and to load the user program into an embedded SRAM or the external FLASH device.

The processor is based on a RISC-V architecture with three standard extensions. The first one reduces the number of internal registers to minimize the area footprint. The second one enables the use of compressed instruction to reduce the size of the user-defined program. In addition, the last one allows the use of multiplication and division for integers.

CPROC integrates an SRAM memory to store the program. Alternatively, an external 64 Mb FLASH is available on the testboard to execute larger programs but at a lower speed. Besides, CPROC embeds an UART interface, an SPI controller and 4 external interruptions to extend the processor capability.

A testboard is being made around a commercial Xilinx KCU105 evaluation board along with a daughter board. It will host CPROC, the FLASH memory, a temperature sensor connected to the ASIC and some LEDs for debugging.

CPROC was received in May 2024 and the first results will be presented. The aim of the presentation is to give a comprehensive view of the RISC-V possibilities, architecture and benefits for HEP projects. Then, the CPROC ASIC will be presented highlighting design choices and how the open-source project has been selected.

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