EICROC: an ASIC to read-out the AC-LGAD sensors for the Electron-Ion Collider (EIC)

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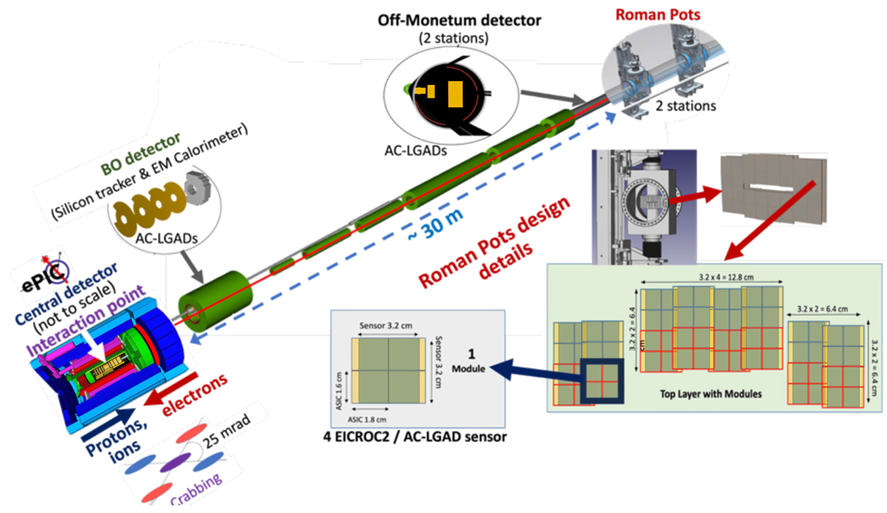
Abstract

An ASIC named EICROC (Electron-Ion Collider Read Out Chip) is designed to read out the AC-LGAD detector for the future EIC accelerator to be built at Brookhaven. These silicon detectors, which appeared just a few years ago, should combine excellent temporal (20-30 ps) and spatial resolution (~20 µm), enabling a new generation of pixel detectors with precise time measurement. Designing an ASIC to read out the AC-LGAD detector represents a significant technological challenge.
The EICROC ASIC is a System on Chip (SoC) that processes the input signals up to digitization. It measures and digitizes the charge and provides a measurement of the Time-of-Arrival (ToA), transmitting these data to the back-end electronics. The first prototype of EICROC in CMOS 130 nm node was submitted in 2022. The ASIC architecture and performance will be presented.

Experiment presentation

The EIC (Electron-Ion Collider) will be a powerful new high-luminosity facility in the United States with the capability to collide high-energy electron beams with high-energy proton and ion beams, providing access to those regions in the nucleon and nuclei where their structure is dominated by gluons (taken from EIC Yellow Report*). The collider is based on RHIC and will be built in Brookhaven, NY.
The EICROC ASIC is placed in the ePIC experiment in the far-forward tracking region. Roman pots with AC-LGAD sensors are used to detect scattered protons and ions at very small angles (up to 5 mrad), which is especially mandatory for exclusive reactions. AC-LGAD sensors are used due to their excellent temporal (20-30 ps) and spatial resolution (~20 µm), which are needed due to the stringent requirements of the experiment.

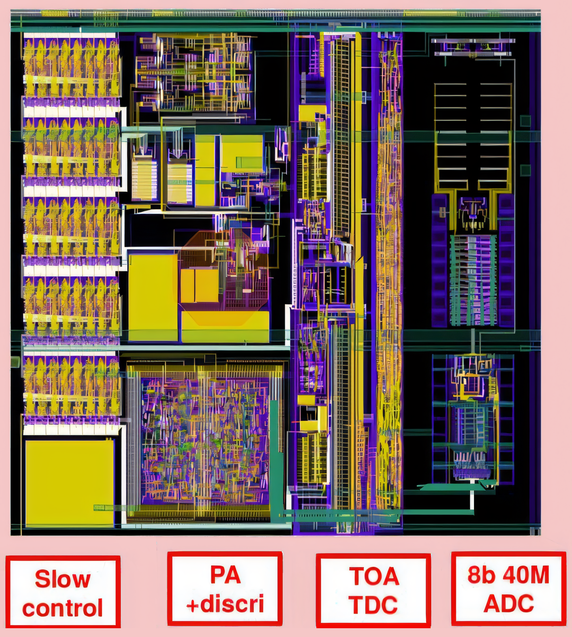


EICROC0 ASIC

4x4 channel AC-LGAD readout ASIC designed for precise charge and timing information

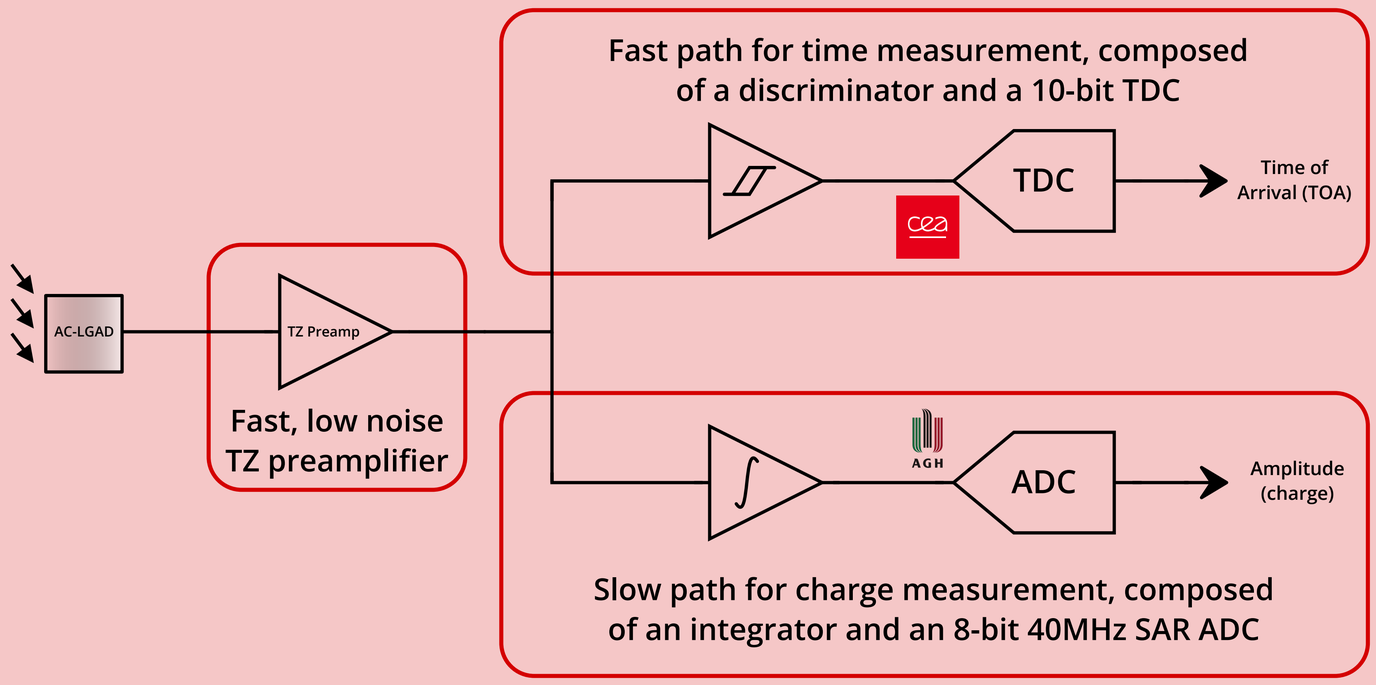
~2mW/channel + 4x20mW « analog probe preamp »

Analog front-end + digital back-end allows to reach desired performance

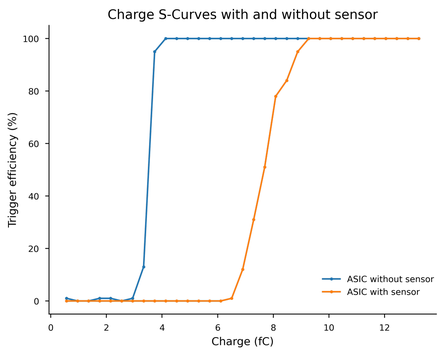


Final EICROC specifications :
- 32x32 pixels / ASIC
- ~1 mW/channel
- Charge detection range 1-50 fC
- Timing jitter ~15-20 ps
- Input capacitance : c_D = 1-5 pF

EICROC0 Channel schematic



Test results are obtained for the following parameters :
- ASIC without sensor : input capacitance of 750 fF and discriminator threshold at 300 DACu
- ASIC with sensor : input capacitance of the AC-LGAD sensor and discriminator threshold at 340 DACu

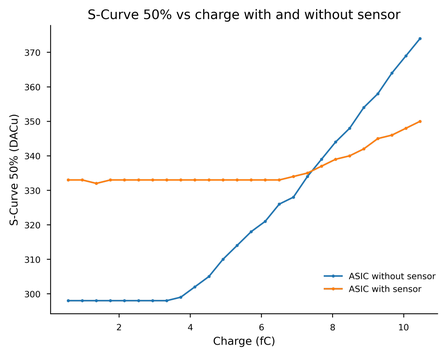


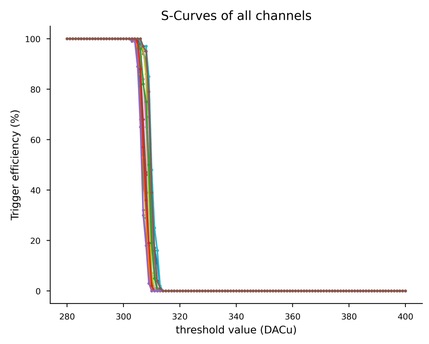
Charge S-Curves are obtained at a specific discriminator threshold value, sweeping the input charge sent to all channels and reading out the hit bits from the ASIC. Results are presented for channel 0.

Results obtained show :

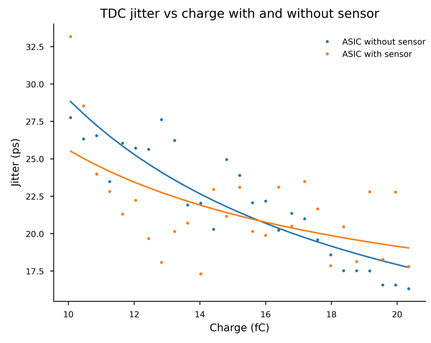
- ASIC without sensor : 3.5 fC min. detected charge with 0.25 fC noise
- ASIC with sensor : 7.65 fC min. detected charge with 0.66 fC noise

The graph below presents the evolution of the 50% of the discriminator threshold S-Curves with respect to the charge. Changes in channel gain are exhibited here.



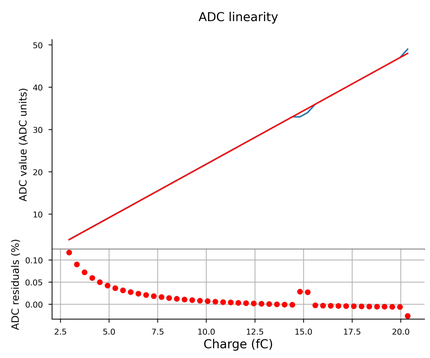


S-Curves are corrected using local internal correction DACs in each channel. By correcting every channel we obtain a discriminator threshold value variation of +/- 2 DACu for the ASIC with and without sensor.
The graph presents corrected S-Curves for the ASIC without sensor.

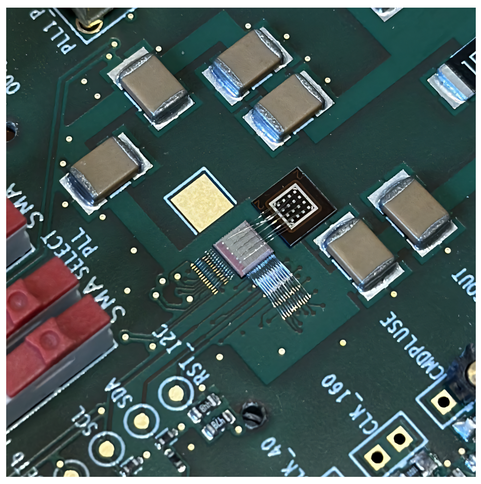


TDC jitter measurements obtained for channel 0 :
- ASIC without sensor :
  - 27.5 ps @ 10 fC
  - 16.5 ps @ 20 fC
- ASIC with sensor :
  - 33 ps @ 10 fC
  - 20 ps @ 20 fC

TDC jitter shows promising performance for medium to high charge values.



The 8 bit 40MHz ADC shows very good linearity and properly digitizes the signal amplitude.
Residuals are around 0.1% for the charge range.
Performance is presented for the ASIC with sensor accross the entire charge injection range.



Conclusion & perspectives

EICROC0 measurement summary		
Measurement	**No sensor**	**With sensor**
Min. detected charge	3.5 fC	7.65 fC
Noise	0.26 fC	0.66 fC
TDC jitter at 10 fC	27.5 ps	33 ps
TDC jitter at 20 fC	16.5 ps	20 ps

EICROC0 is a testbeam prototype used for sensor characterization with pixelated AC-LGAD sensors. The initial performance of the ASIC alone is promising and will be improved with further iterations.
Future versions will focus on improving the testability of the ASIC, as well as efforts to reduce power consumption by modifying the ADC architecture in a next iteration.

The EICROC1 design will present larger dimensions (8x32) to test for floor planning and power distribution issues.

Both versions will be submitted by the end of 2024.

Reference :
"Science Requirements and Detector Concepts for the Electron-Ion Collider: EIC Yellow Report", Nucl. Phys. A 1026 (2022) 122447. arXiv:2103.05419v3