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EICROC: an ASIC to read-out AC-LGAD sensors for the Electron-Ion Collider (EIC)

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The ASIC EICROC is designed to read out the AC-LGAD detectors for the future EIC at Brookhaven National Laboratory (BNL). These detectors should combine excellent temporal (20 ps) and spatial (20 um) resolution, enabling a new generation of pixel detectors with precise time measurement. Designing an ASIC to read out the AC-LGAD detector represents a significant technological challenge. EICROC measures and digitizes the charge and the Time-of-Arrival (ToA) (25 ps), transmitting these data to the back-end electronics. The first prototype of EICROC was submitted (in CMOS 130 nm node) in 2022. The ASIC architecture and performances will be presented.

Summary (500 words)

The EIC (Electron-Ion Collider) project is driven within an international collaboration and aimed at deepening our understanding of the fundamental structure of matter, in particular gluon contributions. At EIC high energy and highly polarized electrons and protons/ions will collide. Its construction is on-going at BNL and the first collisions are foreseen for mid 2030s.

An evolution from LGAD sensors has been proposed for future EIC detectors requiring high timing and spatial resolutions: AC-LGAD sensors. The EICROC ASIC was designed to read out this new AC-LGAD sensor. This chip is based on the developments performed for the ALTIROC chip, an ASIC designed to read out the LGAD sensor of the ATLAS High-Granularity Timing Detector (HGTD), modified to fulfil EIC requirements.

The first prototype of EICROC was submitted (in CMOS 130 nm node) in 2022 and has been tested in the laboratory. EICROC0 is a system-on-chip with analog and digital processing. It embeds 16 independent channels (4x4) working in a trigger-less fashion.

Each channel of the chip consists of a low-noise input trans-impedance preamplifier followed by two paths: a fast path with a discriminator connected to a 10-bit Time-to-Digital Converter (TDC from CEA IRFU group) for time measurement (ToA) with a 25 ps accuracy; a slow path with shaper connected to an 8-bit 40 MHz successive approximation Analog-to-Digital Converter (SAR ADC from AGH Krakow) for charge measurement. The TDC is only activated when the input signal exceeds a defined threshold. When triggered, an acquisition window opens and data from the ADC, TDC and discriminator are stored and automatically read out.

Each pixel sends parallel digitized data of the ADC and the TOA for each clock cycle (40 MHz). If the window acquisition is active, the pixel stores this data into a circular buffer with a depth of 8. When a read-out signal is applied, the stored pixel data are daisy-chained and read out through a single output. The architecture and performances of the first prototype of the ASIC will be presented. The second version of the prototype is currently under design. Improvements and motivations for this second version will also be presented.

Authors: Mr VERPLANCKE, Adrien (OMEGA-CNRS); Dr TORRENTO COELLO, Ana (Université Paris-Saclay (FR)); Mr KY, Beng-Yun (Université Paris-Saclay, CNRS/IN2P3, IJCLab); Mr MUNOZ CAMACHO, Carlos (Université Paris-Saclay, CNRS/IN2P3, IJCLab); Dr DE LA TAILLE, Christophe (OMEGA (FR)); Mr THIENPONT, Damien (OMEGA - Ecole Polytechnique - CNRS/IN2P3); Dr MARCHAND, Dominique (Université Paris-Saclay,

CNRS/IN2P3, IJCLab); Mr BOUYJOU, Florent (CEA IRFU - Université Paris-Saclay (FR)); Mr DULUCQ, Frederic (OMEGA - Ecole Polytechnique - CNRS/IN2P3); MORON, Jakub (AGH University of Krakow (PL)); SERIN, Laurent (IJCLab-CNRS/IN2P3 Orsay(Fr)); IDZIK, Marek (AGH University of Science and Technology (PL)); SEGUIN--MOREAU, Nathalie (OMEGA - Ecole Polytechnique - CNRS/IN2P3); EXTIER, Sebastien (OMEGA (FR)); CONFORTI DI LORENZO, Selma (OMEGA (FR))

Presenter: Mr VERPLANCKE, Adrien (OMEGA-CNRS)

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