[1] University of Bergamo
Department of Engineering
and Applied Sciences
Dalmine (BG), Italy

[2] University of Pavia,
Department of Electrical, Computer
and Biomedical Engineering,
Pavia, Italy

A Time-over-Threshold asynchronous front-end in 28 nm CMOS for the readout of pixel detectors in extreme radiation environments

[3] INFN Sezione di Pavia
[4] INFN Sezione di Bologna
[5] INFN Sezione di Milano

L. Gaioni[1,3], A. Galliani[1,3], L. Ratti[2,3], V. Re[1,3], G. Traversi[1,3], D. Falchieri[4], L. Frontini[5] and A. Stabile[5]

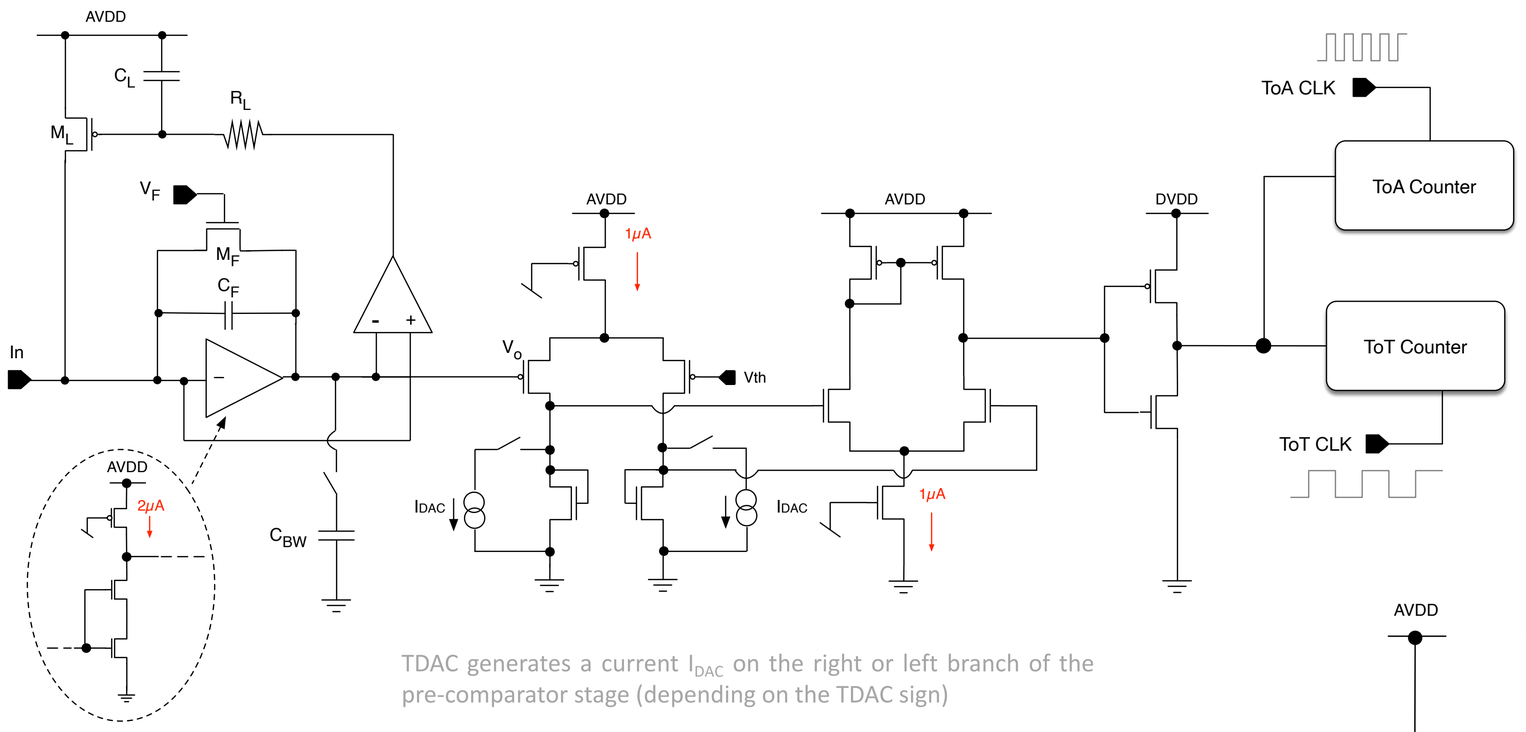
PRIN PiHEX project

TWEPP 2024 - Topical Workshop on Electronics for Particle Physics 2024, 30 September - 4 October 2024, Glasgow, Scotland

Introduction

Advanced pixel readout chips have been developed by the CERN **RD53 collaboration** with a **65 nm** CMOS technology. These chips have successfully met the stringent performance requirements of the **ATLAS and CMS pixel detectors** at the High-Luminosity Large Hadron Collider (HL-LHC). Looking towards future developments, the high-energy physics (HEP) microelectronics community is now focusing on the **28 nm CMOS technology**. The work presented here addresses the design of analog front-end circuits for future, high-rate pixel detectors based on the 28 nm process. Specifically, this research is part of the **PRIN PiHEX project** (funded by the Italian Ministry of University and Research), which represents a natural continuation of the **INFN Falaphel project**. Building upon the progress achieved in the latter, in particular in the field of radiation-hard electronics, PiHEX aims to further advance the state-of-the-art in pixel readout chip technology for high-luminosity colliders and next-generation X-ray imagers.

The analog front-end

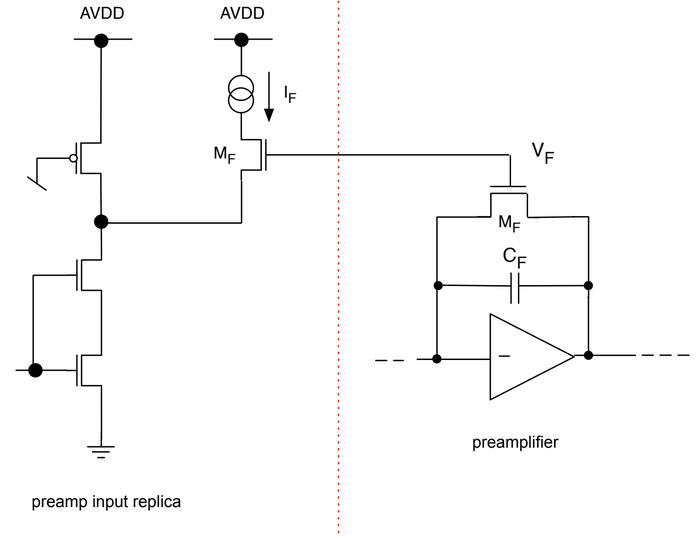


TDAC generates a current I_{DAC} on the right or left branch of the pre-comparator stage (depending on the TDAC sign)

- **preamplifier** with detector leakage compensation circuit
- preamp **bandwidth** can be limited by loading its output with a 20 fF MoM capacitor (C_{BW})
- 5-bit (+ 1 bit sign) threshold **tuning DAC** (TDAC)
- differential input pair loaded with diode connected transistors → **single-ended to differenti**al signal conversion (to improve the immunity to interferences)

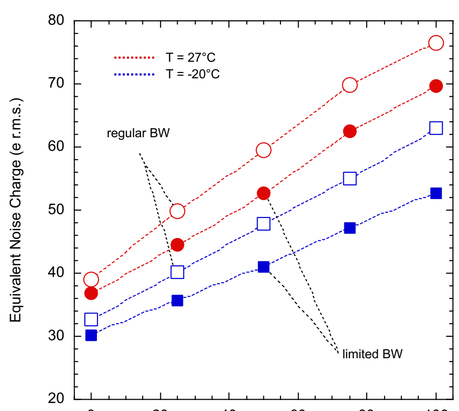
- standard differential pair with active load + output inverter
- **Time-over-Threshold** counter for A/D conversion of the signal
- **Time-of-Arrival** counter for time-walk measurements

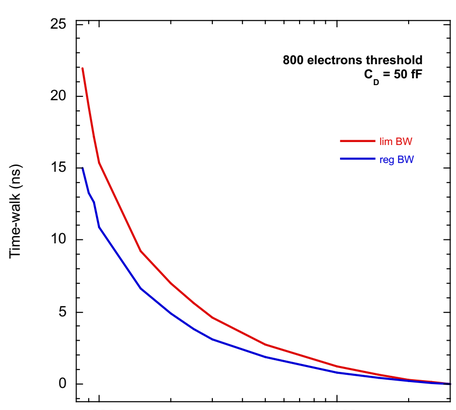
- The **VF** reference voltage is provided to the gate of MF to **regulate discharge** of the preamp feedback capacitance
- A solution has been proposed which makes the architecture robust against **process and temperature variations**

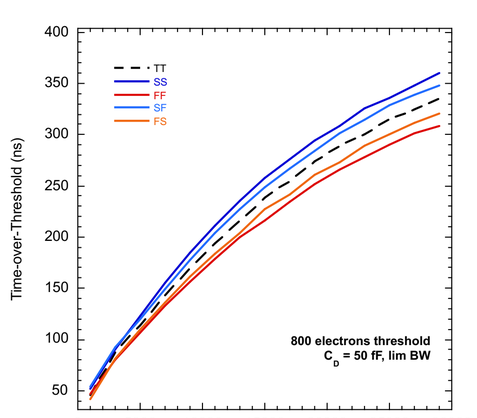


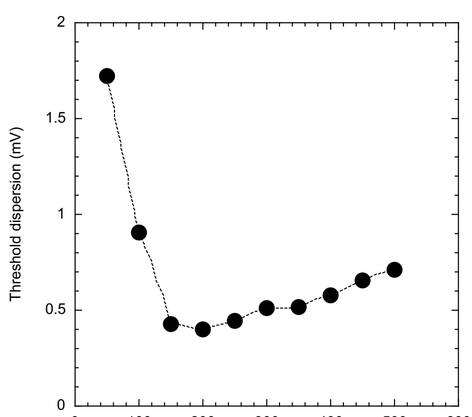
can possibly be distributed along matrix columns (1 every *n* pixels) to compensate for IR drops

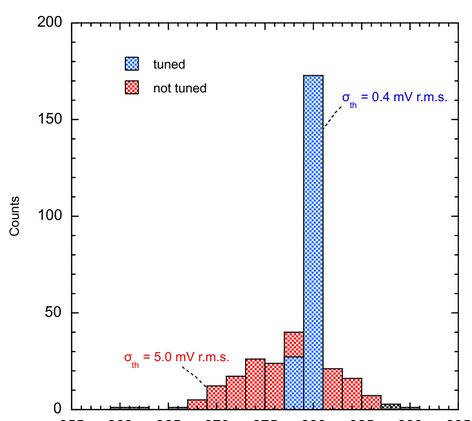
Main simulation results





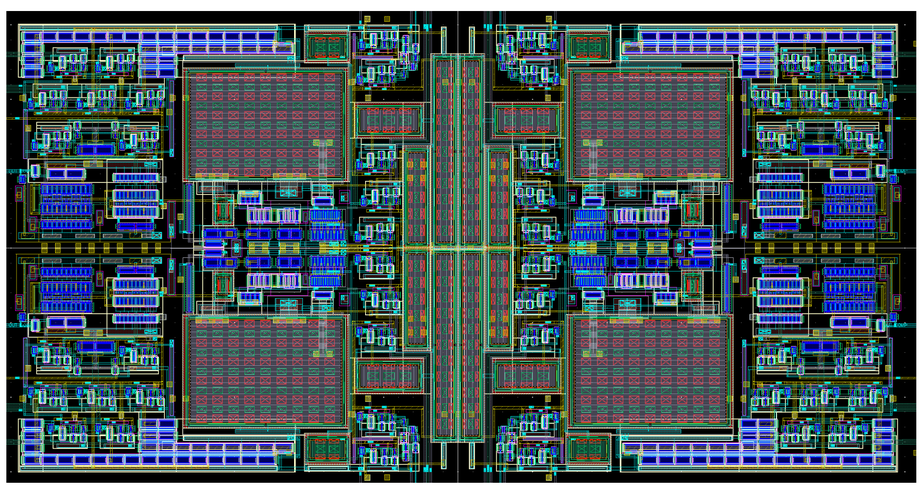






- **ENC** as a function of detector cap for regular and limited preamp BW (room T and -20°C)
- **Time walk < 15 ns** for the regular BW version
- **ToT** as a function of the input charge (~linear up to 12 ke$^-$) in a four corners simulation
- Optimum Threshold dispersion of 0.4 mV (~**16 e r.m.s.**) @ I_{DAC} = 200

Analog macro and chip layout



- **Analog island** arrangement (2x2 pixels)
- Analog macro size → **30 x 17 µm²**

- **8x32 matrix** of readout channels (100 x 25 µm² pixels)
- Shared 8-bit **Time of Arrival Counter** (640 MHz)
- Shared 5-bit **Time-over-Threshold** Counter (40 MHz)
- SPI controller
- 1.7 x 1.5 mm² **prototype chip** submitted in July 2024