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A Time-over-Threshold asynchronous front-end in 28 nm CMOS for the readout of pixel detectors in extreme radiation environments

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This work describes the design, in a 28 nm CMOS technology, of a front-end channel for the readout of pixel sensors in future particle accelerators. The channel being developed leverages the Time-Over-Threshold technique for the numerical conversion of the detector signal amplitude, and includes a low-noise charge sensitive amplifier featuring a compact gain stage architecture. A prototype chip including a matrix of 8x32 readout channels is going to be submitted in Q3-2024. Simulation results for the front-end channel, together with a discussion of the integration of the matrix, are reported in the conference paper

Summary (500 words)

In the realm of electronic circuits for high energy physics experiments, the 28 nm CMOS technology is emerging as a key enabler for the development of instrumentation in the next generation particle colliders. Such a process has been demonstrated to withstand, with rather marginal performance losses, total ionizing doses of the order of 1 Grad(SiO2). With respect to the 65 nm process, which represents the technology choice for the ASICs designed by the RD53 collaboration for the phase-II upgrades of the ATLAS and CMS experiments, the 28 nm node makes it possible to develop more compact digital readout logic that can be ultimately packed into smaller pixel cells. On the other hand, the design of analog circuits in the 28 nm node can be challenging: one of the main reasons for this is related to the supply voltage of the technology, which is limited to 0.9 V. Such a constraint significantly limits the number of architectures that can be implemented in the design of high-gain stages, which are the core of basic analog building blocks such as charge sensitive amplifiers and threshold discriminators. Moreover, the 28 nm CMOS technology leverages resolution enhancement techniques such as Phase-Shifting Masks, which force a number of layout restrictions - including the usage of two dummy gates per transistor side, required for lithography and planarization, as well as maintaining a uniform component orientation throughout the silicon wafer.

This work discusses the development of a front-end circuit being designed in the framework of the INFN Falaphel project and the PiHEX project, funded by the Italian Ministry of University and Research. These projects share the developments of rad-hard, front-end electronics to be operated in harsh radiation environments, such as the one at the hadronic Future Circular Collider, and may also be relevant for possible upgrades at the CMS and ATLAS experiments in the post phase-II era at the LHC.

The front-end channel described in this work exploits the Time-over-Threshold technique for the digitization of the signal delivered by the sensor. It includes a compact charge sensitive amplifier (CSA) equipped with two independent feedback paths, which are used for signal processing and for detector leakage current compensation. The signal processing loop includes an NMOS transistor which ultimately behaves as a constant current source, providing a linear discharge of the CSA feedback capacitance. The biasing structure for the feedback NMOS has been designed in such a way to ensure robustness against PVT variations and voltage drops on the power supply lines. The CSA is followed by a differential comparator, driving a Time-over-Threshold and a Time-of-Arrival counter. A 5-bit ADC is integrated in the elementary cell for the local tuning of the threshold. A prototype including a matrix of 8x32 readout channels (with a pitch of 25 μm x 100 μm) is being developed,

with a submission planned for Q3-2024. The discussion on the matrix integration, together with simulation results relevant to the analog front-end channel, will be reported.

Author: GAIONI, Luigi (University of Bergamo and INFN (IT))

Co-authors: STABILE, Alberto (Università degli studi di Milano); GALLIANI, Andrea (Università degli Studi di Bergamo); FALCHIERI, Davide (Universita e INFN, Bologna (IT)); TRAVERSI, Gianluca (University of Bergamo); RATTI, Lodovico (University of Pavia); FRONTINI, Luca; RE, Valerio (INFN)

Presenter: GAIONI, Luigi (University of Bergamo and INFN (IT))

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