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Radiation-Hard Smart-Pixel Detector ASIC ReadOut with Digital AI in 28nm

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Next-generation silicon pixel detectors with fine granularity will allow for precise measurements of particle tracks in both space and time. A reduction in the size of pixel data must be applied at the collision rate of 40MHz to fully exploit the pixel detector information of every interaction for physics analysis.
We developed radiation hard readout integrated circuit with on-chip digital artificial intelligence in 28nm CMOS. We will present hardware test results on the first prototype fabrications. Preliminary results indicate that reading out clusters from particles above a modest momentum threshold could enable using pixel information at 40MHz.

Summary (500 words)

Detectors at future high energy colliders will face enormous technical challenges. Disentangling the unprecedented numbers of particles expected in each event will require highly granular silicon pixel detectors with billions of readout channels. With event rates as high as 40 MHz, these detectors will generate petabytes of data per second. To enable discovery within strict bandwidth and latency constraints, future trackers must be capable of fast, power efficient, and radiation hard data-reduction at the source.
This effort is pursuing the co-design development of high-performance readout smart pixel ASICs for a future Phase III High Luminosity upgrade of the Large Hadron Collider.

A 1.6mm2 ASIC prototype was designed by Fermilab in CMOS 28 nm bulk process and submitted for manufacturing in February 2024. It leverages the analog front-end pixel design of a previous prototype fabricated and tested in 2023, which achieved a simulated detection level of ˜400e- with 30fF input capacitance.
The ROIC consists of two matrices of 16×16 smart pixels, each 25×25 μm2 in size. Each smart pixel contains a charge-sensitive preamplifier with leakage current compensation and three auto-zero comparators for a 2-bit flash-type ADC. There is digital space for the integration of our fully combinatorial AI that performs momentum classification at the bunch crossing rate. The total power consumption is ~6μW per pixel, which corresponds to ˜1mW/cm2.

The ASIC incorporates programmable front-end charge injection circuitry to generate pixel cluster charges during characterization. The cluster profile will be generated to duplicate hit characteristics of various momentum (pT). We will present early results from chip testing.

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