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Charge Collection Properties of a CMOS Sensor Produced in a 55 nm Process

We present the design and preliminary test results of a MAPS sensor, MIC6_Explorer0, based on a 55nm Quad-well CMOS Image Sensor process for high-energy physics experiment vertex detector applications. MIC6_Explorer0 comprises 3 large matrices and is intended to investigate the charge collection properties of the 55nm process with various MAPS design parameters, including pixel pitch, diode geometry, reset method, and readout circuit structure. Preliminary test results demonstrate that the pixel array with a 24μm x 24μm pixel pitch achieved a 95% charge collection efficiency when exposed to a 55Fe source.

Summary (500 words)

The vertex detector in high-energy physics experiments demands high spatial resolution, fast readout, and low power consumption. The Monolithic Active Pixel Sensor (MAPS) stands out as the most promising technology to fulfill all these requirements. A 55nm CMOS imaging sensor process has been selected because it allows for full CMOS utilization within the pixel, facilitated by the availability of a deep p-well. In this context, we developed the MAPS sensor MIC6_Explorer0 in the 55nm process to investigate the charge collection properties with various MAPS design parameters.

The MIC6_Explorer0 chip measures 3980μm×2145μm and comprises three matrices designed for various purposes. Matrix-1 features 18 sub-matrices of 16*16 pixels with serial analog output for studying pixel pitch, diode geometry, reset method and readout circuit structure. The pixel pitch of sub-matrices A1~A6, A7~A12, A13~A18 is 8 μm, 16 μm and 24 μm, respectively. A1~A6 are readout using a typical two-stage source follower method, while A7~A18 utilize the dual correlated double sampling readout method implemented by two capacitors within each pixel. The A1/A3/A5 sub-matrices are reset using diodes, while other sub-matrices are reset using MOS transistors. Matrix-2 consists of 21 mini-matrices of 4×4 pixels with parallel analog output for the studying pixel pitch, diode geometry, reset method, readout circuit structure and charge collection time within a cluster. The pixel pitch of mini-matrices B1~B9, B10~B15, B16~B21 are 24 μm, 16 μm and 8 μm, respectively. B1~B3 are readout using ALPIDE front-end circuit, while B4~B21 are readout using a two-stage source follower circuit. The B1~B6, B10~B12, B16~B18 mini-matrices are reset using diodes, while other mini-matrices are reset using MOS transistors. Matrix-3 includes 3 diode matrices without readout electronics for direct measurement of leakage current and sensing diode capacitance. These diode matrices are actually a certain number of diodes connected in parallel. The pixel size, N-well size, and spacing of the three types of diode test structures correspond to sub-matrices A4, A8, and A14, respectively.

The testing system comprises multi-channel, high-speed ADCs, DACs, an FPGA, and DAQ firmware to assess the performance of each matrix. The digital I/O of the chip is controlled by the FPGA. The chip's analog signals are sampled by the ADC, then processed by the FPGA and buffered in DDR3 memory before being transmitted to a PC via a 1 Gbps Ethernet interface. Test commands from the control software on the PC are received by the TCP/IP module. Subsequently, the ADCs, DACs and MIC6_Explorer0 controller module are configured by the FPGA according to the commands. Preliminary test results indicate that the pixel with a 24 μm×24 μm pixel pitch in mini-matrix B4 achieved a 95% charge collection efficiency when exposed to a 55Fe source.

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